MN55720

Gray Scale Font Engine

■ Overview

The MN55720 is a high-quality character generator IC that rapidly generates multilevel grayscale data from outline (path) data for characters and similar images. This IC includes input and output FIFO memory units to assure high-speed processing, and provides a local interface (16 or 32 bits) to allow the use of this IC in a wide range of equipment.

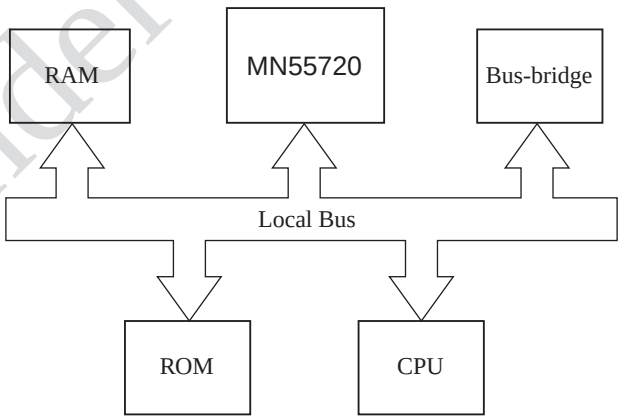
■ Features

- Gray scale levels: Can be set to any level from 2 to 128 levels.
- Bit sizes: Can generate characters of any size.
- Interface specifications: Local bus (Supports both 16-bit and 32-bit busses.)
- Operating frequency: 50 MHz to 70 MHz
- Operating supply voltage: External supply: 3.3 V±0.3 V
  Internal supply: 2.5 V±0.2 V
- Package: 80 pin TQFP (12 mm × 12 mm)

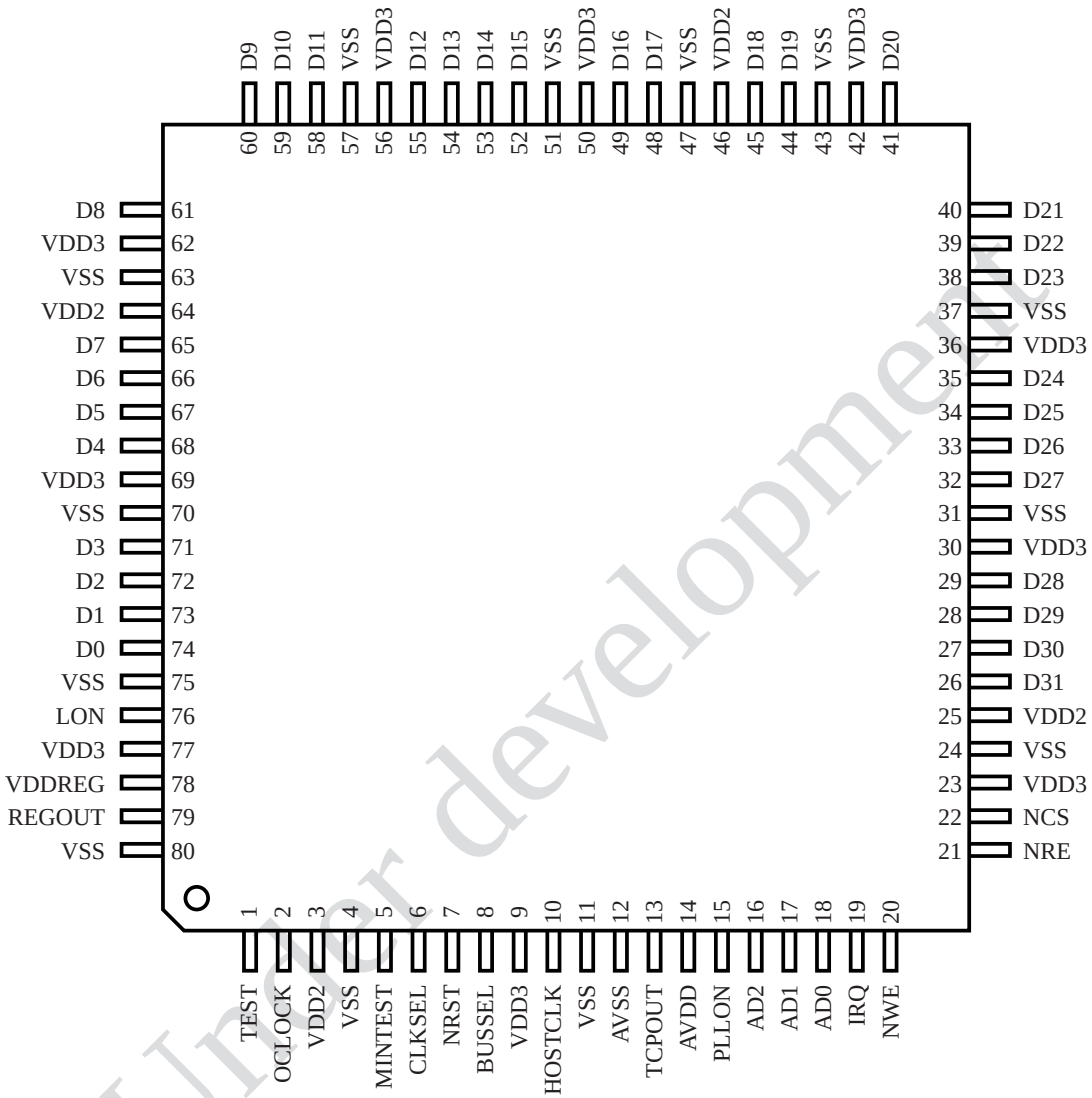
■ Applications

- STB and DTV

■ Block Diagrams



■ Pin Assignments



(TOP VIEW)

■ Pin Descriptions

1) Local 32-bit mode

Pin	I/O	Description
HOSTCLK	I	Clock input from the host
NRST	I	Hardware reset (active low)
AD[2:0]	I	Address signal from the host
NCS	I	Chip select signal from the host (active low)
NWE	I	Write enable signal from the host (active low)
NRE	I	Read enable signal from the host (active low)
D[31:0]	I/O	Data I/O (32-bit)
IRQ	O	Interrupt output to the host (active high)
BUSSEL	I	Data bus width setting (Must be held fixed at the high level)
CLKSEL	I	Clock selection (0: Low-speed clock used, 1: High-speed clock used)
MINTEST	I	Test pin
TEST	I	Test pin
PLLON	I	Test pin
OCLOCK	O	Test pin
TCPOUT	O	Test pin
LON	I	Regulator control (active high)
VDD3	I	3.3 V system power supply (I/O)
VDDREG	I	3.3 V power supply (regulator)
REGOUT	O	Regulator output (2.5 V)
VDD2	I	2.5 V system power supply (internal logic circuits)
VSS	—	Common ground for I/O and internal logic circuits
AVDD	I	PLL system analog power supply (3.3 V)
AVSS	—	PLL system analog ground

Note) 1. Connect the MINTEST pin to ground.
2. The NRST (hardware reset) signal pulse width must be at least 100 ns.

2) Local 16-bit mode

Pin	I/O	Description
HOSTCLK	I	Clock input from the host
NRST	I	Hardware reset (active low)
AD[2:0]	I	Address signal from the host
NCS	I	Chip select signal from the host (active low)
NWE	I	Write enable signal from the host (active low)
NRE	I	Read enable signal from the host (active low)
D[31:16]	I/O	Unused (These lines output fixed low-level signals.)
D[15:0]	I/O	Data I/O (16-bit)

■ Pin Descriptions (continued)

2) Local 16-bit mode (continued)

Pin	I/O	Description
IRQ	O	Interrupt output to the host (active high)
BUSSEL	I	Data bus width setting (Must be held fixed at the high level)
CLKSEL	I	Clock selection (0: Low-speed clock used, 1: High-speed clock used)
MINTEST	I	Test pin
TEST	I	Test pin
PLLON	I	Test pin
OCLOCK	O	Test pin
TCPOUT	O	Test pin
LON	I	Regulator control (active high)
VDD3	I	3.3 V system power supply (I/O)
VDDREG	I	3.3 V power supply (regulator)
REGOUT	O	Regulator output (2.5 V)
VDD2	I	2.5 V system power supply (internal logic circuits)
VSS	—	Common ground for I/O and internal logic circuits
AVDD	I	PLL system analog power supply (3.3 V)
AVSS	—	PLL system analog ground

Note) 1. Connect the MINTEST pin to VSS.
2. The NRST (hardware reset) signal pulse width must be at least 100 ns.

■ Power supply

1. Power on and off sequences

Do not apply power to one of the VDD2 and VDD3 supplies without applying power to the other at the same time. Failing to observe this may cause the problems listed below. The internal logic power supply VDD2 and the external I/O power supply VDD3 should be applied and cut as close to simultaneously as possible.

- Degradation of I/O block devices
- Inability to establish the states of the output and bidirectional pins even by setting NRST low.

2. Using the regulator

The MN55720 includes a built-in 2.5 V output regulator, which allows this device to function as a single 3.3 V power supply IC. However, since the voltage drop in the regulator is 0.8 V, the power consumption in just the regulator will be 80 mW when the IC draws 100 mA.

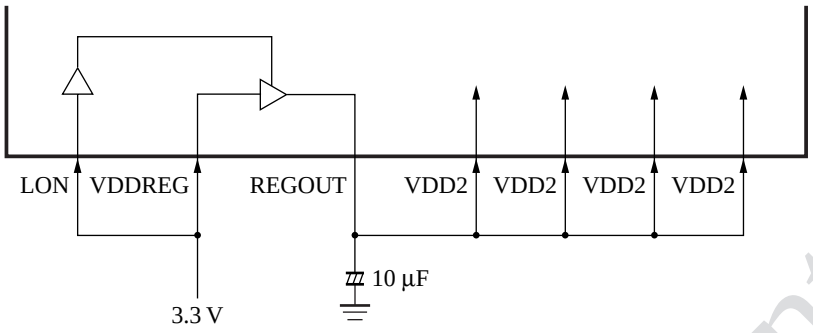
If a 2.5 V level is provided externally and the regulator is not used, provide a 3.3 V level to VDDREG as shown in the figure below.

Note that the 2.5 V regulator output cannot be used to supply other devices.

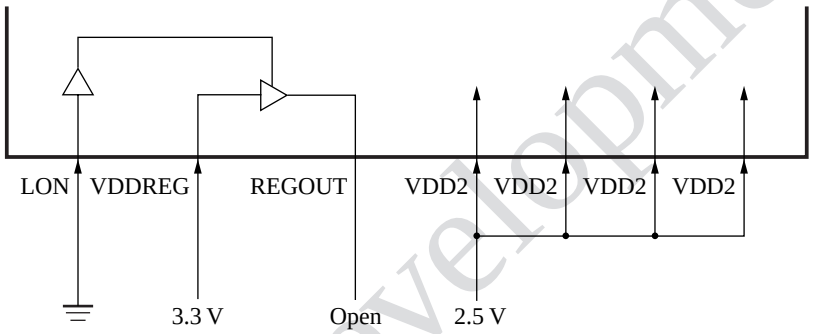
■ Power supply (continued)

2. Using the regulator (continued)

1) When using the regulator output to supply a 2.5 V level



2) When supplying the 2.5 V level externally



■ Functional Description

1. Register memory addresses

1) Memory address map

AD2	AD1	AD0	NAME	Content	R/W
0	0	0	POINT	Outline data input port	W
0	0	1	RASTER	Grayscale data output port	R

2) Register address map

AD2	AD1	AD0	NAME	Content	R/W
0	1	0	PSTATUS	POINT FIFO status	R
0	1	1	RSTATUS	RASTER FIFO status	R
1	0	0	CONTROL	Control register	R/W
1	0	1	VAL_LEVEL	Level value conversion register	R/W

3) Other items

AD2	AD1	AD0	NAME	Content	R/W
1	1	0	SRESET	Software reset	W

■ Functional Description (continued)

2. Memory and register contents

1) Outline data input port (POINT FIFO)

The POINT FIFO is a memory ports for input of the outline data that the MN55720 will expand. It can hold up to 256 double-word data items at the same time.

Data in excess of 256 double-word items must be processed separately.

The total capacity of the POINT FIFO is 256 double words.

- Outline data format (32-bit data)

- POINT FIFO memory map

■ Functional Description (continued)

2. Memory and register contents (continued)

2) Grayscale data output port (RASTER FIFO)

The RASTER FIFO is a memory port for output of the grayscale data created by the MN55720. It can hold up to 256 double-word data items at the same time.

Data in excess of 256 double-word items must be processed separately.

The total capacity of the RASTER FIFO is 256 double words.

- Grayscale data format (32-bit data)

- RASTER FIFO memory map

3) POINT FIFO status register (PSTATUS REGISTER)

This is a read-only register that indicates the status of the MN55720 POINT FIFO.

This register consists of 16 bits and uses the low-order 16 bits of the data bus.

bit 15	14	13	12	11	10	9 … 1	0
0	0	0	0	0	1	PNM	PAL

PNM(R): Indicates the amount of data written to the POINT FIFO.

A maximum of 256 double words of data that can be written to the POINT FIFO.

Maximum amount of data that can be written: 256 double words (0x001 to 0x100)

PAL(R): Indicates the LSB of the POINT FIFO address.

This bit is used for debugging when a 16-bit bus is used.

■ Functional Description (continued)

2. Memory and register contents (continued)

4) RASTER FIFO status register (STATUS REGISTER)

This is a read-only register that indicates the status of the MN55720 RASTER FIFO.
This register consists of 16 bits and uses the low-order 16 bits of the data bus.

bit 15	14	13	12	11	10	9	1	0
1	CNM					RNM		PAL

CNM (R) : Indicates the number of characters the data stored in the RASTER FIFO corresponds to.
RNM (R) : Indicates the amount of data that can be read from the RASTER FIFO.
This value indicates the amount of data for the first character.
Up to 256 double words (0x001 to 0x100)
RAL (R) : Indicates the LSB of the RASTER FIFO address.
This bit is used for debugging when a 16-bit bus is used.

5) CONTROL register (CONTROL REGISTER)

This is a read/write register that sets the MN55720 operating state.
This register consists of 16 bits and uses the low-order 16 bits of the data bus.

bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	PLI	RFL	PR	RR	END	SLP	IM	

PLI(R) : Indicates the initialization status after a hardware reset, software reset, or the clearing of sleep mode.
0 : Initialization complete
1 : Initialization in progress
RFL(R) : Indicates the data storage status of the RASTER FIFO.
1 : RASTER FIFO full (Read wait)
0 : RASTER FIFO not full
PR(R) : Indicates the status of the POINT FIFO.
1 : POINT FIFO writable
0 : POINT FIFO not writable
RR(R) : Indicates the status of the RASTER FIFO.
1 : RASTER FIFO readable
0 : RASTER FIFO not readable
END(R/W) : Sets the data output operation when a 16-bit bus is used.
This setting is only valid when the external pin BUSSEL is set to the low level.
1 : Lower 16 bits first, then upper 16 bits
0 : Upper 16 bits first, then lower 16 bits
SLP(R/W) : Sets sleep mode.
1 : Sets the MN55720 to sleep mode.
0 : Clears sleep mode.
IM(R/W) : The interrupt pin (the external IRQ pin) can be controlled by setting these bits.
00 : Interrupts are generated on all conditions. (default)
01 : POINT FIFO empty interrupt disabled.
10 : All interrupts are disabled for all conditions.
11 : All interrupts are disabled for all conditions.

■ Functional Description (continued)

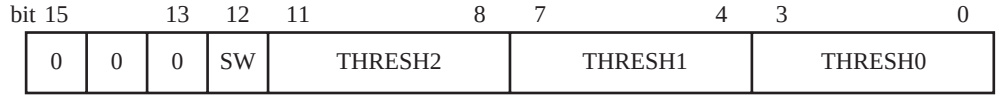
2. Memory and register contents (continued)

6) Level values conversion register (VAL_LEVEL REGISTER)

This is a read/write register that indicates the status of the level value conversion table.

This register consists of 16 bits and uses the low-order 16 bits of the data bus.

This IC is limited to converting 16-level data to 4-level data, and those conversion characteristics can be set freely using this register.



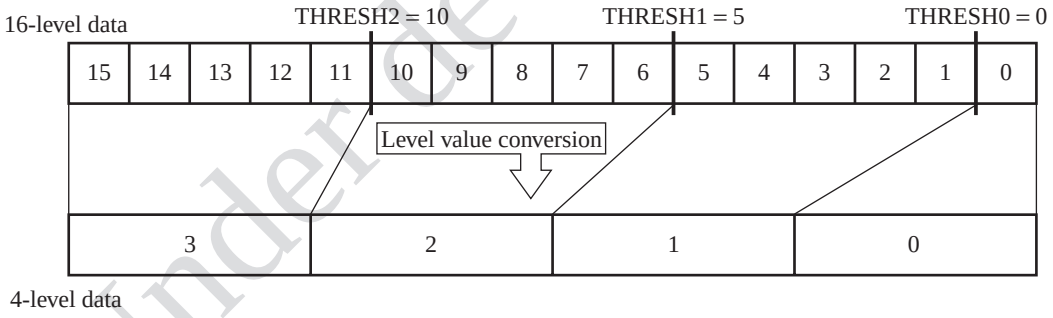
SW(R/W) : Indicates the on/off state of 16-level to 4-level conversion.
1: ON
0: OFF

THRESH2(R/W) : Conversion threshold
Set this field to a value in the range 0x0 to 0xF.
However, THRESH2 must be greater than THRESH1.

THRESH1(R/W) : Conversion threshold
Set this field to a value in the range 0x0 to 0xF.
However, THRESH1 must be greater than THRESH0.

THRESH0(R/W) : Conversion threshold
Set this field to a value in the range 0x0 to 0xF.

Note) Conversion example is shown below when VAL_LEVEL is set to 0x1a50.

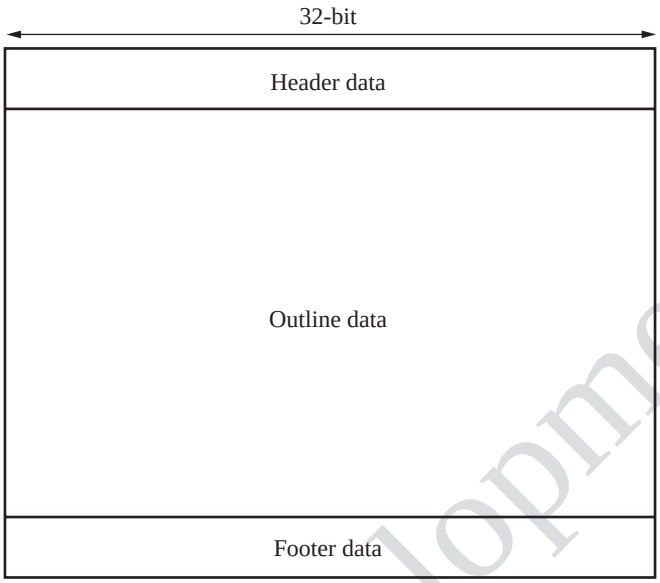


■ Functional Description (continued)

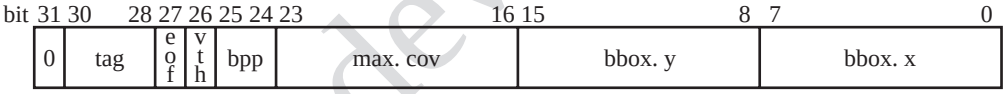
3. Input data format

This section presents the format of the outline data input to the MN55720.

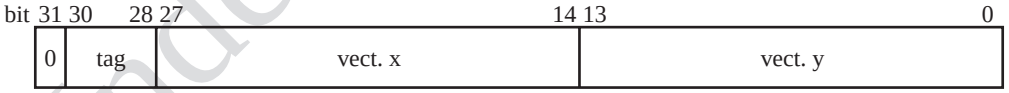
- Overall structure



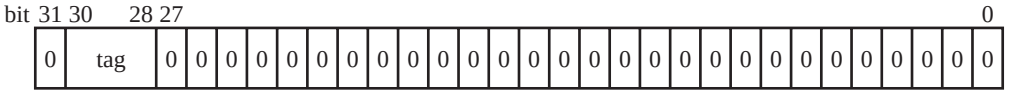
- Header structure



- Outline data structure



- Footer data structure



■ Functional Description (continued)

3. Input data format (continued)

- Parameter descriptions

tag	Data attributes 000 : header 001 : quadratic's or cubic's control point 1 010 : cubic's control point 2 011 : end of data 100 : begin contour 101 : end of line 110 : end of quadratic 111 : end of cubic
eof	Fill rule setting 0 : Use internal fill when outline segments cross. 1 : Do not use internal fill when outline segments cross.
vth	Threshold setting used when binary data is expanded. 0 : Off 1 : On
bpp	Setting for the number of output bits per pixel 00 : 1-bit 01 : 2-bit 10 : 4-bit 11 : 8-bit
max. cov	Level value setting for the frame being expanded. 0x01h to 0x7Fh (Two levels) (128 levels)
bbox. x	Output data width (X) for the frame being expanded. 0x00h to 0x1Fh (1 pixel) (32 pixel)
bbox. y	Output data width (Y) for the frame being expanded. 0x00h to 0x1Fh (1 pixel) (32 pixel)
vect. x	Vector data axis (X)
vect. y	Vector data axis (Y)

■ Functional Description (continued)

4. Output data format

This section presents the format of the grayscale data output by the MN55720.

- When bpp = 11 (Assuming bbox.x = n and bbox.y = m)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	pix[0]								pix[1]								pix[2]								pix[3]								line 0
1	pix[4]								pix[5]								pix[6]								pix[7]								
2	pix[8]								pix[9]								pix[10]								pix[11]								
	.....								.....								.....								.....								
	pix[n-2]								pix[n-1]								pix[n]								—								
	pix[0]								pix[1]								pix[2]								pix[3]								line 1
	pix[4]								pix[5]								pix[6]								pix[7]								
	pix[8]								pix[9]								pix[10]								pix[11]								
	.....								.....								.....								.....								
	pix[n-2]								pix[n-1]								pix[n]								—								
	⋮								⋮								⋮								⋮								⋮
	pix[0]								pix[1]								pix[2]								pix[3]								line m
	pix[4]								pix[5]								pix[6]								pix[7]								
	pix[8]								pix[9]								pix[10]								pix[11]								
	.....								.....								.....								.....								
	pix[n-2]								pix[n-1]								pix[n]								—								

- When bpp = 10 (Assuming bbox.x = n and bbox.y = m)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	pix[0]				pix[1]				pix[2]				pix[3]				pix[4]				pix[5]				pix[6]				pix[7]				line 0
1	pix[8]				pix[9]				pix[10]				pix[11]				pix[12]				pix[13]				pix[14]				pix[15]				
	.....				.....				.....				.....				.....				.....				.....				.....				
	pix[n-4]				pix[n-3]				pix[n-2]				pix[n-1]				pix[n]				—				—				—				
	pix[0]				pix[1]				pix[2]				pix[3]				pix[4]				pix[5]				pix[6]				pix[7]				line 1
	pix[8]				pix[9]				pix[10]				pix[11]				pix[12]				pix[13]				pix[14]				pix[15]				
	.....				.....				.....				.....				.....				.....				.....				.....				
	pix[n-4]				pix[n-3]				pix[n-2]				pix[n-1]				pix[n]				—				—				—				
	⋮				⋮				⋮				⋮				⋮				⋮				⋮				⋮				⋮
	pix[0]				pix[1]				pix[2]				pix[3]				pix[4]				pix[5]				pix[6]				pix[7]				line m
	pix[8]				pix[9]				pix[10]				pix[11]				pix[12]				pix[13]				pix[14]				pix[15]				
	.....				.....				.....				.....				.....				.....				.....				.....				
	pix[n-4]				pix[n-3]				pix[n-2]				pix[n-1]				pix[n]				—				—				—				

■ Functional Description (continued)

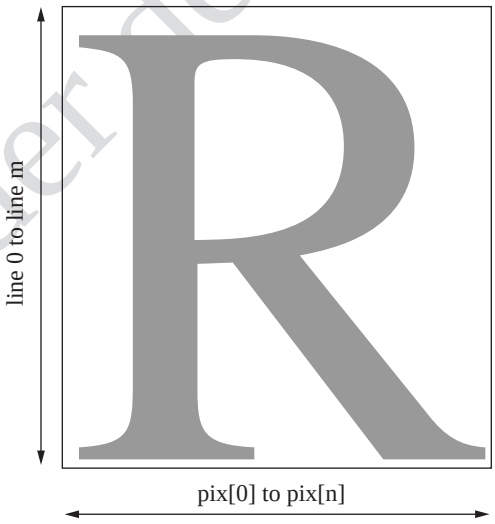
4. Output data format (continued)

- When bpp = 01 (Assuming bbox.x = 26 and bbox.y = m)

	31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0	
0	pix[0]	pix[1]	pix[2]	pix[3]	pix[4]	pix[5]	pix[6]	pix[7]	pix[8]	pix[9]	pix[10]	pix[11]	pix[12]	pix[13]	pix[14]	pix[15]	line 0
1	pix[16]	pix[17]	pix[18]	pix[19]	pix[20]	pix[21]	pix[22]	pix[23]	pix[24]	pix[25]	pix[26]	—	—	—	—	—	
2	pix[0]	pix[1]	pix[2]	pix[3]	pix[4]	pix[5]	pix[6]	pix[7]	pix[8]	pix[9]	pix[10]	pix[11]	pix[12]	pix[13]	pix[14]	pix[15]	line 1
3	pix[16]	pix[17]	pix[18]	pix[19]	pix[20]	pix[21]	pix[22]	pix[23]	pix[24]	pix[25]	pix[26]	—	—	—	—	—	
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	pix[0]	pix[1]	pix[2]	pix[3]	pix[4]	pix[5]	pix[6]	pix[7]	pix[8]	pix[9]	pix[10]	pix[11]	pix[12]	pix[13]	pix[14]	pix[15]	line m
	pix[16]	pix[17]	pix[18]	pix[19]	pix[20]	pix[21]	pix[22]	pix[23]	pix[24]	pix[25]	pix[26]	—	—	—	—	—	

- When bpp = 00 (Assuming bbox.x = 29 and bbox.y = m)

	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0	
0	← pix[0:29] →	– –	line 0
1	← pix[0:29] →	– –	line 1
2	← pix[0:29] →	– –	line 2
	⋮	⋮	⋮
	← pix[0:29] →	– –	line m



■ Operational Description

1. Pin settings

This section presents the pin settings and conditions that control the operating state of the MN55720.

1) Clock setting

Set the clock setting pin (CLKSEL) according to the table below.

- Clock pin settings

CLKSEL	HOSTCLK frequency	Internal operating frequency
0	25 MHz to 35 MHz	50 MHz to 70 MHz
1	50 MHz to 70 MHz	50 MHz to 70 MHz

2) Bus width setting

Set the bus width setting pin (BUSSEL) according to the table below.

- Bus width pin settings

BUSSEL	Bus width
0	16-bit bus
1	32-bit bus

2. Operating procedures

This section presents the operating procedures used with the MN55720.

1) Overview of operating procedures

- Initialization

  Initialization is the processing performed after a hardware reset, and consists of clearing the memory and setting the operating conditions.

- Interrupt signal wait

  The interrupt signal wait operation consists of waiting until the issues of external interrupts.

- Outline data write

  The outline data write operation consists of the input processing required to generate multilevel grayscale data.

- Grayscale data readout

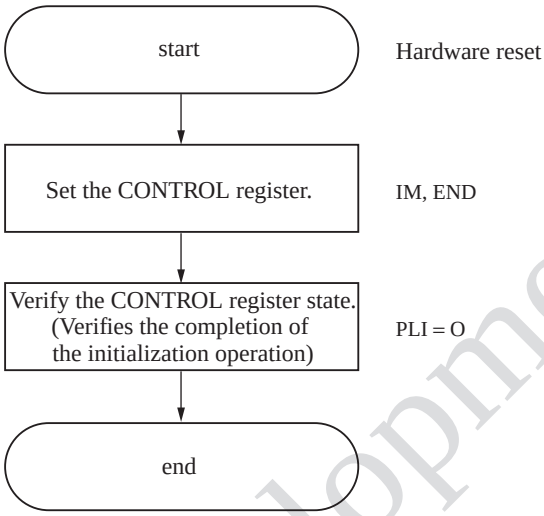
  The grayscale data readout operation consists of the output processing for the generated multilevel grayscale data.

■ Operational Description (continued)

2. Operating procedures (continued)

2) Initialization

- Flowchart for the initialization operation



- Description of the initialization flowchart steps

The registers are initialized by the reset operation due to a hardware reset (NRST), and memory initialization processing starts automatically.

- Set the CONTROL register.

This operation consists of setting the conditions for the interrupts (IRQ) generated and setting the endian type if a 16-bit bus is used. If the CONTROL register is not set explicitly, the MN55720 will operate at the initial conditions.

- Verify the CONTROL register state.

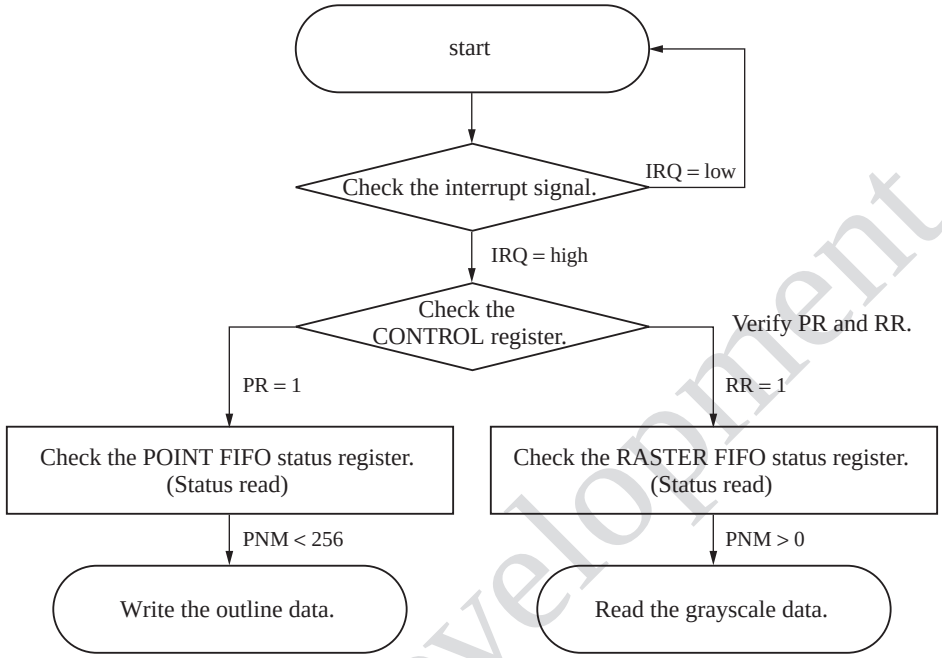
This operation consists of reading out the CONTROL register and verifying that PLI is 0. If PLI is not 0, wait for a brief period and read the CONTROL register again.

■ Operational Description (continued)

2. Operating procedures (continued)

3) Interrupt signal wait operation

- Flowchart for the interrupt signal wait operation



- Description of the interrupt signal wait operation flowchart steps

Changes in the internal state can be verified by recognizing the interrupt signal issued.

- Check the interrupt signal.

Monitor the interrupt signal (IRQ) until the conditions set in the CONTROL register are met and the MN55720 asserts the interrupt signal (IRQ).

- Check the CONTROL register.

Read the CONTROL register and verify that either PR or RR is 1.

If neither PR nor RR is 1, read the CONTROL register again.

After checking the PR and RR bits and determining the interrupt type, determine which processing must be performed next.

- Check the POINT/RASTER FIFO status register.

Read either the POINT or RASTER FIFO status register, depending on the status of the PR and RR bits.

Perform the outline data write or grayscale data read operation required according to the PNM or RNM value in the POINT or RASTER FIFO status register.

- Notes

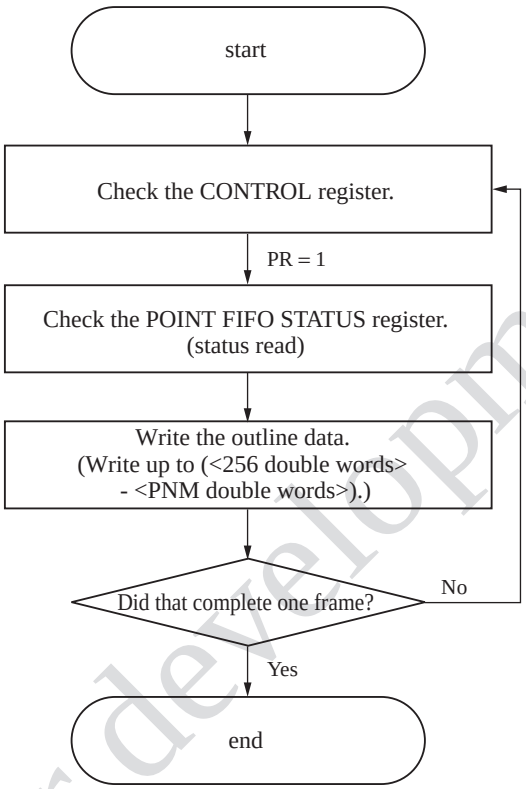
If the IRQ pin signal is not used, check the CONTROL register periodically and perform the processing that follows the CONTROL register check operation in the flowchart above according to bits 4 and 5 in the CONTROL register.

■ Operational Description (continued)

2. Operating procedures (continued)

4) Outline data write operation

- Flowchart for the outline data write operation



- Description of the outline data write operation flowchart steps

  This operation writes the outline data for processing.

  - Check the CONTROL register.

    Read the CONTROL register. If PR is 1, then outline data can be written.

  - Check the POINT FIFO STATUS register.

    Read the POINT FIFO STATUS register and determine the value of the PNM field.

  - Write the outline data.

    Input up to (<256 double words> - <PNM double words>) of outline data to the outline data input port (POINT FIFO).

  - Terminate a single frame

    If the outline data write operation complete the input of outline data for a single character, the processing required for this operation has been completed.

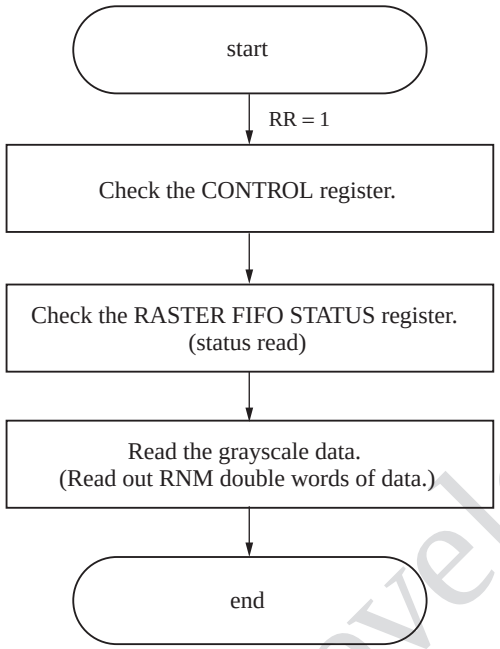
    If there is remaining outline data that must be input, check the CONTROL register again and perform the write operation described above again.

■ Operational Description (continued)

2. Operating procedures (continued)

5) Grayscale data read operation

- Flowchart for the grayscale data read operation



RNM read

RNM : 001h (1 double-word) to
100h (256 double-word)

- Description of the grayscale data read operation flowchart steps

  This operation reads out the grayscale data generated.

  - Check the CONTROL register.

    Read the CONTROL register. If the RR bit is 1, then there is grayscale data to read.

  - Check the RASTER FIFO STATUS register.

    Read the RASTER FIFO STATUS register, and determined the value of the RNM field.

  - Read the grayscale data.

    The multilevel grayscale data for a single character can be read out from the grayscale data output port (RASTER FIFO).

    The maximum amount of grayscale data that can be output at a time is 256 double words. The amount of grayscale data that can be read out is indicated by RNM. Read individual double words RNM times to read out all the grayscale data.

    Reading out the number of double words indicated by RNM completes the readout of the grayscale data for a single multilevel character.

  - Terminate a single frame

    When reading out the grayscale data completes the grayscale data output for a single character, that completes the processing.

    If the data for multiple characters is stored (that is, if CNM is greater than 1), read out grayscale data CNM times.

■ Operational Description (continued)

3. Sleep mode settings

1) Sleep mode operation

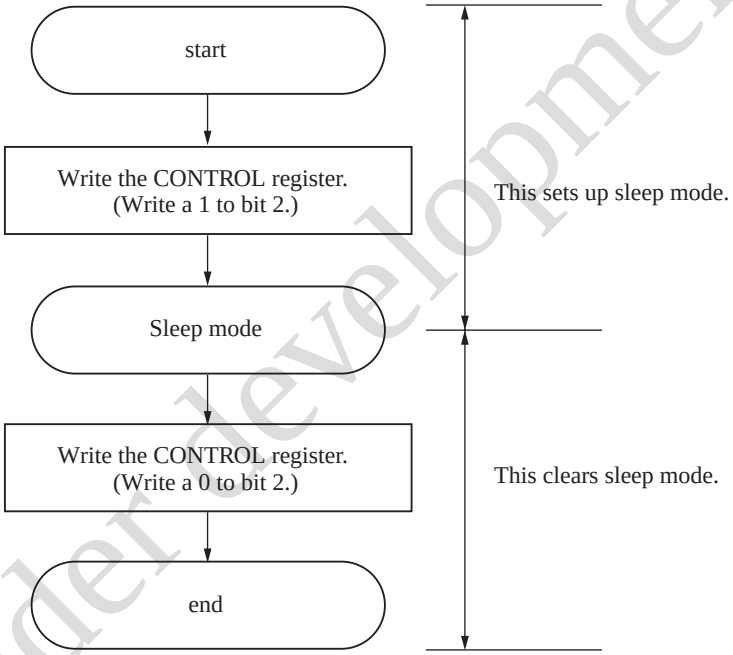
The internal operating clock can be stopped and the device set to sleep mode by setting bit 2 (SLP) in the CONTROL register to 1.

After using this IC's internal outline data processing, write a 1 to bit 2 in the CONTROL register when that processing has completed. Note that this IC's internal data is not guaranteed after it is switched to sleep mode.

Sleep mode can be cleared by writing a 0 to bit 2 in the CONTROL register. Note that after sleep mode is cleared, the IC automatically applies an internal reset.

The CONTROL register does not need to be set up again after sleep mode has been cleared, that is, it retains the state it had prior to sleep mode.

- Sleep mode flowchart



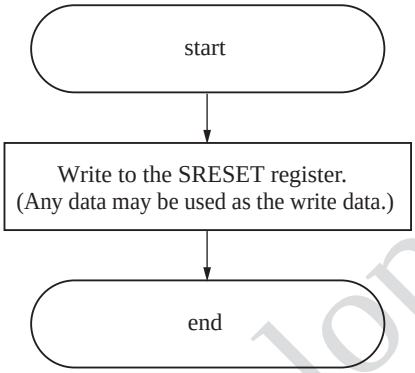
■ Operational Description (continued)

4. Software reset procedure

1) Software reset operation

A software reset can be applied by writing the SRESET register. Any value whatsoever can be used as the data written. A software reset can be applied before or after writing data to, or reading data from, FIFOs or registers. However, since whole internal data is reset, it will be necessary to set up the CONTROL register again after the software reset.

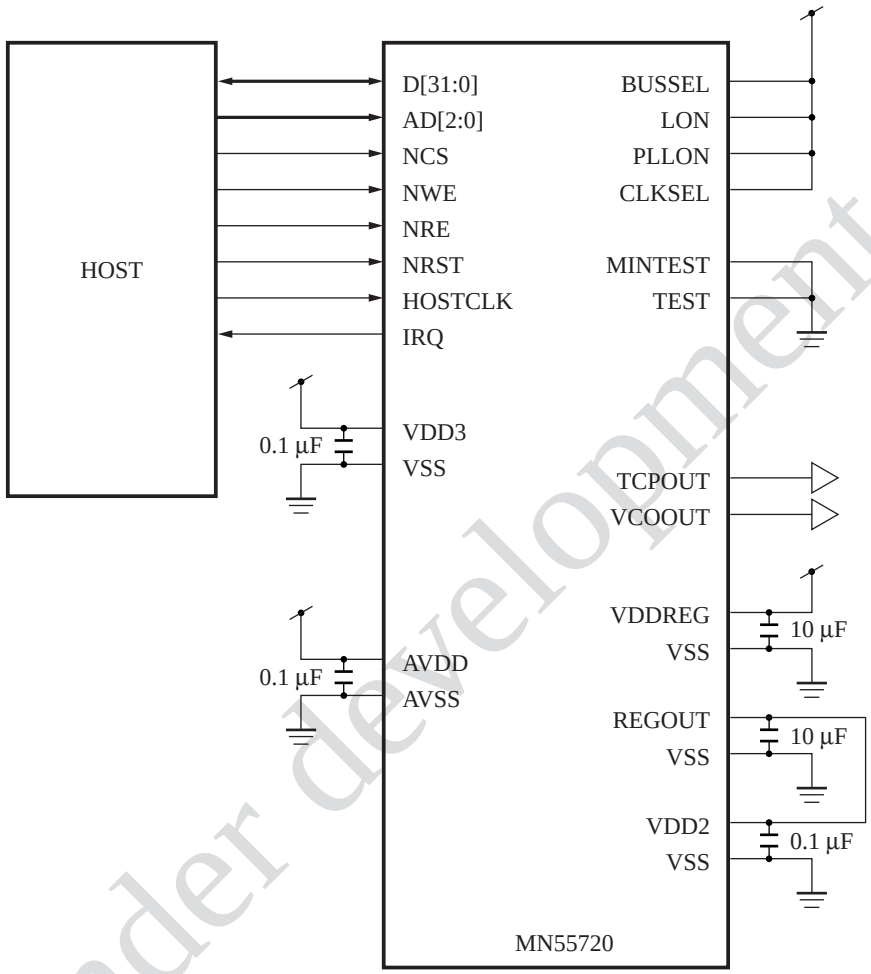
- Software reset flowchart



■ External Connection Examples

1. Connections used in 32-bit mode

The figure presents an example of external connections used with the MN55720.

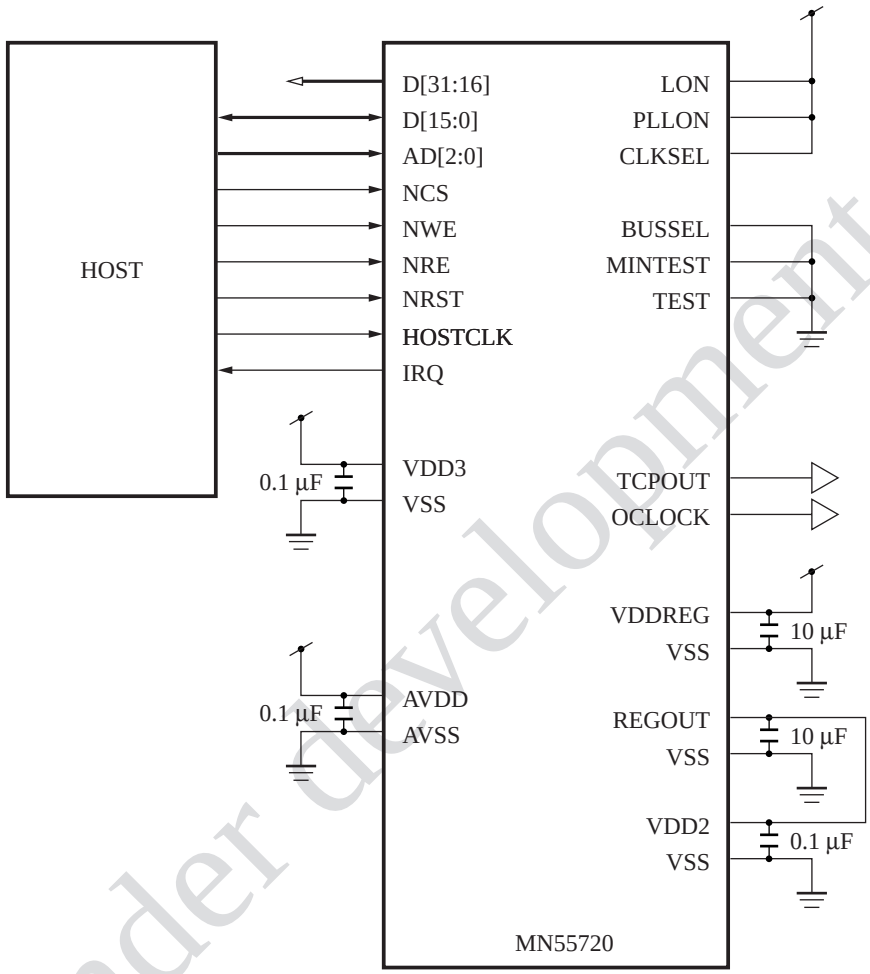


Note) The CLKSEL setting (fixed at the high level) shown here is used when a high-speed clock (50 MHz to 70 MHz) is used.
If a low-speed clock (25 MHz to 25 MHz) is used, CLKSEL must be connected to a low level.
The example shown here is a circuit that uses the built-in regulator. See the section Power Supply, 2. Regulator usage, for the circuit required to use an external 2.5 V supply.

■ External Connection Examples (continued)

2. Connections used in 16-bit mode

The figure presents an example of external connections used with the MN55720.



Note) The CLKSEL setting (fixed at the high level) shown here is used when a high-speed clock (50 MHz to 70 MHz) is used.
If a low-speed clock (25 MHz to 25 MHz) is used, CLKSEL must be connected to a low level.
The example shown here is a circuit that uses the built-in regulator. See the section Power Supply, 2. Regulator usage, for the circuit required to use an external 2.5 V supply.

■ Electrical Characteristics

1. Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
External supply voltage *	V_{DD}	– 0.3 to +4.6	V
Internal supply voltage *	V_{DDI}	– 0.3 to +3.6	V
Input pin voltage	V_I	– 0.3 to V_{DD}+0.3 (Upper limit: 4.6 V)	V
Output pin voltage	V_O	– 0.3 to V_{DD}+0.3 (Upper limit: 4.6 V)	V
Output current (Type HL4 pins)	I_O	±12	mA
Output current (Type HL8 pins)	I_O	±24	mA
Power supply input current	I_V	±70 (Per pin)	mA
Power dissipation	P_D	T.B.D.	mW
Operating temperature	T_{opr}	–10 to +70	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note) 1. *: Apply and remove the power supply voltages at as close to the same time as possible.
2. Type HL4 pins: IRQ and CLOCK
Type HL8 pins: D0 to D31
3. The absolute maximum ratings are limit values for stresses applied to the chip so that the chip will not be destroyed. Operation is not guaranteed within these ranges.
4. All the VDD and VSS pins must be connected to the external corresponding power supply or ground.

2. Recommended Operating Conditions at V_{SS} = 0 V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
External supply voltage	V_{DD}		3.0	3.3	3.6	V
Internal supply voltage *	V_{DDI}		2.3	2.5	2.7	V
Operating temperature	T_{opr}		–10	—	70	°C
Input rise time	t_r		0	—	100	ns
Input fall time	t_f		0	—	100	ns

Note) ∗: The guaranteed values for the internal supply voltage apply when power is provided directly from and external supply. (When the regulator is not used.)

3. I/O Capacitances at V_{SS} = 0 V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input pins	C_I	$V_{DD} = V_I = 0$ V	—	7	8	pF
Output pins	C_O	f = 1 MHz	—	7	8	pF
I/O pins	$C_{I/O}$	T_{opr} = 25°C	—	7	8	pF

■ Electrical Characteristics (continued)

4. DC Characteristics

V_{DD} = 3.0 V to 3.6 V, V_{DDI} = 2.3 V to 2.7 V, V_{SS} = 0 V, f_{TEST} = 70 MHz, T_{opr} = −10°C to +70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating current drain	I_{DDO}	$V_I = V_{DD}$ or V_{SS} , f = 70 MHz, V_{DD} = 3.3 V V_{DDI} = 2.5 V, outputs open	—	—	20 *	mA
Current drain with the internal supply operating	I_{DDIO}	$V_I = V_{DD}$ or V_{SS} , f = 70 MHz, V_{DD} = 3.3 V V_{DDI} = 2.5 V, outputs open	—	—	180 *	mA
LVCMOS input level pins: HOSTCLK, NRST, AD0 to AD2, NCS, NWE, NRE, BUSSEL, CLKSEL, TEST, PLLON, LON						
High-level input voltage	V_{IH}		$V_{DD} \times 0.7$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.3$	V
Input leakage current	I_{LI}	$V_I = V_D$ or V_{SS}	—	—	±10	µA
LVCMOS input level pins with built-in pull-down resistor: MINTEST						
High-level input voltage	V_{IH}		$V_{DD} \times 0.7$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.3$	V
Pull-down resistor	R_{IL}	$V_I = V_{DD}$	10	30	90	kΩ
Input leakage current	I_{LIL}	$V_I = V_{SS}$	—	—	±10	µA
LVCOM I/O level pins: D0 to D31						
High-level input voltage	V_{IH}		$V_{DD} \times 0.7$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.3$	V
High-level output voltage	V_{OH}	I_{OH} = −8.0 mA $V_I = V_{DD}$ or V_{SS}	$V_{DD} \times 0.7$	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 8.0 mA $V_I = V_{DD}$ or V_{SS}	—	—	$V_{DD} \times 0.3$	V
Output leakage current	I_{LO}	V_O = high-impedance state $V_I = V_{DD}$ or V_{SS} $V_O = V_{DD}$ or V_{SS}	—	—	±10	µA
Push-pull outputs: OCLOCK and IRQ						
High-level output voltage	V_{OH}	I_{OH} = −4.0 mA $V_I = V_{DD}$ or V_{SS}	$V_{DD} \times 0.7$	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 4.0 mA $V_I = V_{DD}$ or V_{SS}	—	—	$V_{DD} \times 0.3$	V

Note) *: These values are preliminary.

■ Electrical Characteristics (continued)

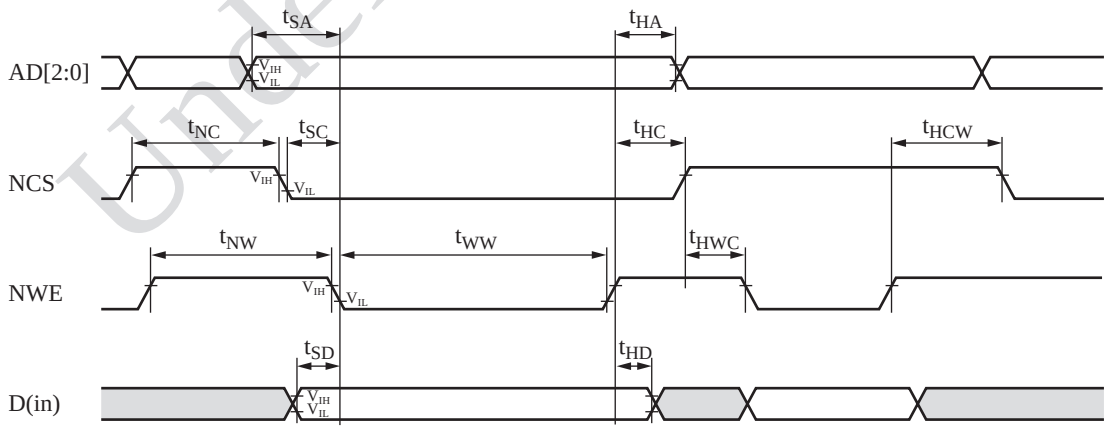
5. AC Characteristics

1) Register and memory access timing

Parameter	Symbol	Min	Max	Unit
Address setup	t_{SA}	0	—	ns
Address hold	t_{HA}	2	—	ns
Data setup	t_{SD}	0	—	ns
Data hold	t_{HD}	2	—	ns
NCS setup	t_{SC}	0	—	ns
NCS hold	t_{HC}	2	—	ns
NCS negated period	t_{NC}	HCK+1	—	ns
NWE hold time during the NCS negated period	t_{HWC}	5	—	ns
NRE hold time during the NCS negated period	t_{HRC}	5	—	ns
NWE pulse width	t_{WW}	HCK+2	—	ns
NWE negated period	t_{NW}	HCK+1	—	ns
NCS hold time during the NWE negated period	t_{HCW}	5	—	ns
NRE pulse width	t_{WR}	2 × HCK+5	—	ns
NRE negated period	t_{NR}	HCK+1	—	ns
NCS hold time during the NRE negated period	t_{HCR}	5	—	ns
NRE access time	t_{AR}	—	1HCK+12.3	ns
Data output hold time	t_{HRD}	2	—	ns

Note) HCK is the HOSTCLK clock cycle time

• Write cycle

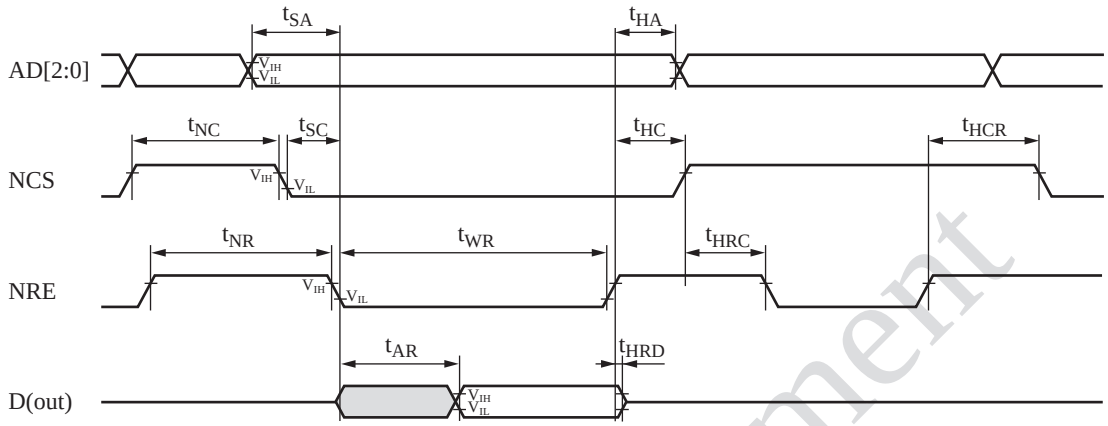


■ Electrical Characteristics (continued)

5. AC Characteristics (continued)

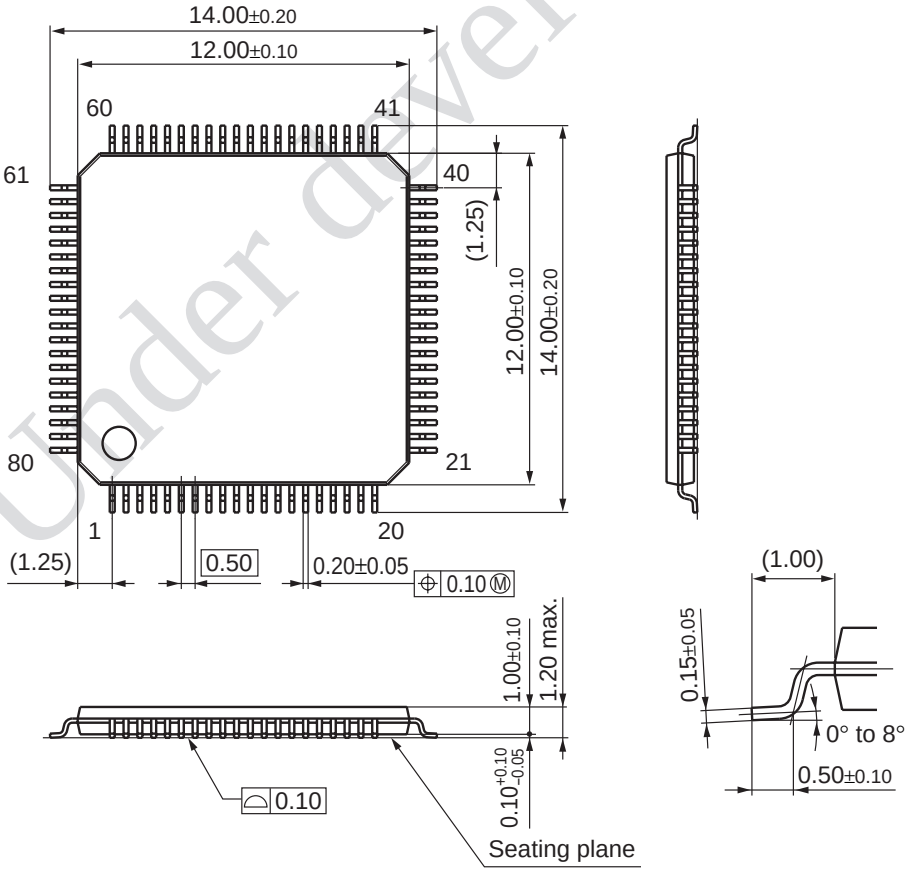
1) Register and memory access timing (continued)

- Read cycle



■ Package Dimensions (Unit: mm)

- TQFP080-P-1212D (Lead free)



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