MN66621BRG

MD Record/Playback IC with ATRAC3 Support

■ Overview

The MN66621BRG MD Record/Playback IC integrates functions of ATRAC encoding and decoding processing, sampling frequency conversion, digital servo, digital signal-processing, and memory controller on a single chip.

A full-functionality MD player/recorder can be implemented by combining the MN66621BRG with an RF IC (the Panasonic AN22011A), DRAM, A/D and D/A converters, and a microcontroller.

■ Features

ATRAC Compression/Expansion Functions

- MDLP encoding/decoding support (LP2/LP4)
- ATRAC encoding/decoding support (stereo and mono)
- High-speed recording support (4× speed for all of the ATRAC, LP2, and LP4 modes)
- High-fidelity encoding algorithms (ATRAC/LP2/LP4)
- Uses a 24-bit digital signal processor (DSP)
- Digital volume control with 10-bit smooth fade function
  (Playback: – ∞ dB to +18 dB, common left and right setting. Record: – ∞ dB to +18 dB, independent left and right settings.)
- Peak level detection function
- Silent segment detection function
- Bass and treble boost functions
- Low headphone sound leakage position (ASC)
- Digital audio interface (IEC 958 conformant)
- On-chip CD IC interface (audio and subcode data)

Sampling Frequency Converter Function

- Supported frequencies: 32 kHz, 44.1 kHz, 48 kHz

Digital Signal-Processing Functions

- ACIRC error correction (C1: double correction, C2: quadruple correction)
- C1 error flag detection function

Audio D/A Converter

- On-chip audio D/A converter system, including a low-pass filter

Memory Controller

- Supported external DRAM organizations: 1 Mbit,
  1 Mbit × 2, 4 Mbits, 4 Mbits × 2, 16 Mbits, 16 Mbits × 2, 64 Mbits.
- The microcontroller can access external DRAM (The capacity used can be set under program control.)
  (Example) If the microcontroller uses 2 KB as a work area plus the area for 9 UTOC sectors in the external DRAM, the amount of data area available for shock prevention memory (SPM) will be as follows.
  Assuming one 4 Mbit DRAM is used: 4 Mbit is 1 024 × 1 024 × 4 = 4 194 304 bits
  Converting to bytes gives: 4 194 304/8 = 524 288 bytes
  Working area of 2 KB: 1 024 × 2 = 2 048 bytes
  Since 1 UTOC sector is 2 344 bytes, 9 sectors is: 2 344 × 9 = 21 096 bytes
  The remaining area after subtracting work area and UTOC area will be:
  524 288 - 2 048 -21 096 = 510 144 bytes
  Dividing the remaining memory by the number of bytes in a sector (2 344 bytes) gives:
  501 144/2 344 = 213.8 -> 213 sectors
  Similar calculations give:
  46 sectors/1 Mbit, 101 sectors/2 Mbits, 884 sectors/16 Mbits, 3 568 sectors/64 Mbits

■ Features (continued)

Memory Controller (continued)

- Simple TOC/UTOC editing commands
- TOC/UTOC playback functions during recording

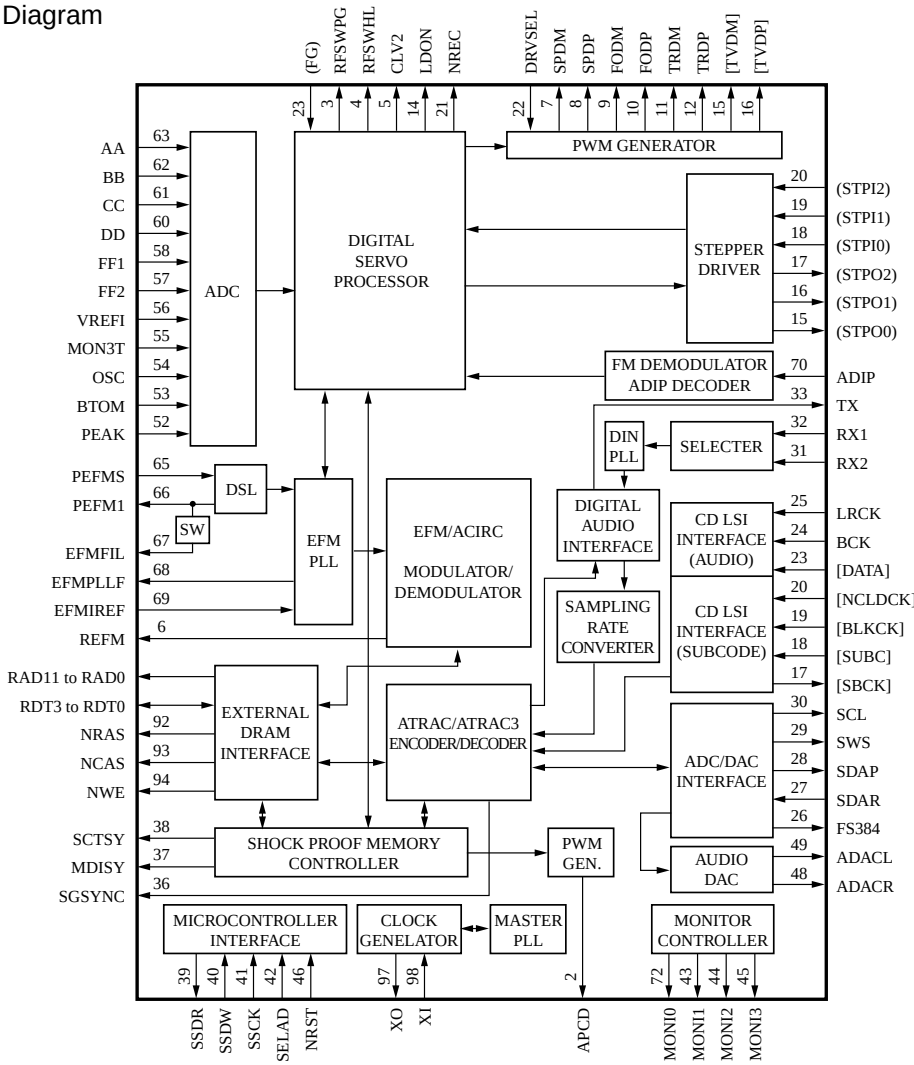
Digital Servo

- Focus, tracking, traverse, and spindle (EFM/ADIP/FG) servos
  Note that the FG servo system only applies when a stepping motor is used.
- The traverse servo system supports both stepping and DC motors.
- Supports three types of PWM output as servo outputs.
- Status detection function: TRCRS, OFTR, BDO, NTJ, NRFDET, FLOCK, TLOCK, and SLOCK outputs provid
- Bit detection function

■ Applications

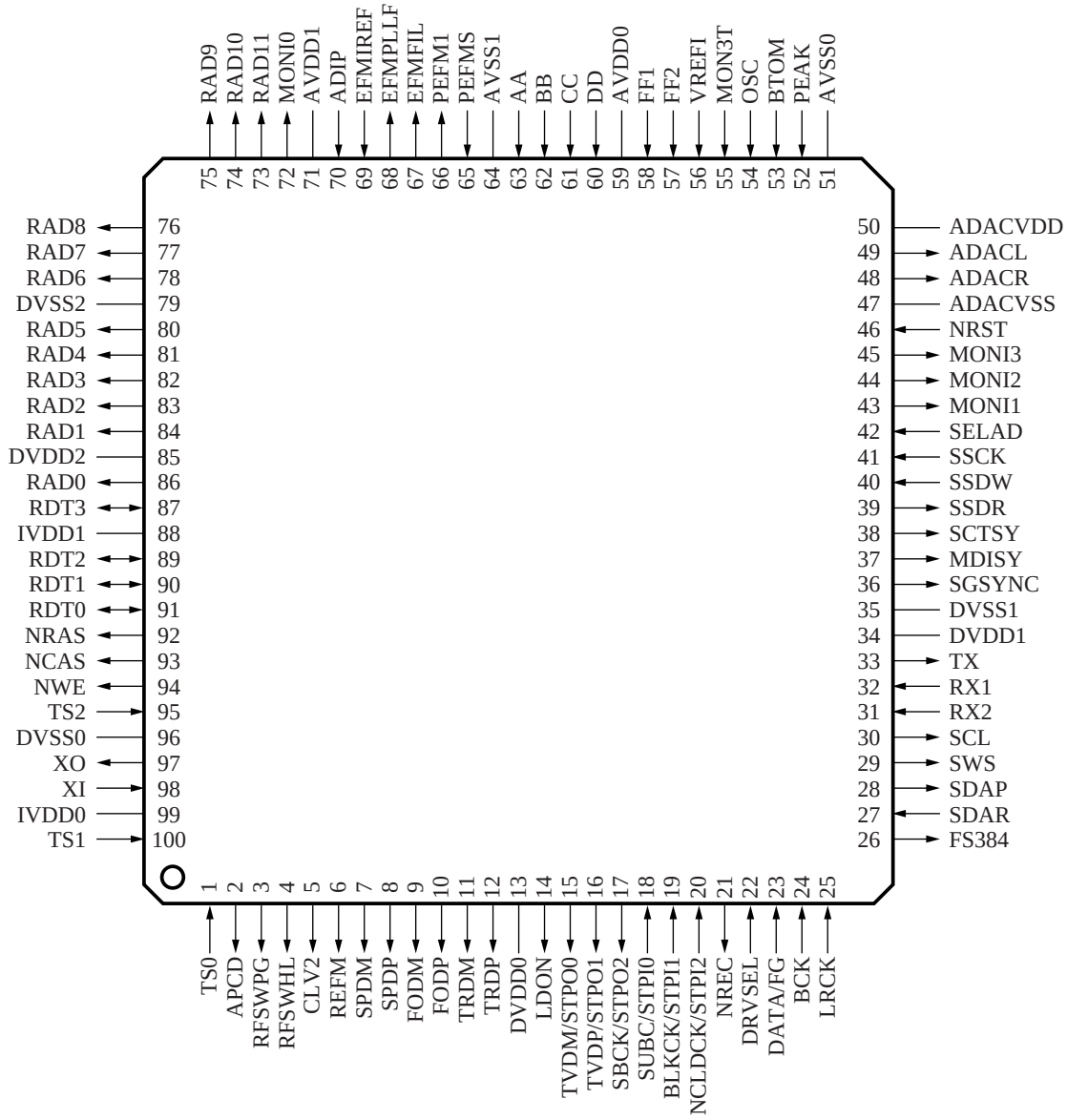
- MD players and MD recorders

■ Block Diagram



Note) The MN66621BRG allows either a stepping motor or a DC motor to be selected for the sled system. Items in parentheses "( )" apply when a stepping motor is used, and items in square brackets "[ ]" apply when a DC motor is used.

■ Pin Arrangement



(TOP VIEW)

■ Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	TS0	DI	Test mode control input 0
2	APCD	DO	Laser power setting PWM output
3	RFSWPG	DO	Pit/groove setting signal
4	RFSWHL	DO	High/low reflectivity setting signal
5	CLV2	DO	Linear velocity switching signal
6	REFM	DTO	EFM signal output
7	SPDM	DTO	Spindle minus side drive signal
8	SPDP	DTO	Spindle plus side drive signal
9	FODM	DTO	Focus minus side drive signal
10	FODP	DTO	Focus plus side drive signal
11	TRDM	DTO	Tracking minus side drive signal
12	TRDP	DTO	Tracking plus side drive signal
13	DVDD0	DVDD	Digital system power supply 0
14	LDON	DO	Laser diode on/off control signal
15	TVDM/STPO0	DTO	Traverse minus side drive signal, stepper drive signal 0
16	TVDP/STPO1	DTO	Traverse plus side drive signal, stepper drive signal 1
17	SBCK/STPO2	DO	Subcode Q register clock output, stepper drive signal 2
18	SUBC/STPI0	DI	Subcode Q code input, stepper status input 0
19	BLKCK/STPI1	DI	Subcode block clock signal input, stepper status input 1
20	NCLDCK/STPI2	DI	Subcode frame clock signal input, stepper status input 2
21	NREC	DO	Record/playback switching signal output
22	DRVSEL	DSI	Driver mode selection input
23	DATA/FG	DSI	CD input audio data, FG input
24	BCK	DI	CD input bit clock
25	LRCK	DI	CD input word clock
26	FS384	DO	External A/D and D/A converter reference clock
27	SDAR	DI	Audio data input
28	SDAP	DO	Audio data output
29	SWS	DO	Word clock output
30	SCL	DO	Bit clock output
31	RX2	DI	Digital audio interface input 2
32	RX1	DI	Digital audio interface input 1
33	TX	DO	Digital audio interface output
34	DVDD1	DVDD	Digital system power supply 1

Note) I/O column notation

DI: Digital input pin, DO: Digital output pin, DIO: Digital I/O pin, DSI: Digital I/O pin with Schmitt trigger circuit, DTO: Tristate digital output pin, AI: Analog input pin, AO: Analog output pin

■ Pin Descriptions (continued)

Pin No.	Pin Name	I/O	Description
35	DVSS1	DVSS	Digital system ground 1
36	SGSYNC	DO	ATRAC processing frame sync signal
37	MDISY	DO	Microcontroller interrupt signal 1
38	SCTSY	DO	Microcontroller interrupt signal 2
39	SSDR	DO	Read data (microcontroller interface)
40	SSDW	DSI	Write data (microcontroller interface)
41	SSCK	DSI	Shift clock (microcontroller interface)
42	SELAD	DSI	Address signal selection signal (microcontroller interface)
43	MONI1	DO	Monitor output 1
44	MONI2	DO	Monitor output 2
45	MONI3	DO	Monitor output 3
46	NRST	DSI	Reset signal input
47	ADACVSS	AVSS	Audio D/A converter ground
48	ADACR	AO	Audio output: right channel
49	ADACL	AO	Audio output: left channel
50	ADACVDD	AVDD	Audio D/A converter power supply
51	AVSS0	AVSS	Analog system ground 0
52	PEAK	AI	Servo A/D converter input signal
53	BTOM	AI	Servo A/D converter input signal
54	OSC	AI	Servo A/D converter input signal
55	MON3T	AI	Servo A/D converter input signal
56	VREFI	AI	Center point voltage input (reference voltage)
57	FF2	AI	Servo A/D converter input signal
58	FF1	AI	Servo A/D converter input signal
59	AVDD0	AVDD	Analog system ground 0
60	DD	AI	Servo A/D converter input signal
61	CC	AI	Servo A/D converter input signal
62	BB	AI	Servo A/D converter input signal
63	AA	AI	Servo A/D converter input signal
64	AVSS1	AVSS	Analog system ground 1
65	PEFMS	AI	EFM signal input
66	PEFM1	AO	EFM data slicing loop filter pin 1
67	EFMFIL	AO	EFM data slicing loop filter pin 2
68	EFMPLLF	AO	EFM PLL filter pin

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■ Pin Descriptions (continued)

Pin No.	Pin Name	I/O	Description
69	EFMIREF	AI	EFM PLL reference current setting pin
70	ADIP	AI	ADIP signal input
71	AVDD1	AVDD	Analog system power supply 1
72	MONI0	DO	Monitor output 0
73	RAD11	DO	DRAM address output 11
74	RAD10	DO	DRAM address output 10
75	RAD9	DO	DRAM address output 9
76	RAD8	DO	DRAM address output 8
77	RAD7	DO	DRAM address output 7
78	RAD6	DO	DRAM address output 6
79	DVSS2	DVSS	Digital system ground 2
80	RAD5	DO	DRAM address output 5
81	RAD4	DO	DRAM address output 4
82	RAD3	DO	DRAM address output 3
83	RAD2	DO	DRAM address output 2
84	RAD1	DO	DRAM address output 1
85	DVDD2	DVDD	Digial system power supply 2
86	RAD0	DO	DRAM address output 0
87	RDT3	DIO	DRAM data I/O 3
88	IVDD1	IVDD	I/O system power supply 1
89	RDT2	DIO	DRAM data I/O 2
90	RDT1	DIO	DRAM data I/O 1
91	RDT0	DIO	DRAM data I/O 0
92	NRAS	DO	DRAM RAS signal
93	NCAS	DO	DRAM CAS signal
94	NWE	DO	DRAM write enable signal
95	TS2	DI	Test mode control input 2
96	DVSS0	DVSS	Digital system ground 0
97	XO	DO	Crystal oscillator output
98	XI	DI	Crystal oscillator input
99	IVDD0	IVDD	I/O system power supply 0
100	TS1	DI	Test mode control input 1

Note) I/O column notation

DI: Digital input pin, DO: Digital output pin, DIO: Digital I/O pin, DSI: Digital I/O pin with Schmitt trigger circuit, DTO: Tristate digital output pin, AI: Analog input pin, AO: Analog output pin

■ Electrical Characteristics

1. Absolute Maximum Ratings at V_{SS} = AV_{SS} = 0 V

Item	Symbol	Rating	Unit
I/O digital system supply voltage	IV_{DD}	– 0.3 to +4.6	V
Internal digital system supply voltage	DV_{DD}	– 0.3 to +2.5	V
Analog system supply voltage	AV_{DD}	– 0.3 to +4.6	V
Digital input pin voltage	V_I	– 0.3 to IV_{DD}+0.3 (Maximum: 4.6)	V
Digital output pin voltage	V_O	– 0.3 to IV_{DD}+0.3 (Maximum: 4.6)	V
Analog input pin voltage	V_{IA}	– 0.3 to AV_{DD}+0.3 (Maximum: 4.6)	V
Analog output pin voltage	V_{OA}	– 0.3 to AV_{DD}+0.3 (Maximum: 4.6)	V
Output current (HL4 type pins)	I_O	±12	mA
Output current (HL8 type pins)	I_O	±24	mA
Power dissipation	P_D	700	mW
Operating temperature	T_{opr}	–10 to +70	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note) 1. The absolute maximum ratings are limit values for stresses applied to the chip so that the chip will not be destroyed. Operation is not guaranteed within these ranges.

2. All of the IV_{DD}, DV_{DD}, AV_{DD}, V_{SS}, and AV_{SS} pins must be connected externally and the corresponding power or ground level supplied.

3. Insert bypass capacitors between the IV_{DD} and V_{SS} pins, the DV_{DD} and V_{SS} pins, and the AV_{DD} and V_{SS} pins.

4. Connect the TS0 to TS3 pins to V_{SS}.

5. IV_{DD} pins: IVDD0, IVDD1 DV_{DD} pins: DVDD0, DVV1, DVDD2
   AV_{DD} pins: AVDD0, AVDD1, ADACVDD V_{SS} pins: DVSS0, DVSS1, DVSS2
   AV_{SS} pins: AVSS0, AVSS1, ADACVSS
   Analog input pins: PEAK, BTOM, OSC, MON3T, VREFI, FF2, FF1, DD, CC, BB, AA, PEFMS, EFMIREF, ADIP
   Analog output pins: ADACL, ADACR, PEMF1, EFMFIL, EFMPLLF
   HL4 type pins: APCD, RFSWPG, RFSWHL, CLV2, REFM, SPDM, SPDP, FODM, FODP, TRDM, TRDP, LDON, TVDM, TVDP, SBCK, NREC, SDAP, SWS, SCL, TX, SGSYNC, MIDSY, SCTSY, SSDR, MONI1, MONI2, MONI3, MONI0, NWE
   HL8 type pins: FS384, RAD11 to RAD0, RDT3 to RDT0, NRAS, NCAS

2. Recommended Operating Conditions at V_{SS} = AV_{SS} = 0 V

Item	Symbol	Condition	Min	Typ	Max	Unit
1) During normal speed operation						
I/O digital system supply voltage	IV_{DD}		2.1	3.3	3.6	V
Internal digital system supply voltage	DV_{DD}		1.30	1.8	1.95	V
Analog system supply voltage	AV_{DD}		2.1	3.3	3.6	V
Ambient temperature	T_a		–10	—	70	°C
Oscillator frequency	f_{osc}	Xtal : 16.9344 MHz	—	16.9344	—	MHz

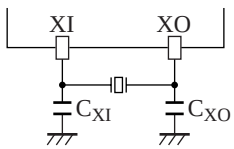


Figure 1. Oscillator circuit example

Note) Appropriate values of these circuit constants depend on the type of the oscillator element used. Consult the manufacturer of the oscillator element to determine appropriate values for the element used.

■ Electrical Characteristics (continued)

2. Recommended Operating Conditions (continued) at V_{SS} = AV_{SS} = 0 V

Item	Symbol	Condition	Min	Typ	Max	Unit
2) During high speed operation (2× to 4× ATRAC, 2× to 4× ATRAC3)						
I/O digital system supply voltage	IV_{DD}		3.0	3.3	3.6	V
Internal digital system supply voltage	DV_{DD}		1.65	1.8	1.95	V
Analog system supply voltage	AV_{DD}		3.0	3.3	3.6	V
Ambient temperature	T_a		–10	—	70	°C
Oscillator frequency	f_{osc}	Xtal : 16.9344 MHz	—	16.9344	—	MHz

Note) This IC cannot be used in self-oscillation mode at 33.8688 MHz (768Fs). For that frequency, input a clock signal directly to the XI pin.

3. DC Characteristics at IV_{DD} = 2.1 V to 3.6 V, AV_{DD} = 2.1 V to 3.6 V, DV_{DD} = 1.30 V to 1.95 V, V_{SS} = AV_{SS} = 0 V, T_a = -10°C to 70°C

Item		Symbol	Condition	Min	Typ	Max	Unit
Supply current (normal speed)	DV_{DD} supply	I_{DD}	IV_{DD} = AV_{DD} = 3.3 V	—	20	40	mA
	IV_{DD} supply	I_{DDI}	DV_{DD} = 1.80 V	—	6	12	
	AV_{DD} supply	I_{DDA}	VI = IV_{DD} or V_{SS} f = 16.9344 MHz, no load	—	6.5	13	
Supply current (standby mode)	DV_{DD} supply	I_{DD}	VI = IV_{DD} or V_{SS}	—	—	8	mA
	IV_{DD} supply	I_{DDI}	No load, with the clock stopped	—	—	3.5	
	AV_{DD} supply	I_{DDA}	DV_{DD} = 1.5 V	—	—	1	
1) Oscillator circuit: XI, XO							
High-level input voltage		V_{IH}		IV_{DD} × 0.8	—	IV_{DD}	V
Low-level input voltage		V_{IL}		0	—	IV_{DD} × 0.2	V
Internal feedback resistor		R_{FB}	IV_{DD} = 3.3 V	0.33	1	3	MΩ
2) CMOS input level pins: TS0, TS1, RX1, RX2, SDAR, LRCK, BCK, DATA, DRVSEL, NCLDCK, BLKCK, SUBC							
High-level input voltage		V_{IH}		IV_{DD} × 0.8	—	IV_{DD}	V
Low-level input voltage		V_{IL}		0	—	IV_{DD} × 0.2	V
Input leakage current		I_{LI}		—	—	±10	µA
3) CMOS input level pins with built-in pull-down resistors: TS2							
High-level input voltage		V_{IH}		IV_{DD} × 0.8	—	IV_{DD}	V
Low-level input voltage		V_{IL}		0	—	IV_{DD} × 0.2	V
Pull-down resistor		R_{IL}	V_I = IV_{DD}	8	30	100	kΩ
Input leakage current		I_{LI}	V_I = V_{SS}	—	—	±10	µA

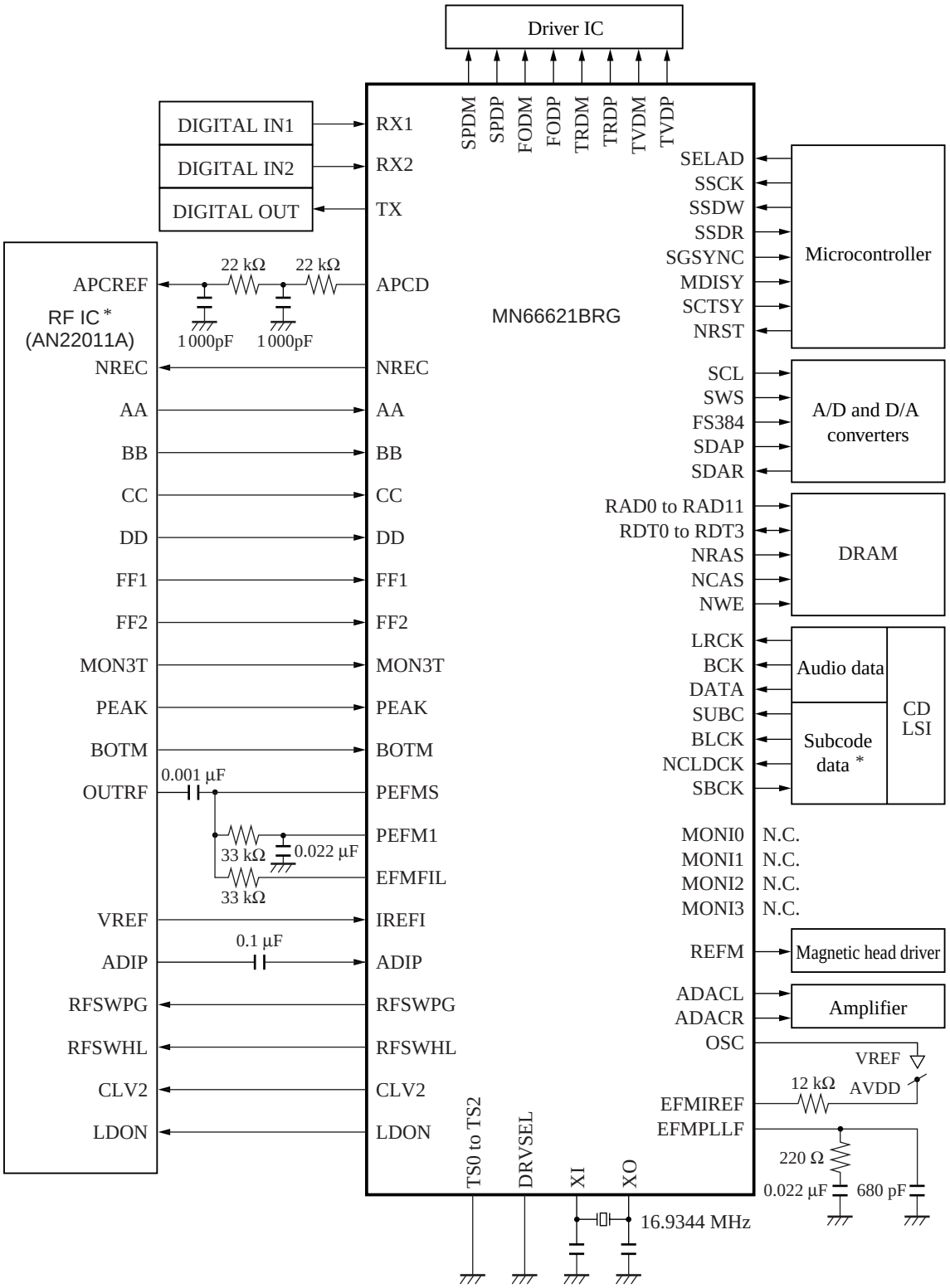
■ Electrical Characteristics (continued)

3. DC Characteristics (continued)

IV_{DD} = 2.1 V to 3.6 V, AV_{DD} = 2.1 V to 3.6 V, DV_{DD} = 1.30 V to 1.95 V, V_{SS} = AV_{SS} = 0 V, T_a = −10°C to 70°C

Item	Symbol	Condition	Min	Typ	Max	Unit
4) CMOS input level pins with built-in Schmitt trigger circuit: NRST, SSCK, SSDW, SELAD						
High-level input voltage	V_{IH}		IV_{DD} × 0.8	—	IV_{DD}	V
Low-level input voltage	V_{IL}		0	—	IV_{DD} × 0.2	V
Input leakage current	I_{LI}	$V_I = IV_{DD}$ or V_{SS}	—	—	±10	µA
5) Push-pull outputs - HL4 type: APCD, RFSWPG, RFSWHL, CLV2, LDON, SBCK, NREC, SDAP, SWS, SCL, TX, SGSYNC, MDISY, SCTSY, SSDR, MONI1, MONI2, MONI3, MONI0, NWE						
High-level output voltage	V_{OH}	I_{OH} = −2.0 mA $V_I = IV_{DD}$ or V_{SS}	IV_{DD} − 0.5	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 2.0 mA $V_I = IV_{DD}$ or V_{SS}	—	—	0.5	V
6) Push-pull outputs - HL4 type: FS384, RAD11 to RAD0, NRAS, NCAS						
High-level output voltage	V_{OH}	I_{OH} = −4.0 mA $V_I = IV_{DD}$ or V_{SS}	IV_{DD} − 0.5	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 4.0 mA $V_I = IV_{DD}$ or V_{SS}	—	—	0.5	V
7) CMOS level I/O pins - HL8 type: RDT3 to RDT0						
High-level input voltage	V_{IH}		IV_{DD} × 0.8	—	IV_{DD}	V
Low-level input voltage	V_{IL}		0	—	IV_{DD} × 0.2	V
High-level output voltage	V_{OH}	I_{OH} = −4.0 mA $V_I = IV_{DD}$ or V_{SS}	IV_{DD} − 0.5	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 4.0 mA $V_I = IV_{DD}$ or V_{SS}	—	—	0.5	V
Output leakage current	O_{LI}	$V_I = IV_{DD}$ or V_{SS}	—	—	±10	µA
8) Push-pull tristate outputs - HL4 type: TVDP, TRDT, FODP, SPDP, REFM, TVDM, TRDM, FODM, SPDM						
High-level output voltage	V_{OH}	I_{OH} = −2.0 mA $V_I = IV_{DD}$ or V_{SS}	IV_{DD} − 0.5	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 2.0 mA $V_I = IV_{DD}$ or V_{SS}	—	—	0.5	V
Output leakage current	O_{LI}	$V_I = IV_{DD}$ or V_{SS}	—	—	±10	µA

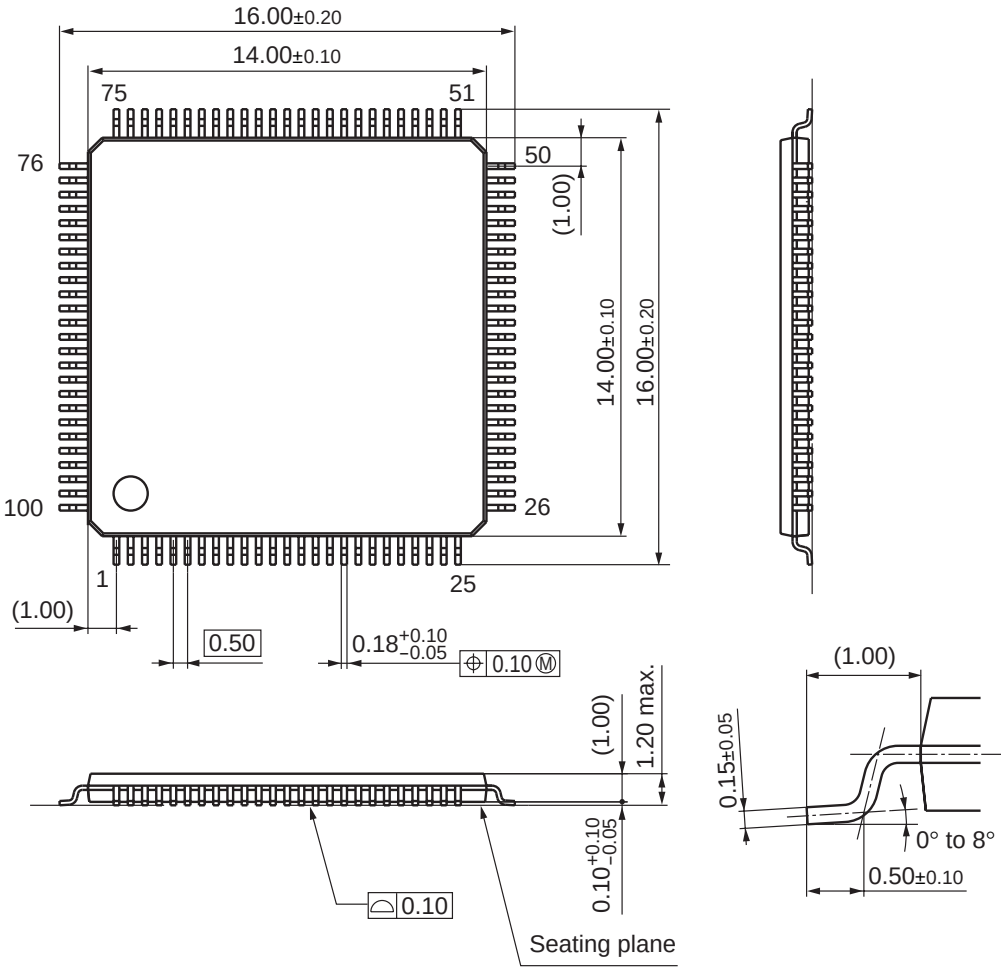
■ Application Circuit Example



Note) ∗: This device assumes the use of Panasonic AN22011A as RF IC, and Panasonic MN662790 (or similar products) as subcode interface.

■ Package Dimensions (Unit: mm)

• TQFP100-P 1414E (Lead-free package)



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