MN66710

Full-Function DAB Receiver LSI

■ Overview

The MN66710 is a single-chip digital signal processing LSI for a DAB (digital audio broadcast) receiver, including OFDM demodulation, service selection, error correction, and MPEG audio decoding. The MN66710 conforms to the European DAB standard (ETS 300 401). Since the MN66710 includes an on-chip A/D converter for the IF signal input, it can be directly input the 3.072 MHz center frequency analog IF signal output from the DAB high-frequency circuit. A DAB receiver is implemented easily by combining MN66710 with a small number of additional components, in particular, 4M DRAMs for working memory, audio D/A converters, microcontrollers, and etc.

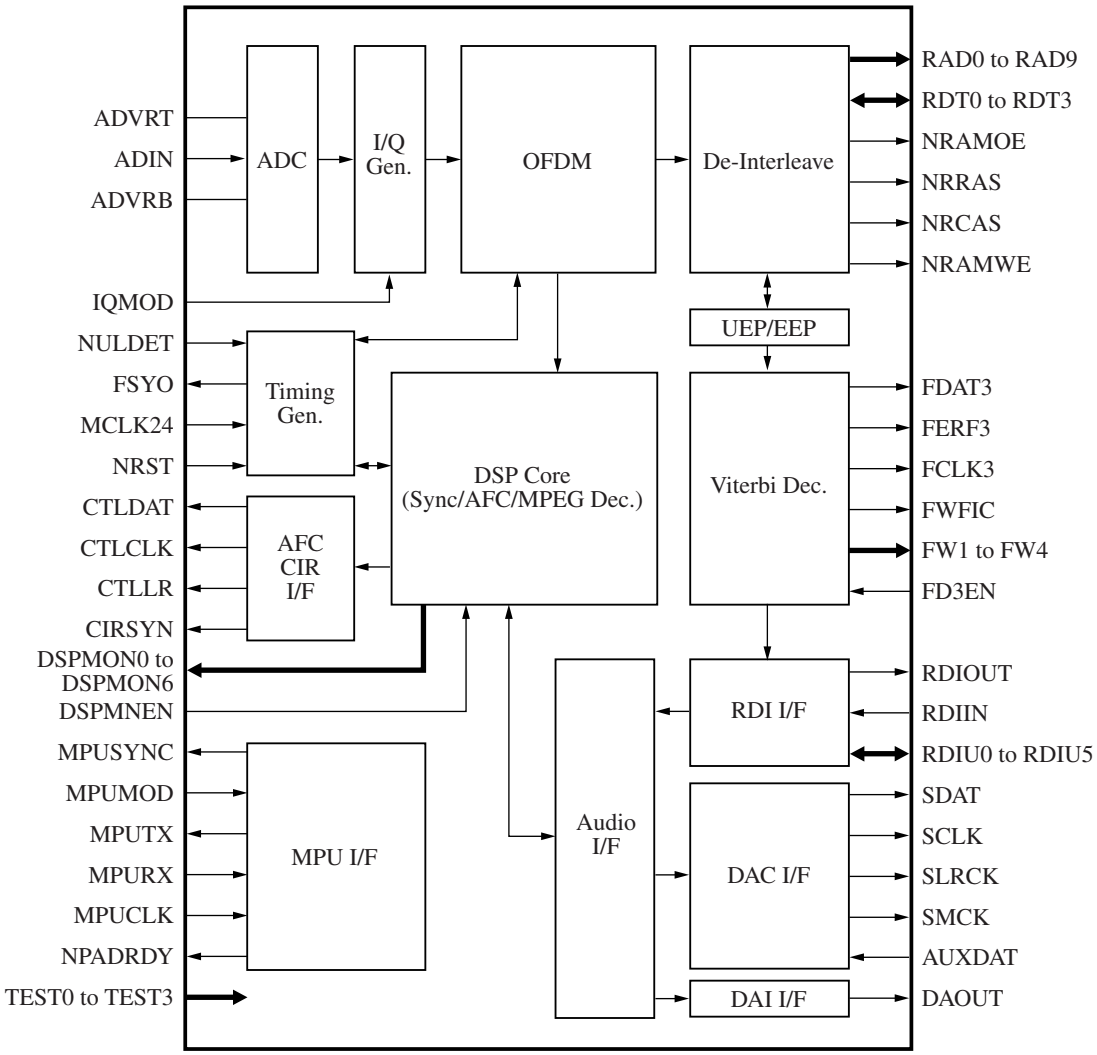
■ Features

- The DAB signal-processing block is integrated on a single chip. (with external 4M DRAMs)
- Supports all of DAB modes I, II, III, and IV.
- Achieves a processing data rate of up to 1.536 Mbps.
- Up to 4 MSC sub-channels can be selected.
- MPEG audio decoder (Also supports LSF.)
- Supports the standard audio D/A converter interface.
- Digital audio output unit conforming EIAJ CP-1201 (External driver required.)
- RDI output and dedicated audio RDI input units (For high capacity mode only.)
- F-PAD and X-PAD extraction function
- AIC support function provided in hardware.
- Supports multiplex restructuring with no interruption of the audio signal.
- TII decoding function (basic mode)
- Low supply voltage: 3.3 V±0.3 V
- Low power: Under 500 mW

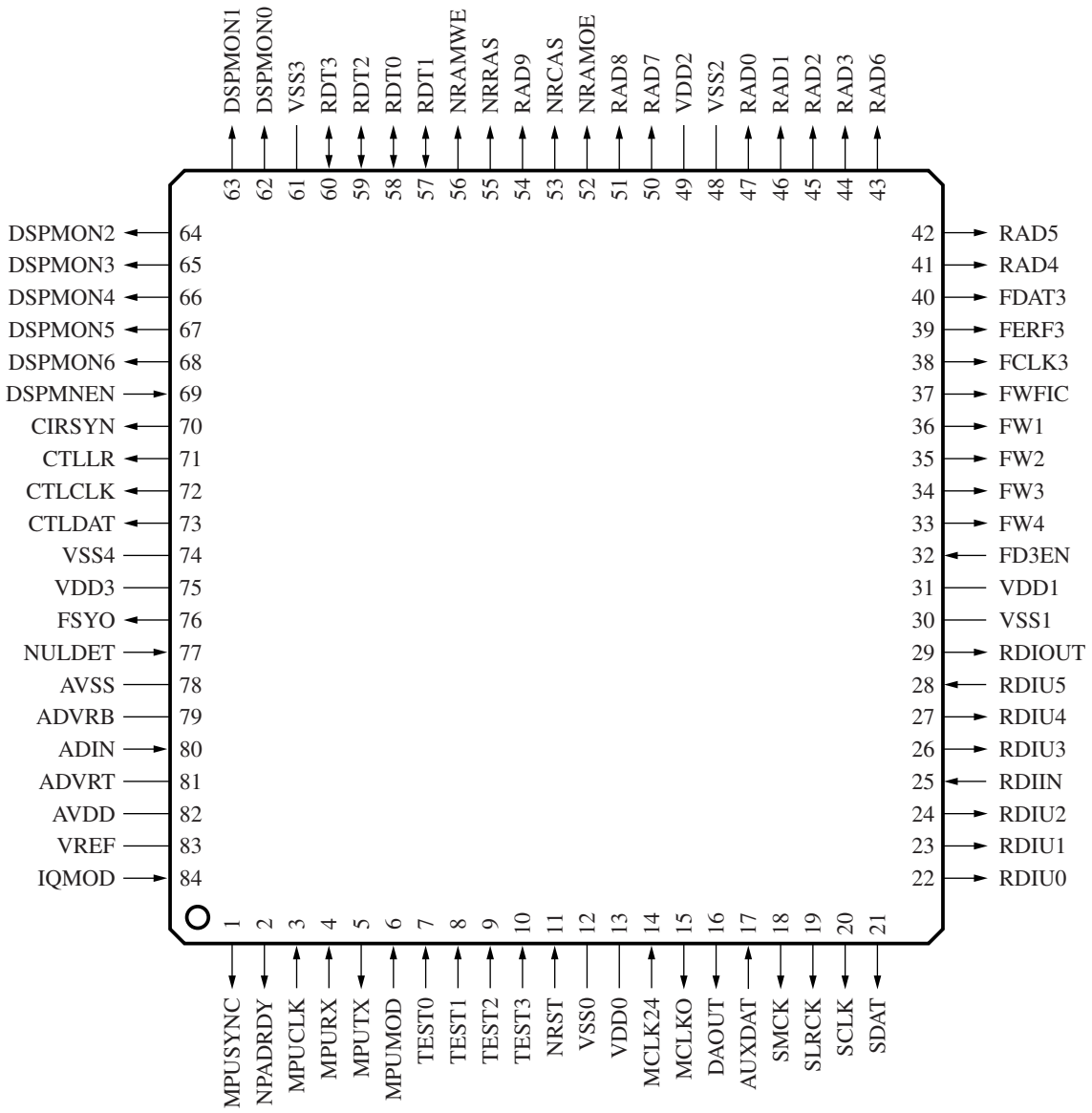
■ Applications

- DAB (digital audio broadcast) receivers

■ Block Diagram



■ Pin Arrangement



(TOP VIEW)

Note) Do not leave any of the VDD and VSS pins open.
Connect the TEST0 to TEST3 pin to VSS.

■ Pin Descriptions

Pin No.	Pin Name	I/O	Descriptions	Note
1	MPUSYNC	O	Microcontroller operation reference signal	Timing signal with a 24 ms period
2	NPADRDY	O	PAD data ready signal	Indicates that the PAD register can be read
3	MPUCLK	I	Microcontroller interface data clock	
4	MPURX	I	Microcontroller interface reception data	
5	MPUTX	O	Microcontroller interface transmission data	
6	MPUMOD	I	Microcontroller interface mode	
7	TEST0	I	Test mode setup	Normally connect to V_{SS}
8	TEST1	I	Test mode setup	Normally connect to V_{SS}
9	TEST2	I	Test mode setup	Normally connect to V_{SS}
10	TEST3	I	Test mode setup	Normally connect to V_{SS}
11	NRST	I	Master reset input	The IC is reset when this input is set low
12	VSS0	—	Digital system ground	
13	VDD0	—	Digital system power supply	
14	MCLK24	I	Master clock input (24.576 MHz)	
15	MCLKO	O	Master clock oscillator circuit output	For use with a crystal oscillator element
16	DAOUT	O	SPDIF digital audio interface output	
17	AUXDAT	I	Audio A/D converter serial data input	Auxiliary input A/D converter connection
18	SMCK	O	Audio A/D and D/A converter master clock	Outputs a 256 fs clock
19	SLRCK	O	Audio A/D and D/A converter left/right clock	
20	SCLK	O	Audio A/D and D/A converter serial clock output	
21	SDAT	O	Audio D/A converter serial data output	Audio output D/A converter connection
22	RDIU0	O	Auxiliary outputs for RDI expansion	Normally left open
23	RDIU1	O	Auxiliary outputs for RDI expansion	Normally left open
24	RDIU2	O	Auxiliary outputs for RDI expansion	Normally left open
25	RDIIN	I	RDI input	RDI back channel (audio only)
26	RDIU3	O	Auxiliary outputs for RDI expansion	Normally left open
27	RDIU4	O	Auxiliary outputs for RDI expansion	Normally left open
28	RDIU5	I	Auxiliary inputs for RDI expansion	Normally connect to V_{SS}
29	RDIOUT	O	RDI output	For high capacity mode only
30	VSS1	—	Digital system ground	
31	VDD1	—	Digital system power supply	
32	FD3EN	I	General-purpose data output enable	Output enable for FDAT3, FERF3, and FCLK3
33	FW4	O	General-purpose output window 4	Window for sub-channel 4
34	FW3	O	General-purpose output window 3	Window for sub-channel 3
35	FW2	O	General-purpose output window 2	Window for sub-channel 2

■ Pin Descriptions (continued)

Pin No.	Pin Name	I/O	Descriptions	Note
36	FW1	O	General-purpose output window 1	Window for sub-channel 1 (audio)
37	FWFIC	O	General-purpose output window 0	FIC window
38	FCLK3	O	General-purpose data output clock	1.536 MHz continuous clock
39	FERF3	O	General-purpose data output error flag	Flag that indicates Viterbi-corrected bits
40	FDAT3	O	General-purpose data output data	
41	RAD4	O	External DRAM address, bit 4	For connecting external DRAM
42	RAD5	O	External DRAM address, bit 5	For connecting external DRAM
43	RAD6	O	External DRAM address, bit 6	For connecting external DRAM
44	RAD3	O	External DRAM address, bit 3	For connecting external DRAM
45	RAD2	O	External DRAM address, bit 2	For connecting external DRAM
46	RAD1	O	External DRAM address, bit 1	For connecting external DRAM
47	RAD0	O	External DRAM address, bit 0	For connecting external DRAM
48	VSS2	—	Digital system ground	
49	VDD2	—	Digital system power supply	
50	RAD7	O	External DRAM address, bit 7	For connecting external DRAM
51	RAD8	O	External DRAM address, bit 8	For connecting external DRAM
52	NRAMOE	O	External DRAM output enable	For connecting external DRAM
53	NRCAS	O	External DRAM column address strobe	For connecting external DRAM
54	RAD9	O	External DRAM address, bit 9	For connecting external DRAM
55	NRRAS	O	External DRAM row address strobe	For connecting external DRAM
56	NRAMWE	O	External DRAM write enable	For connecting external DRAM
57	RDT1	I/O	External DRAM data, bit 1	For connecting external DRAM
58	RDT0	I/O	External DRAM data, bit 0	For connecting external DRAM
59	RDT2	I/O	External DRAM data, bit 2	For connecting external DRAM
60	RDT3	I/O	External DRAM data, bit 3	For connecting external DRAM
61	VSS3	—	Digital system ground	
62	DSPMON0	O	DSP monitor, bit 0	Normally left open
63	DSPMON1	O	DSP monitor, bit 1	Normally left open
64	DSPMON2	O	DSP monitor, bit 2	Normally left open
65	DSPMON3	O	DSP monitor, bit 3	Normally left open
66	DSPMON4	O	DSP monitor, bit 4	Normally left open
67	DSPMON5	O	DSP monitor, bit 5	Normally left open
68	DSPMON6	O	DSP monitor, bit 6	Normally left open
69	DSPMNEN	I	DSP monitor output enable	A low level disables DSP monitor output
70	CIRSYN	O	CIR display cycle signal	CIR monitor display trigger signal
71	CTLLR	O	AFC/CIR D/A converter left/right clock	For AFC control and CIR monitor display
72	CTLCLK	O	AFC/CIR D/A converter clock	For AFC control and CIR monitor display

■ Pin Descriptions (continued)

Pin No.	Pin Name	I/O	Descriptions	Note
73	CTLDAT	O	AFC/CIR D/A converter data	For AFC control and CIR monitor display
74	VSS4	—	Digital system ground	
75	VDD3	—	Digital system power supply	
76	FSYO	O	Frame sync signal output	
77	NULDET	I	Null symbol detection signal input	
78	AVSS	—	Analog system ground	
79	ADVRB	—	A/D converter low side reference voltage	
80	ADIN	I	A/D converter analog input	
81	ADVRT	—	A/D converter high side reference voltage	
82	AVDD	—	Analog system power supply	
83	VREF	—	Reference supply for 5 V input pads	
84	IQMOD	I	Digital IQ generation switching input	Normally connect to V_{DD}

■ Electrical Characteristics

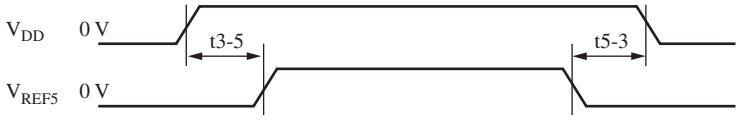
1. Absolute Maximum Ratings at T_a = 25°C, V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage (digital)	V_{DD}	– 0.3 to +4.6	V
Supply voltage (analog)	AV_{DD}	– 0.3 to +4.6	V
5 V reference voltage *1	V_{REF5}	– 0.3 to +5.7	V
Input pin voltage (except for the type A and type B)	V_I	– 0.3 to V_{DD}+0.3	V
Input pin voltage (type A)	V_{I5}	– 0.3 to +6.0 *2	V
Input pin voltage (type B)	V_{I5}	– 0.3 to V_{REF5}+0.3 *2	V
Output pin voltage (except for the type B)	V_O	– 0.3 to V_{DD}+0.3	V
Output pin voltage (type B)	V_{O5}	– 0.3 to V_{REF5}+0.3 *2	V
Output current (type HL1)	I_O	±3	mA
Output current (type HL2)	I_O	±6	mA
Output current (type HL4)	I_O	±12	mA
Output current (type HL8)	I_O	±24	mA
Power dissipation	P_D	1030	mW
Storage temperature	T_{stg}	–55 to +125	°C

■ Electrical Characteristics (continued)

1. Absolute Maximum Ratings at T_a = 25°C, V_{SS} = 0 V (continued)

Note) 1. *1 : The power supply rise and fall sequences must meet the stipulations shown below.



The times t3-5 and t5-3 must be non-negative.

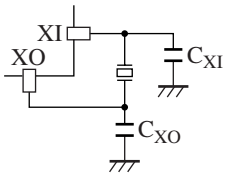
V_{DD} and V_{REF5} should change smoothly.

*2 : If $V_{DD} \leq 1.4$ V: – 0.3 V to +4.6 V

2. Type A pins : RDIU5, MPURX, RDIIN, MPUCLK, MPUMOD, NULDET
   Type B pins : RAD9, RDT0 to RDT3, FSYO, CTLLR, DAOUT, NRCAS, NRRAS, CIRSYN, CTLCLK, CTLDAT, DSPMON0 to DSPMON6, NRAMOE, NRAMWE, DSPMNEN
   Type HL1 pins : FW1 to FW4, FCLK3, FDAT3, FERF3, FWFIC, DSPMON0 to DSPMON6, DSPMNEN
   Type HL2 pins : RDIU0 to RDIU4
   Type HL4 pins : FSYO, SCLK, SDAT, SMCK, CTLLR, DAOUT, MPUTX, SLRCK, AUXDAT, CIRSYN, CTLCLK, CTLDAT, RDIOUT, MPUSYNC, NPADRDY
   Type HL8 pins : RAD0 to RAD9, RDT0 to RDT3, NRCAS, NRRAS, NRAMOE, NRAMWE
3. The absolute maximum ratings are limiting values under which the chip will not be destroyed. Operation is not guaranteed within these ranges.
4. External power and ground levels must be connected directly to all of the VDD and VSS pins respectively.
5. Connect the MINTEST pin to ground.
6. When used in car audio equipment, insert bypass capacitors (recommended value: 0.1 µF) between VDD and VSS.

2. Recommended Operating Conditions at V_{SS} = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage (digital)	V_{DD}		3.0	3.3	3.6	V
Supply voltage (analog)	AV_{DD}		3.0	3.3	3.6	V
5 V reference voltage	V_{REF5}		4.75	5.0	5.25	V
Ambient temperature	T_a		–30	—	85	°C
Input rise time	t_r		0	—	100	ns
Input fall time	t_f		0	—	100	ns
Oscillator frequency	$f_{OSC}1$	24.576 MHz Xtal	—	24.576	—	MHz
Recommended external capacitor value	$C_{XI}7$	V_{DD} = 3.3 V	—	47	—	pF
	$C_{XO}7$	Built-in feedback resistor	—	47	—	pF



Note) 1. Since the oscillator characteristics depend on the oscillator element itself, external capacitances, and other factors, consult the manufacturer of the oscillator element to determine the circuit constants.
2. Apply 5 V to 5 V reference voltage if 5 V inputs are used. This has no steady-state current consumption.
   Do not apply the 5 V if the 3.3 V is not being applied to the LSI.
   3.3 V may be supplied to this pin if only a single 3.3 V power supply is used.

■ Electrical Characteristics (continued)

3. DC Characteristics at V_{DD} = 3.0 V to 3.6 V, V_{REF5} = 4.75 V to 5.25 V, V_{SS} = 0.00 V, f_{TEST} = 24.576 MHz, T_a = −30°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating supply current	I_{DDO}	$V_I = V_{DD}$ or V_{SS} f = 24.576 MHz V_{DD} = 3.3 V, outputs open	—	110	200	mA
Oscillator circuit: MCLK24, MCLKO						
High-level input voltage	V_{IH}		$V_{DD} \times 0.8$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.2$	V
Internal feedback resistor	R_f7	$V_I = V_{DD}$ or V_{SS} V_{DD} = 3.3 V	313	940	2820	kΩ
CMOS level input pins: FD3EN, TEST0, TEST1, TEST2, IQMOD						
High-level input voltage	V_{IH}		$V_{DD} \times 0.8$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.2$	V
Input leakage current	I_{LI}	$V_I = V_{DD}$ or V_{SS}	—	—	±5	µA
CMOS level input pin with Schmitt trigger circuit: NRST						
Input threshold voltage	VT+	V_{DD} = 3.0 V to 3.6 V	—	1.85	$V_{DD} \times 0.8$	V
	VT−		$V_{DD} \times 0.2$	1.45	—	
Input leakage current	I_{LI}	$V_I = V_{DD}$ or V_{SS}	—	—	±5	µA
CMOS level input pin with built-in pull-down resistor: TEST3						
High-level input voltage	V_{IH}		$V_{DD} \times 0.85$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.15$	V
Pull-down resistor	R_{IL}	$V_I = V_{DD}$	10	30	90	kΩ
Input leakage current	I_{LI}	$V_I = V_{SS}$	—	—	±10	µA
TTL level input pins: RDIU5, MPURX, RDIIN, MPUCLK, MPUMOD, NULDET						
High-level input voltage	V_{IH}		2.2	—	5.25	V
Low-level input voltage	V_{IL}		0	—	0.6	V
Input leakage current	I_{LI}	V_I = 5.25 V or V_{SS}	—	—	±10	µA
Push-pull output pins: FW1 to FW4, FCLK3, FDAT3, FERF3, FWFIC						
High-level output voltage	V_{OH}	I_{OH} = −1.0 mA $V_I = V_{DD}$ or V_{SS}	$V_{DD} - 0.5$	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 1.0 mA $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V
Push-pull output pins: MPUTX, MPUSYNC, NPADRDY						
High-level output voltage	V_{OH}	I_{OH} = −4.0 mA $V_I = V_{DD}$ or V_{SS}	$V_{DD} - 0.5$	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 4.0 mA $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V

■ Electrical Characteristics (continued)

3. DC Characteristics at V_{DD} = 3.0 V to 3.6 V, V_{REF5} = 4.75 V to 5.25 V, V_{SS} = 0.00 V, f_{TEST} = 24.576 MHz, T_a = −30°C to +85°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Push-pull output pins: RAD0 to RAD8						
High-level output voltage	V_{OH}	I_{OH} = −8.0 mA $V_I = V_{DD}$ or V_{SS}	V_{DD} − 0.5	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 8.0 mA $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V
CMOS level I/O pins: RDIU0 to RDIU4						
High-level input voltage	V_{IH}		$V_{DD} \times 0.8$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.2$	V
High-level output voltage	V_{OH}	I_{OH} = −2.0 mA $V_I = V_{DD}$ or V_{SS}	V_{DD} − 0.5	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 2.0 mA $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V
Output leakage current	I_{LO}	V_O = High-impedance state $V_I = V_{DD}$ or V_{SS} $V_O = V_{DD}$ or V_{SS}	—	—	±5	µA
CMOS level I/O pins: SCLK, SDAT, SMCK, SLRCK, AUXDAT, RDIOUT						
High-level input voltage	V_{IH}		$V_{DD} \times 0.8$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.2$	V
High-level output voltage	V_{OH}	I_{OH} = −4.0 mA $V_I = V_{DD}$ or V_{SS}	V_{DD} − 0.5	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 4.0 mA $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V
Output leakage current	I_{LO}	V_O = High-impedance state $V_I = V_{DD}$ or V_{SS} $V_O = V_{DD}$ or V_{SS}	—	—	±5	µA
TTL level I/O pins: DSPMON0 to DSPMON6, DSPMNEN						
High-level input voltage	V_{IH}		2.2	—	V_{REF5}	V
Low-level input voltage	V_{IL}		0	—	0.6	V
High-level output voltage	V_{OH}	I_{OH} = −1.0 mA $V_I = V_{DD}$ or V_{SS}	2.4	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 1.0 mA $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V
Output leakage current	I_{LO}	V_O = High-impedance state V_I = 5.25 V or V_{SS} V_O = 5.25 V or V_{SS}	—	—	±10	µA

■ Electrical Characteristics (continued)

3. DC Characteristics at V_{DD} = 3.0 V to 3.6 V, V_{REF5} = 4.75 V to 5.25 V, V_{SS} = 0.00 V, f_{TEST} = 24.576 MHz, T_a = −30°C to +85°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TTL level I/O pins: FSYO, CTLLR, DAOUT, CIRSYN, CTLCLK, CTLDAT						
High-level input voltage	V_{IH}		2.2	—	V_{REF5}	V
Low-level input voltage	V_{IL}		0	—	0.6	V
High-level output voltage	V_{OH}	I_{OH} = −4.0 mA $V_I = V_{DD}$ or V_{SS}	2.4	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 4.0 mA $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V
Output leakage current	I_{LO}	V_O = High-impedance state V_I = 5.25 V or V_{SS} V_O = 5.25 V or V_{SS}	—	—	±10	µA
TTL level I/O pins: RAD9, RDT0 to RDT3, NRCAS, NRRAS, NRAMOE, NRAMWE						
High-level input voltage	V_{IH}		2.2	—	V_{REF5}	V
Low-level input voltage	V_{IL}		0	—	0.6	V
High-level output voltage	V_{OH}	I_{OH} = −8.0 mA $V_I = V_{DD}$ or V_{SS}	2.4	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 8.0 mA $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V
Output leakage current	I_{LO}	V_O = High-impedance state V_I = 5.25 V or V_{SS} V_O = 5.25 V or V_{SS}	—	—	±10	µA

4. AC Characteristics at V_{DD} = 3.0 V to 3.6 V, V_{REF5} = 4.75 V to 5.25 V, V_{SS} = 0.00 V, f_{TEST} = 24.576 MHz, T_a = −30°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Clock input						
MCLK24 clock period	t_{MCLK}	See figure 1.	36	40.69	45	ns
MCLK24 high-level period	t_{MCLKH}		18	—	—	ns
MCLK24 low-level period	t_{MCLKL}		15	—	—	ns
Microcontroller interface						
MPUCLK clock period	t_{MPUC}	See figure 2.	4 × T	—	—	ns
MPUCLK high-level period	t_{MPUCH}		72	—	—	ns
MPUCLK low-level period	t_{MPUCL}		60	—	—	ns

Note) The symbol T in the table refers to the MCLK24 period, t_{MCLK}.

■ Electrical Characteristics (continued)

4. AC Characteristics at V_{DD} = 3.0 V to 3.6 V, V_{REF5} = 4.75 V to 5.25 V, V_{SS} = 0.00 V, f_{TEST} = 24.576 MHz, T_a = −30°C to +85°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Microcontroller interface (continued)						
MPUMOD setup time	t_{MODS}	See figure 3,4.	0	—	—	ns
MPUMOD hold time	t_{MODH}		2 × T	—	—	ns
MPURX setup time	t_{RXS}		0	—	—	ns
MPURX hold time	t_{RXH}		2 × T	—	—	ns
MPUTX delay time	t_{TXD}		—	—	2 × T	ns
Write disabled period 1	t_{WRNG1}		6 × T	—	—	ns
Write disabled period 2	t_{WRNG2}		4 × T	8 × T	—	ns
Read disabled period	t_{RDNG}		4 × T	8 × T	—	ns
DRAM interface						
Random read/write cycle time	t_{RC}	See figure 5.	120	—	—	ns
RAS precharge time	t_{RP}		37.5	40	—	ns
RAS pulse width	t_{RAS}		75	80	—	ns
CAS pulse width	t_{CAS}		17.5	20	—	ns
Row address setup time	t_{ASR}		10	—	—	ns
Row address hold time	t_{RAH}		17.5	—	—	ns
Column address setup time	t_{ASC}		10	—	—	ns
Column address hold time	t_{CAH}		17.5	—	—	ns
RAS/CAS delay time	t_{RCD}		35	—	45	ns
RAS column address delay time	t_{RAD}		17.5	—	25	ns
RAS hold time	t_{RSH}		35	—	—	ns
CAS hold time	t_{CSH}		60	—	—	ns
CAS/RAS precharge time	t_{CRP}		37.5	40	—	ns
OE/data input delay time	t_{ODD}		20	—	—	ns
Write command setup time	t_{WCS}		40	—	—	ns
Write command hold time	t_{WCH}		15	—	—	ns
Data input setup time	t_{DS}		12.5	—	—	ns
Data input hold time	t_{DH}		17.5	—	—	ns
Fast page mode cycle time	t_{PC}		40	—	—	ns
Fast page mode precharge time	t_{CP}		15	17.5	—	ns

Note) The symbol T in the table refers to the MCLK24 period, t_{MCLK}.

■ Electrical Characteristics (continued)

4. AC Characteristics at V_{DD} = 3.0 V to 3.6 V, V_{REF5} = 4.75 V to 5.25 V, V_{SS} = 0.00 V, f_{TEST} = 24.576 MHz, T_a = −30°C to +85°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DRAM interface (continued)						
Master clock/RAS delay time	t_1	See figure 5.	7	—	32.5	ns
Master clock/CAS delay time	t_2		7	—	32.5	ns
Master clock/address delay time	t_3		27.5	—	57.5	ns
Master clock/WE delay time	t_4		7	—	32.5	ns
Master clock/data input delay time	t_5		27.5	—	57.5	ns
Master clock/OE delay time	t_6		7	—	30	ns
Data output setup time	t_7		0	—	—	ns
Data output hold time	t_8		20	—	—	ns
Audio interface						
SMCK clock period	t_{SMCK}	See figure 6.	72	81.38	—	ns
SMCK high-level period	t_{SMCKH}		31	—	—	ns
SMCK low-level period	t_{SMCKL}		31	—	—	ns
SCLK period	t_{SCLK}	See figure 7.	288	325.52	—	ns
SCLK high-level period	t_{SCLKH}		100	—	—	ns
SCLK low-level period	t_{SCLKL}		100	—	—	ns
SCLK delay time	t_{SCLKD}		—	—	41	ns
SDAT delay time	t_{SDATD}		—	—	40	ns
SLRCK delay time	t_{SLRD}		—	—	41	ns
AUXDAT setup time	t_{AUXS}		8.5	—	—	ns
General-purpose data outputs						
FCLK3 clock period	t_{FCLK}	See figure 8.	576	651.04	—	ns
FCLK3 high-level period	t_{FCLKH}		200	—	—	ns
FCLK3 low-level period	t_{FCLKL}		200	—	—	ns
FCLK3 delay time	t_{FCLKD}		—	—	15.5	ns
FDAT3 delay time	t_{FDATD}		—	—	21.5	ns
FERF3 delay time	t_{FERFD}		—	—	21	ns
FWFIC and FW1:4 delay time	t_{FWD}		—	—	18	ns

■ Electrical Characteristics (continued)

4. AC Characteristics at V_{DD} = 3.0 V to 3.6 V, V_{REF5} = 4.75 V to 5.25 V, V_{SS} = 0.00 V, f_{TEST} = 24.576 MHz, T_a = −30°C to +85°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CIR/AFC Output Timing						
CTLCLK clock period	t_{CCLK}	See figure 9.	576	651.04	—	ns
CTLCLK high-level period	t_{CCLKH}		200	—	—	ns
CTLCLK low-level period	t_{CCLKL}		200	—	—	ns
CIRSYN delay time	t_{CIRD}		—	—	241	ns
CTLCLK delay time	t_{CCLKD}		—	—	35	ns
CTLDAT delay time	t_{CDATD}		—	—	35	ns
CTLLR delay time	t_{CLRD}		—	—	37	ns

5. A/D Converter Characteristics at V_{DD} = 3.30 V, V_{REF5} = 5.00 V, V_{SS} = 0.00 V, T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution	RES		—	—	8	bit
Nonlinearity error	NLE1	f_{MSPCK} = 24.576 MHz V_{RT} = 2.6 V, V_{RB} = 0.6 V	—	±1.5	±2.0	LSB
Differential nonlinearity error	DNLE1	f_{MSPCK} = 24.576 MHz V_{RT} = 2.6 V, V_{RB} = 0.6 V	—	±0.5	±1.5	LSB

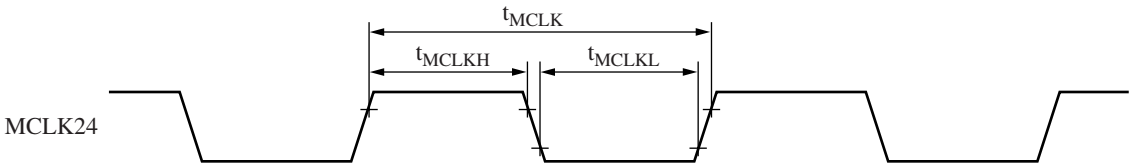


Figure 1. Clock input

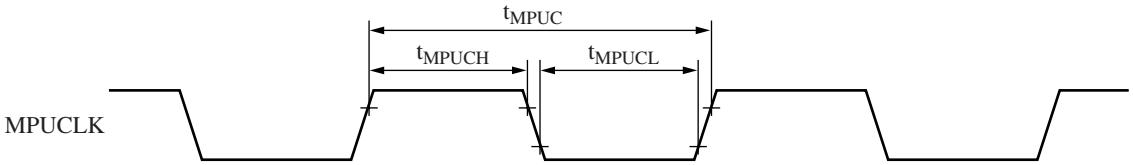


Figure 2. Microcontroller interface (data clock)

■ Electrical Characteristics (continued)

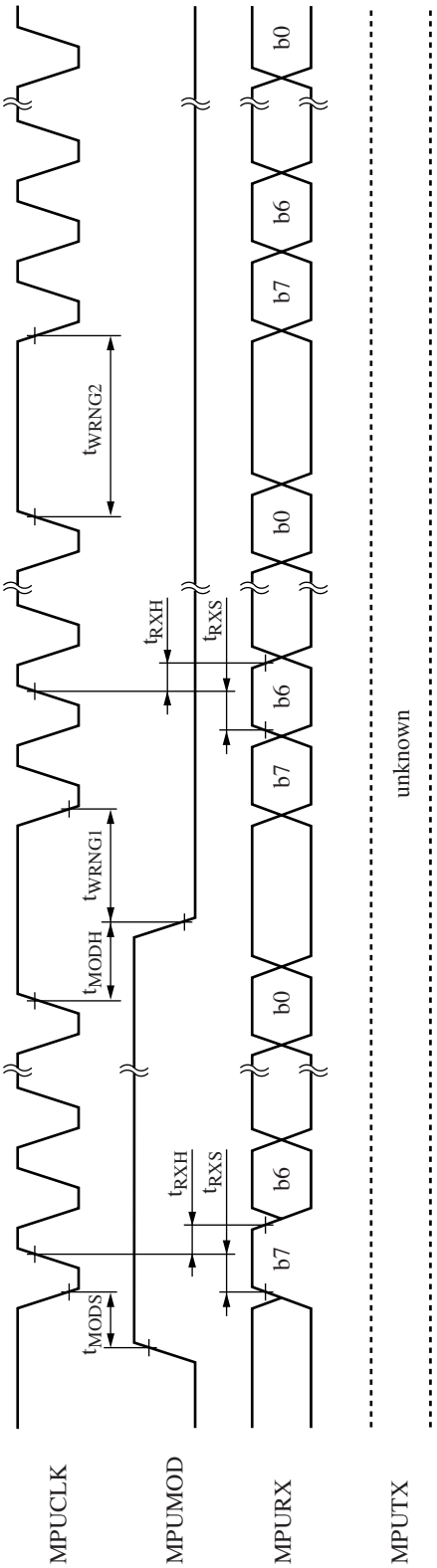


Figure 3. Microcontroller interface (data write time)

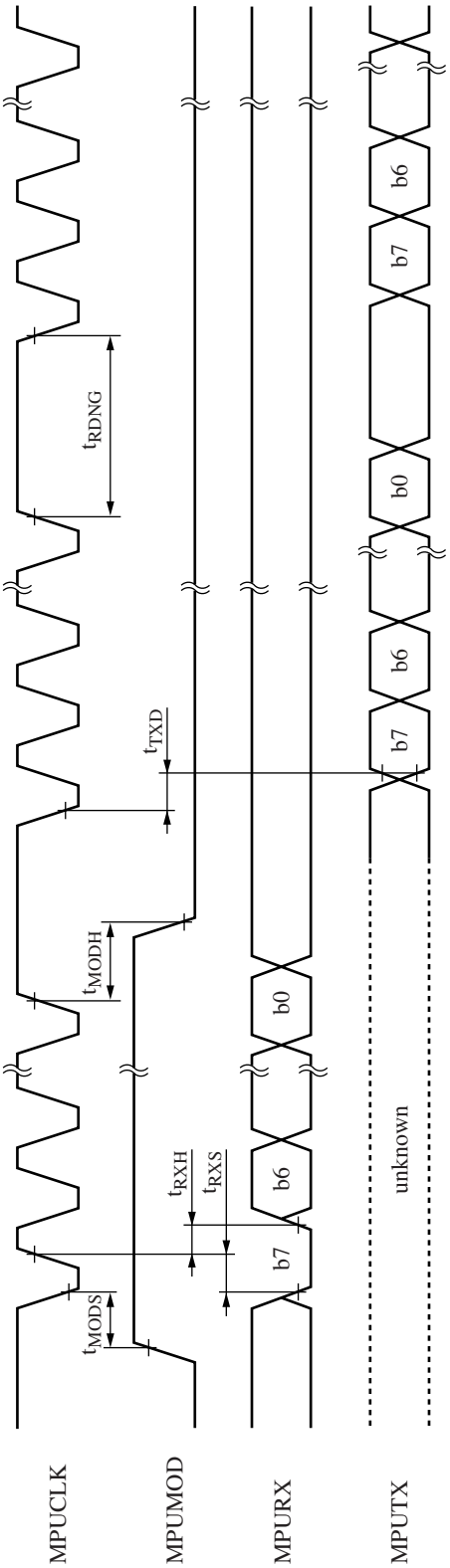


Figure 4. Microcontroller interface (data read time)

■ Electrical Characteristics (continued)

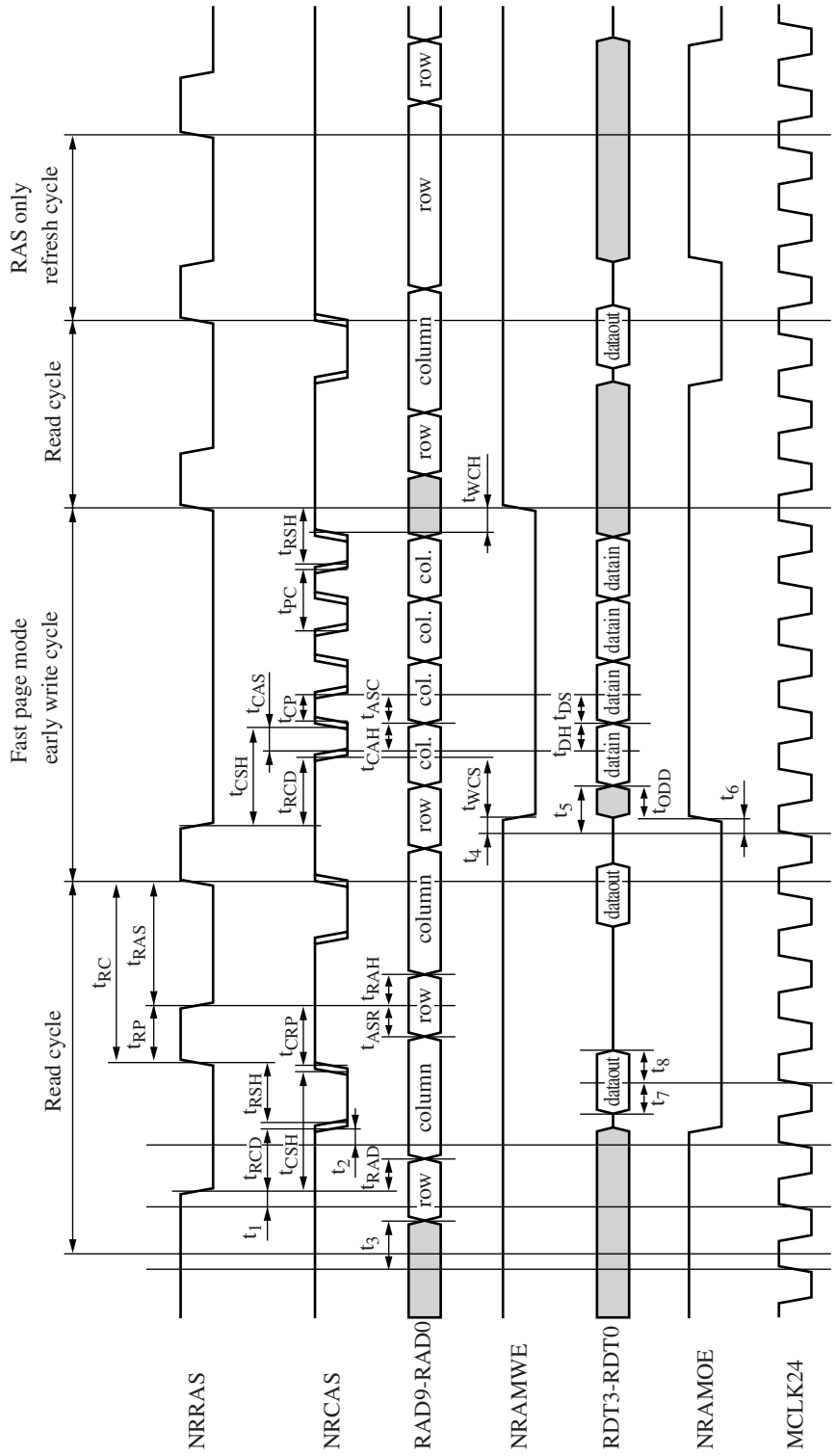


Figure 5. DRAM interface

■ Electrical Characteristics (continued)

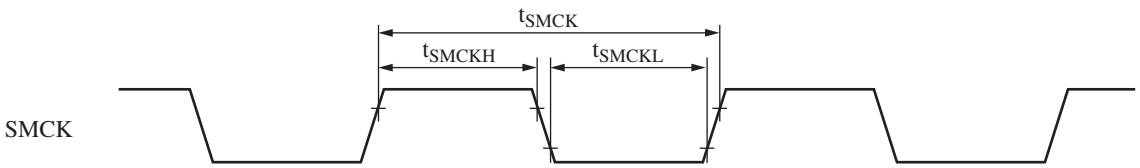


Figure 6. Audio interface

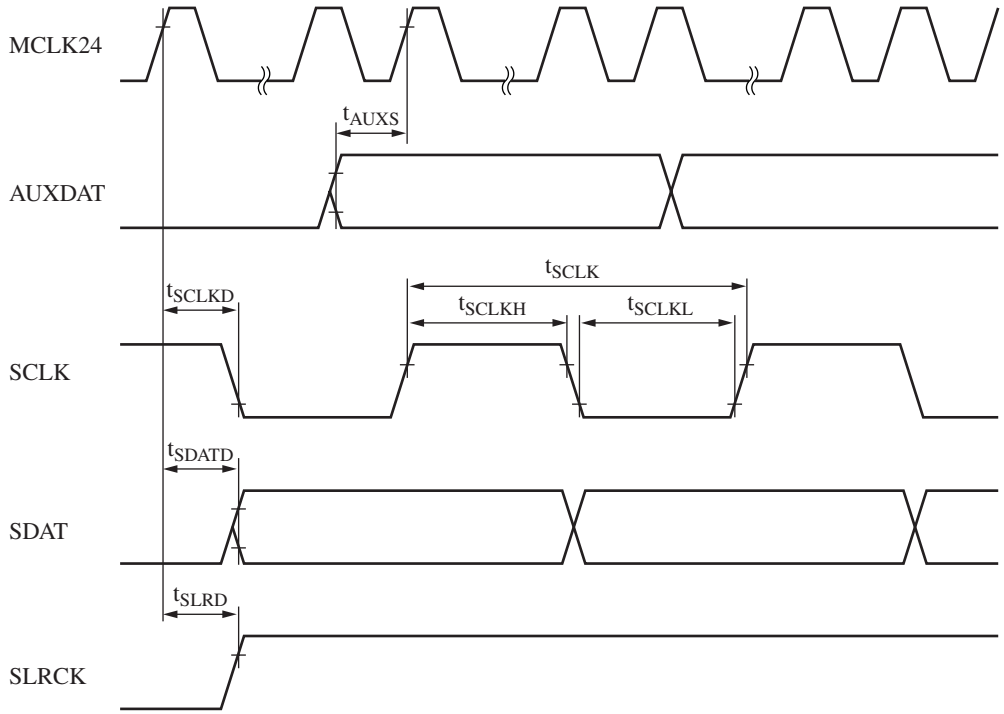


Figure 7. Audio output timing

■ Electrical Characteristics (continued)

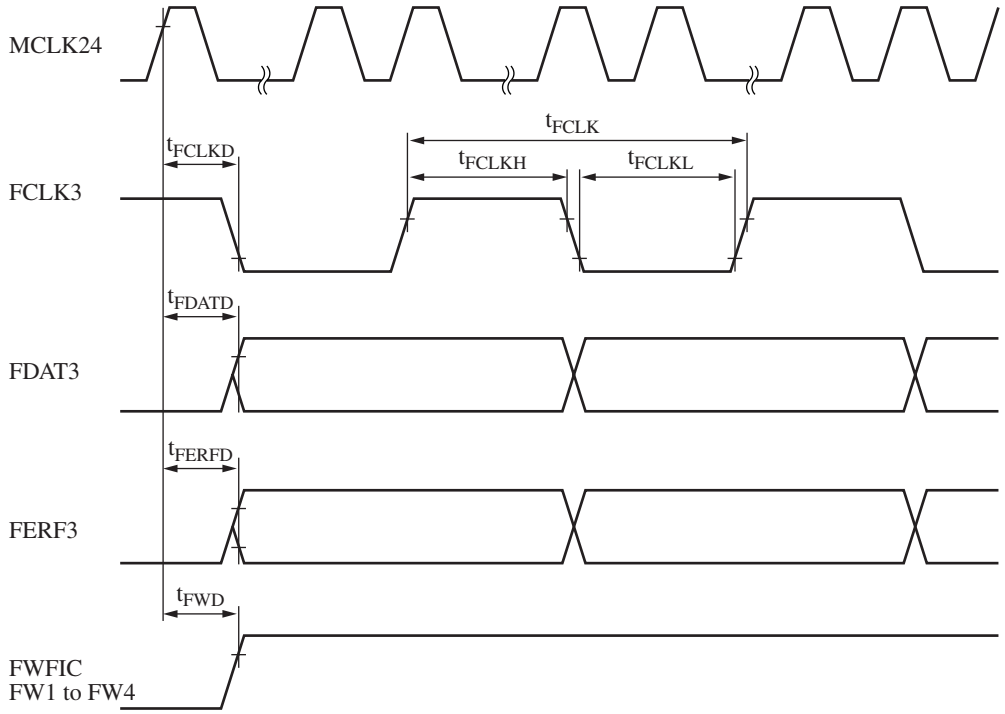


Figure 8. General-purpose data output

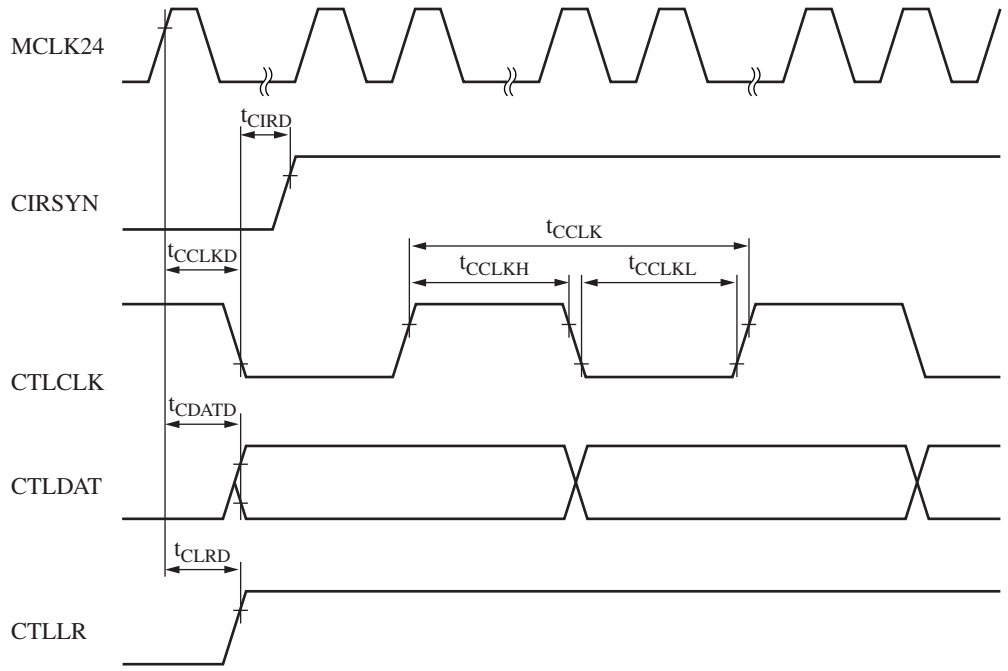
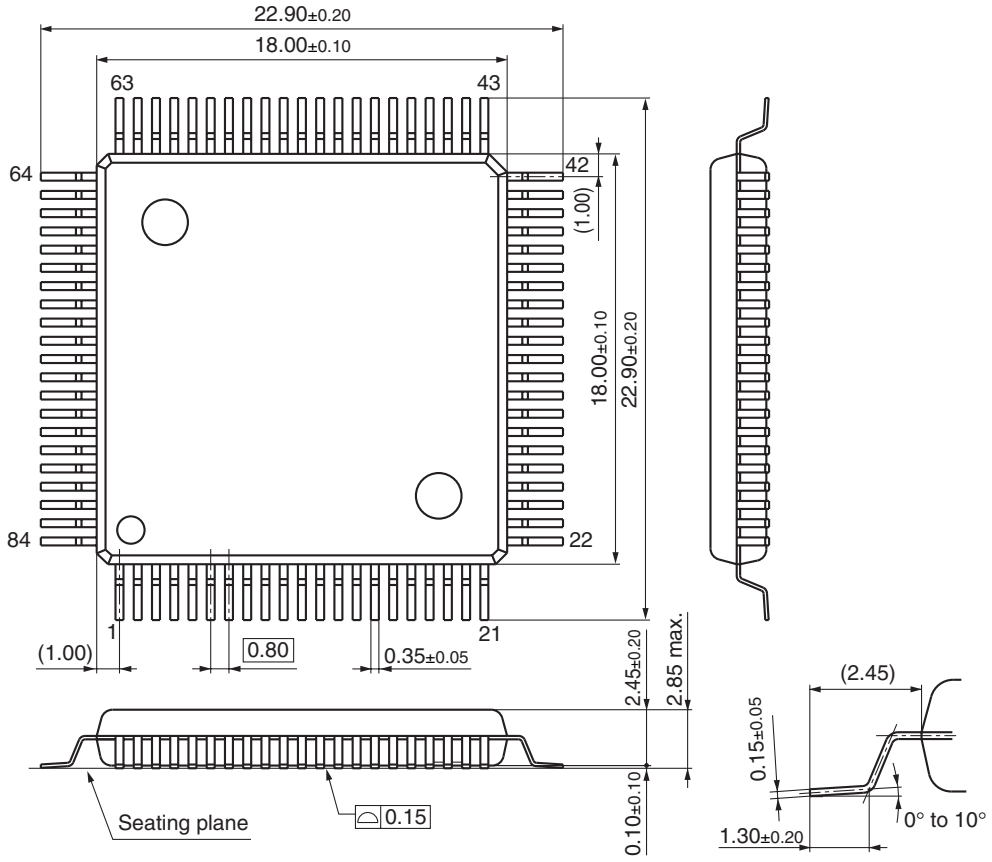


Figure 9. CIR/AFC output timing

■ Package Dimensions (Unit: mm)

• QFP084-P-1818E (Lead-free package)



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