National Semiconductor

MICROCIRCUIT DATA SHEET

MNLF412-X REV 0C1

Original Creation Date: 05/02/95
Last Update Date: 04/14/98
Last Major Revision Date: 05/02/95

LOW OFFSET, LOW DRIFT DUAL JFET INPUT OPERATIONAL AMPLIFIER

General Description

These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators,fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input Impedance, high slew rate and wide bandwidth.

Industry Part Number

LF412

NS Part Numbers

LF412MH/883 *
LF412MJ/883 **

Prime Die

LF412

Controlling Document

5962-9676001QGA*,QPA**

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Internally trimmed offset voltage. 1mV (max)
- Input offset voltage drift. 10uV/ C (max)
- Low input bias current. 50pA
- Low input noise current. 0.01 pA/Root Hz
- Wide gain bandwidth. 3MHz (min)
- High slew rate. 10V/uS (min)
- Low supply current. 1.8 mA/Amplifier
- High input impedance. 10E12 Ohms
- Low total harmonic distortion Av=10, RL=10K, ±0.02%
  Vo = 20 Vp-p, BW = 20 Hz - 20KHz
- Low 1/f noise corner. 50Hz
- Fast settling time to 0.01%. 2uS

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range (Note 3)	±15V
Output Short Circuit Duration (Note 4)	Continuous
Power Dissipation (Note 2)	
H Package (Note 3)	800mW
J Package	TBD
Tjmax	150 C
ThetaJA (Typical)	
METAL CAN	
(Still Air)	160 C/W
(500 LF/Min Air Flow)	83 C/W
CERDIP	
(Still Air)	122 C/W
(500 LF/Min Air Flow)	66 C/W
ThetaJC	
METAL CAN	38 C/W
CERDIP	15 C/W
Operating Temperature Range	-55 C ≤ TA ≤ 125 C
Storage Temperature Range	-65 C ≤ TA ≤ 150 C
Lead Temperature	
Soldering, (10 Sec.)	260 C
ESD Tolerance (Note 5)	1700V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 4: Any of the amplifier outputs can be shorted to ground indefintely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 5: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±15V, Vcm = 0, Rs = 0

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input offset Voltage	Rs = 10K Ohms			-3	3	mV	1
					-5	5	mV	2, 3
Delta Vio/ Delta T	Temperature Coefficient of Input Offset Voltage	Rs = 10K Ohms, 25 C ≤ TA ≤ 125 C	2		-20	20	uV/C	2
		Rs = 10K Ohms, -55 C ≤ TA ≤ 25 C	2		-20	20	uV/C	3
Iio	Input Offset Current		4		-.1	.1	nA	1
			4		-25	25	nA	2
Iib+	Input Bias Current		4			.2	nA	1
			4			50	nA	2
Iib-	Input Bias Current		4			.2	nA	1
			4			50	nA	2
CMRR	Common Mode Rejection Ratio	Rs ≤ 10K ohms, Vcm = ±11V			70		dB	1, 2, 3
+PSRR	Supply Voltage Rejection Ratio	6V ≤ +Vs ≤ 15V, -Vs = -15V			70		dB	1, 2, 3
-PSRR	Supply Voltage Rejection Ratio	+Vs = 15V, -15V ≤ -Vs ≤ -6V			70		dB	1, 2, 3
Is	Supply Current					6.5	mA	1, 2, 3
-Ios	Output Short Circuit Current				13	45	mA	1
					6	45	mA	2, 3
+Ios	Output Short Circuit Current				-45	-13	mA	1
					-45	-6	mA	2, 3
Avs+	Large Signal Voltage Gain	Vo = 0 to 10V, RL = 2K ohms	3		25		V/mV	4
			3		15		V/mV	5, 6
Avs-	Large Signal Voltage Gain	Vo = 0 to -10V, RL = 2K ohms	3		25		V/mV	4
			3		15		V/mV	5, 6
Vo+	Output Voltage Swing	RL = 10K Ohms, +Vin = 11V, -Vin = -11V			12		V	4, 5, 6
Vo-	Output Voltage Swing	RL = 10K Ohms, +Vin = -11V, -Vin = 11V				-12	V	4, 5, 6
Vcm	Input Common Mode Voltage Range		1		±11		V	

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VS = ±15V, VCM = 0, RS = 0

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
SR+	Slew Rate	Vout = -5V to 5V			8		V/us	7
SR-	Slew Rate	Vout = 5V to -5V			8		V/us	7
GBW	Gain Bandwidth Product				2.7		MHz	7

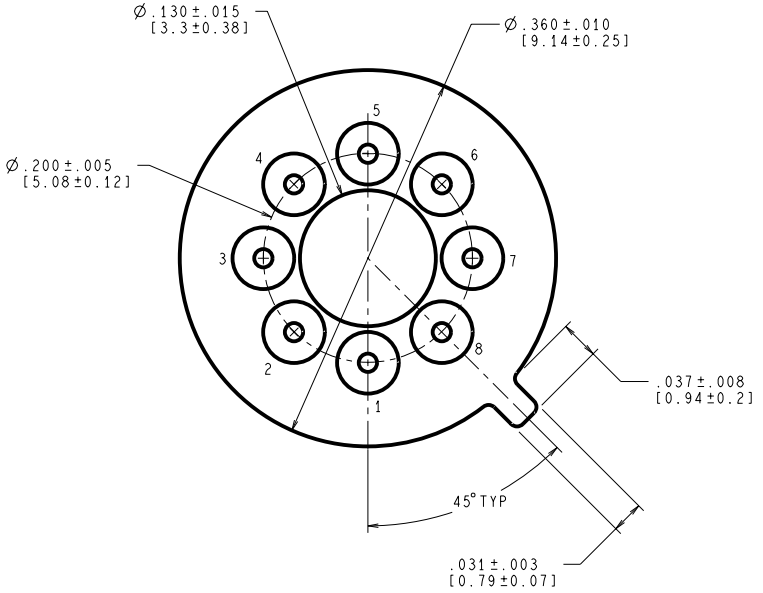
Note 1: Guaranteed by CMRR.
Note 2: Guaranteed parameter, not tested.
Note 3: Datalog reading in K = V/mV.
Note 4: RS = 10K Ohms at +125 C.

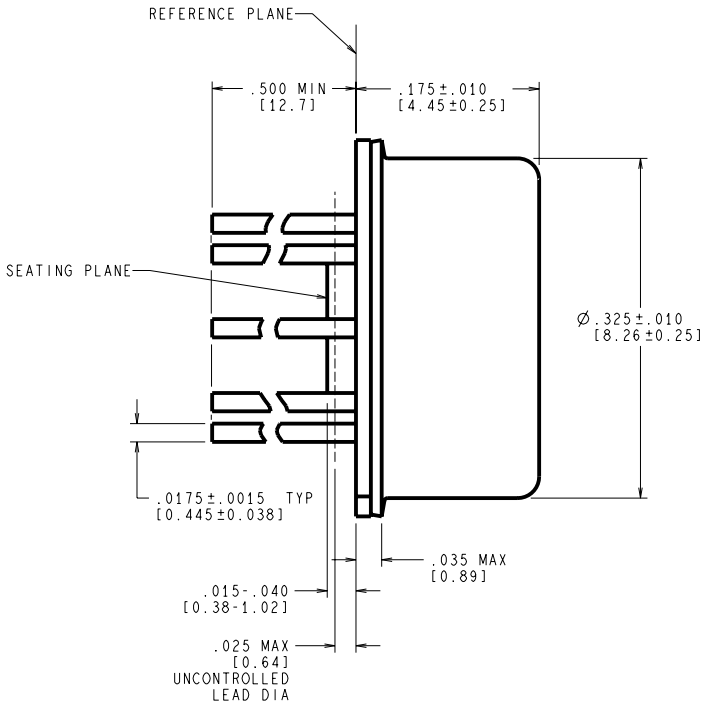
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05487HRA3	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (B/I CKT)
06116HRA2	CERDIP (J), 8 LEAD (B/I CKT)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000176A	METAL CAN (H), 8 LEAD (PINOUT)
P000177A	CERDIP (J), 8 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN: MARTA SUCHY	06/22/95
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

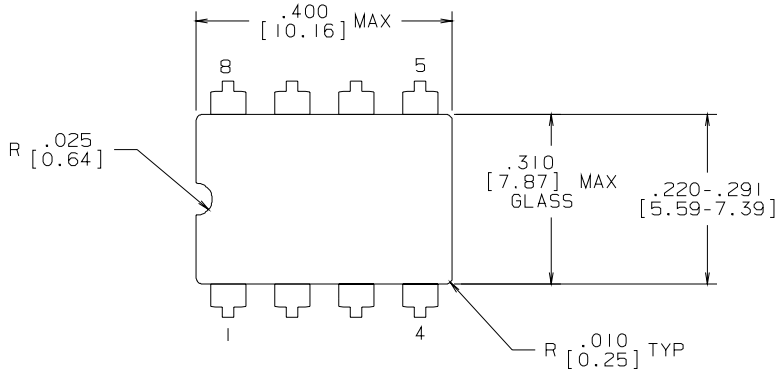
METAL CAN, TO-99, 8 LEAD, .200 DIA P.C.

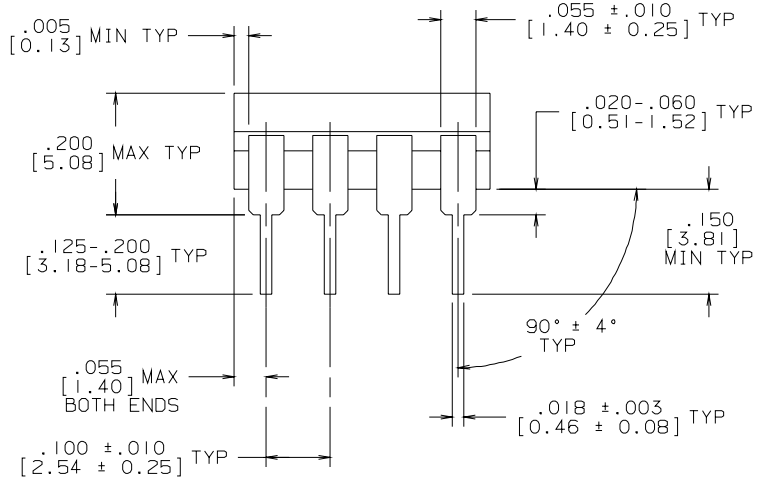
PROJECTION — INCH [MM]

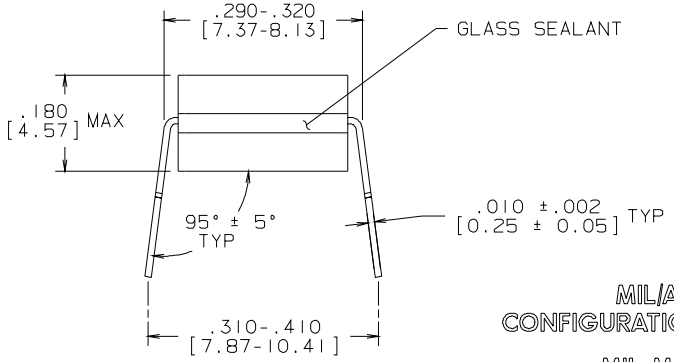
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H08C	F

DO NOT SCALE DRAWING — SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

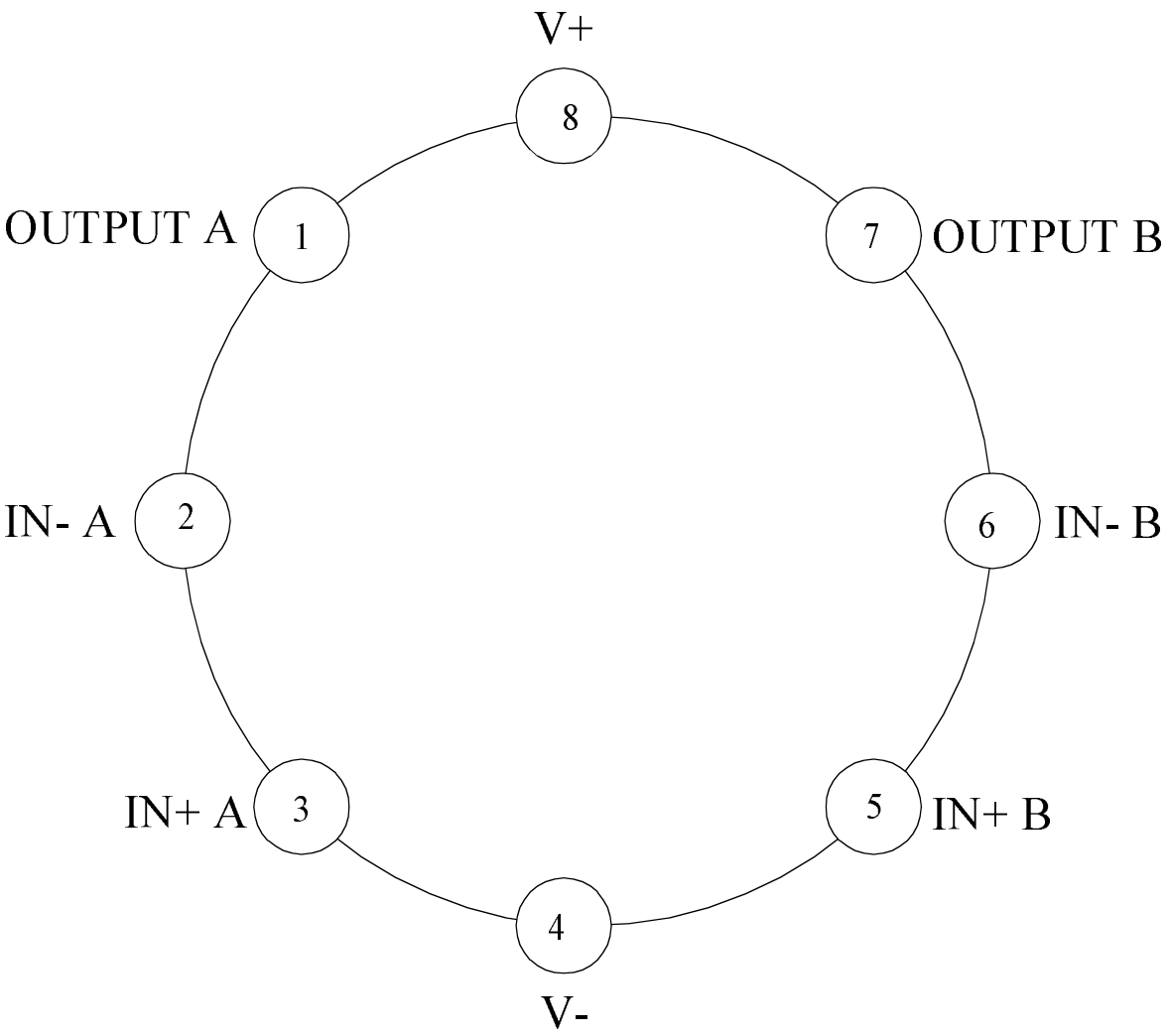
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

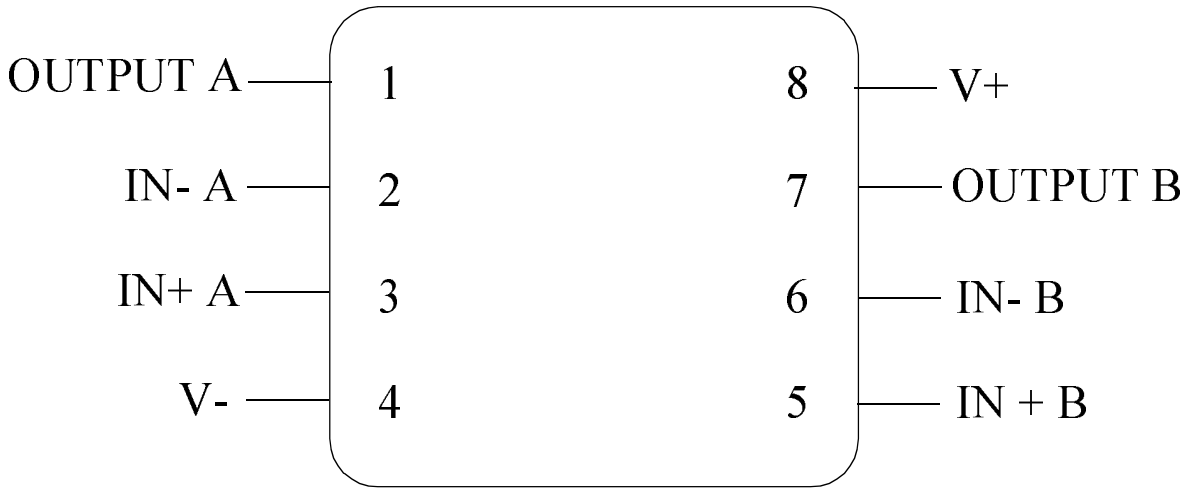
SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



LF412H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000176A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LF412J

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000177A

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Revision History

Rev	ECN #	Rel Date	Originator	Changes
0C1	M0002839	04/14/98	Barbara Lopez	Update MDS: MNLF412-X Rev. 0B0 to MNLF412-X Rev. 0C1. Updated burn-in graphics and added pinouts. Added thermal data. Added notes for power dissipation and Absolute Maximum Ratings.