National Semiconductor

MICROCIRCUIT DATA SHEET

MNLMC662AM-X REV 0B1

Original Creation Date: 08/21/95
Last Update Date: 10/23/98
Last Major Revision Date: 04/01/98

CMOS DUAL OPERATIONAL AMPLIFIER

General Description

The LMC662 CMOS Dual operational amplifier is ideal for operation from a single supply. It operates from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input Offset Current, drift and broadband noise, as well as voltage gain into realistic loads (2k Ohms and 600 Ohms), are all equal to, or better than, widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly-Silicon-Gate CMOS process.

See the LMC660 datasheet for a Quad CMOS operational amplifier with these same features.

Industry Part Number

LMC662AM

NS Part Numbers

LMC662AMJ/883

Prime Die

LMC662

Controlling Document

5962-9209401MPA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Rail-to-rail output swing.
- Specified for 2k Ohm and 600 Ohm loads.
- High voltage gain. 126dB
- Low input offset voltage. 3mV
- Low offset voltage drift. 1.3uV/ C
- Ultra low input bias current. 2fA
- Input common-mode range includes V-.
- Operating range from +5V to +15V supply.
- Iss = 400uA/amplifier; independent of V+.
- Low distortion. 0.01% at 10kHz
- Slew rate. 1.1V/us

Applications

- High-impedance buffer or preamplifier.
- Precision current-to-voltage converter.
- Long-term integrator.
- Sample-and-Hold circuit.
- Peak detector.
- Medical instrumentation.
- Industrial controls.
- Automotive sensors.

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (V+ - V-)	16V
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pins	(V+)+0.3V,(V-)-0.3V
Current at Input Pin (Note 4)	±5mA
Current at Output Pin (Note 3)	±18mA
Current at Power Supply Pin	35mA
Maximum Junction Temperature	150 C
Power Dissipation (Note 2)	170mW
Output Short Circuit to V+ (Note 4)	
Output Short Circuit to V- (Note 3)	
Storage Temperature Range	-65 C to +150 C
Operating Temperature Range	-55 C ≤ TA ≤ +125 C
Thermal Resistance (Note 6)	
ThetaJA	
8-Pin CERAMIC DIP (Still Air)	TBD
(500LF/Min Air flow)	TBD
ThetaJC	
8-Pin CERAMIC DIP	TBD
Lead Temperature (Soldering, 10 seconds)	260 C
ESD Tolerance (Note 5)	500V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Applies to both single-supply and split-supply operation. Continous short circuit operation at elevated ambient temperature and/or multiplle Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150 C. Output currents in excess of ±30mA over long term may adversely affect reliability.

Note 4: Do not connect output to V+, when V+ is greater than 13V or reliability may be adversely affected.

Note 5: Human body model, 1.5k Ohms in series with 100pF.

(Continued)

Note 6: All numbers apply for packages soldered directly into a PC board.

Recommended Operating Conditions

(Note 1)

Supply Voltage Range

4.75V to 15.5V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = +5V, V- = 0V, Vcm = 1.5V, Vo = V+/2, Rl > 1M Ohm, Rs = 0

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage				-3.0	3.0	mV	1
					-3.5	3.5	mV	2, 3
Iib	Input Bias Current				-20	20	pA	1
					-100	100	pA	2, 3
Iio	Input Offset Current				-20	20	pA	1
					-100	100	pA	2, 3
CMRR	Common Mode Rejection Ratio	Vcm = 0V and 12V, V+ = 15V			70		dB	1
					68		dB	2, 3
PSRR	Positive Power Supply Rejection Ratio	V+ = 5V and 15V, Vo = 2.5V, V- = 0V			70		dB	1
					68		dB	2, 3
PSRR	Negative Power Supply Rejection Ratio	V- = -10V and 0V, Vo = 2.5V, V+ = 5V			84		dB	1
					82		dB	2, 3
Vcm	Input Common Mode Voltage Range	V+ = 5V and 15V For CMRR >= 50dB			V+ -2.3	-0.1	V	1
					V+ -2.6	0	V	2, 3
Io	Output Current V+ = 5V	Sourcing, Vo = 0V			16		mA	1
					12		mA	2, 3
		Sinking, Vo = 5V			16		mA	1
					12		mA	2, 3
Io	Output Current V+ = 15V	Sourcing, Vo = 0V			19		mA	1, 2, 3
		Sinking, Vo = 13V			19		mA	1, 2, 3
Icc	Supply Current	Both Amplifiers Vo = 1.5V			0.258	1.3	mA	1
					0.310	1.8	mA	2, 3
		V+=15V, Both amps, Vo = 1.5V			0.258	2.5	mA	1
					0.200	4.3	mA	2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = +5V, V- = 0V, Vcm = 1.5V, Vo = V+/2, Rl > 1M Ohm, Rs = 0

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Avs	Large Signal Voltage Gain	Sourcing Vo = 7.5V to 11.5V, Rl Connected to 7.5V, V+ = 15V, Rl = 2K Ohm	1		400		V/mV	4
			1		300		V/mV	5, 6
		Sourcing Vo = 7.5V to 11.5V, RL Connected to 7.5V, V+ = 15V, Rl = 600 Ohm	1		200		V/mv	4
			1		150		V/mv	5, 6
		Sinking Vo = 2.5V to 7.5V, RL Connected to 7.5V, V+ = 15V, Rl = 2K Ohm	1		180		V/mV	4
			1		70		V/mV	5, 6
		Sinking Vo = 2.5V to 7.5V, RL Connected to 7.5V, V+ = 15V, Rl = 600 Ohm	1		100		V/mV	4
			1		20		V/mV	5, 6
Vop	Output Swing	V+ = 5V, Rl = 2K Ohm to V+/2			4.82	0.15	V	4
					4.77	0.19	V	5, 6
		V+ = 5V, Rl = 600 Ohm to V+/2			4.41	0.50	V	4
					4.24	0.63	V	5, 6
		V+ = 15V, Rl = 2K Ohm to V+/2			14.50	0.35	V	4
					14.40	0.43	V	5, 6
		V+ = 15V, Rl = 600 Ohm to V+/2			13.35	1.16	V	4
					13.02	1.42	V	5, 6

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: V+ = +5V, V- = 0V, Vcm = 1.5V, Vo = V+/2, Rl > 1M Ohm, Rs = 0

Sr±	Slew Rate	V+ = +15V	2		0.8		V/uS	4
Sr±	Slew Rate	V+ = +15V	2		0.5		V/uS	5, 6
Gbw	Gain Bandwidth	f = 50KHz			0.5		MHz	4, 5, 6

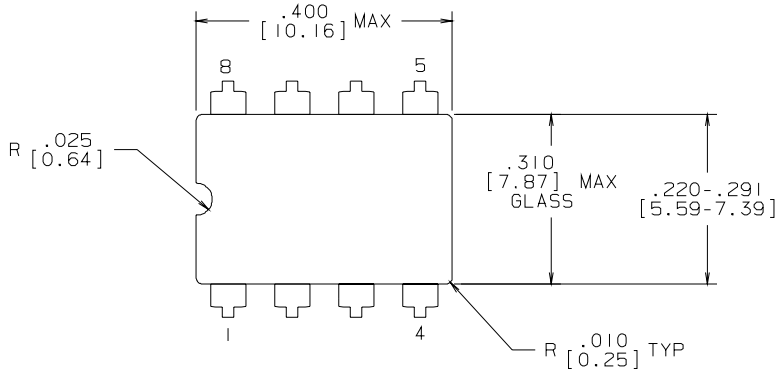
Note 1: Vcm = 7.5V and Rl connected to 7.5V.
Note 2: +Sr: Connected as Voltage Follower with 0-10V step input. Measurement taken from 4V to 8V. -Sr: Connected as Voltage Follower with 10-0V step input. Measurement taken from 6V to 2V.

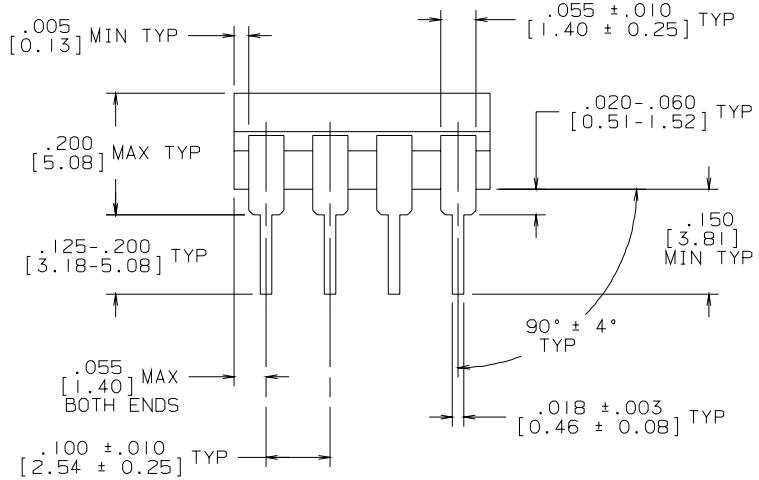
Graphics and Diagrams

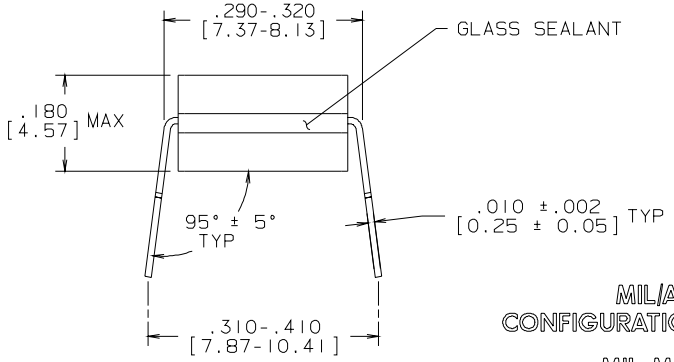
GRAPHICS#	DESCRIPTION
06086HRC4	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000166A	CERDIP (J), 8 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
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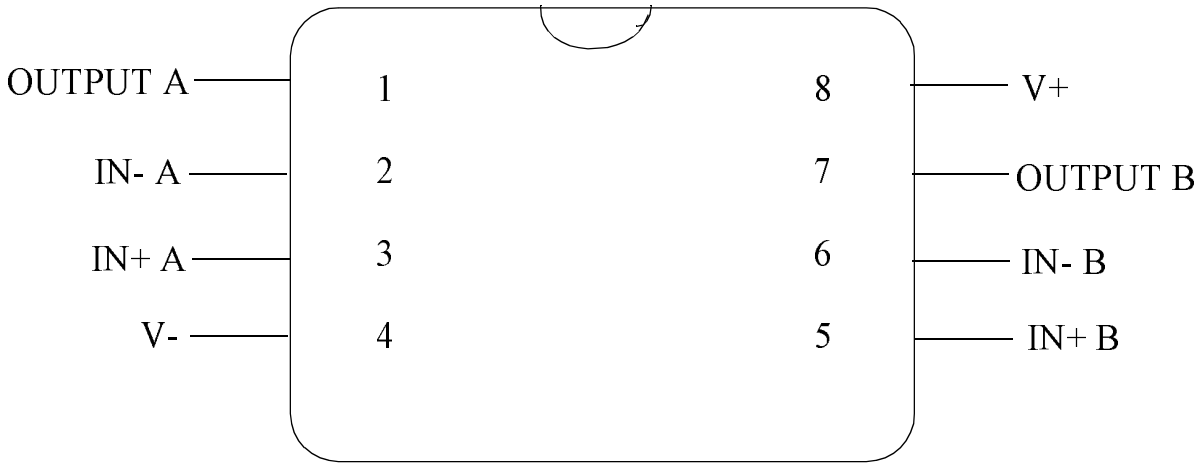
CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



LMC662AMJ/883

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000166A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0000608	10/23/98	Barbara Lopez	Initial Release to MDS: MNLMC662AM-X Rev. 0A0.
0B1	M0002852	10/23/98	Barbara Lopez	Update MDS: MNLMC662AM-X Rev. 0A0 to MNLMC662AM-X Rev. 0B1. Updated B/I graphic. Updated SMD drawing number to match SMD. Updated Subgroups to match SMD.