MPC105/D
(Motorola Order Number)

1/95
REV 1

PowerPC™

Advance Information

MPC105 PCI Bridge/Memory Controller Technical Summary

This document provides an overview of the MPC105 PCI bridge/memory controller (PCIB/MC). It includes the following:

- An overview of MPC105 features
- Details about the MPC105 device. This includes descriptions of the MPC105's functional units and interfaces.
- A description of the MPC105's signals and registers

In this document, the term "60x" is used to denote a 32-bit microprocessor from the PowerPC Architecture™ family. 60x processors implement the PowerPC™ architecture as it is specified for 32-bit addressing, which provides 32-bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits (single-precision and double-precision).

1.1 Overview

The MPC105 provides a PowerPC reference platform compliant bridge between the PowerPC microprocessor family and the Peripheral Component Interconnect (PCI) bus. PCI support allows system designers to rapidly design systems using peripherals already designed for PCI and the other standard interfaces available in the personal computer hardware environment. The MPC105 integrates secondary cache control and a high-performance memory controller that supports DRAM, SDRAM, ROM, and Flash ROM.

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The MPC105 is the first device in a family of products that provides system-level support for industry-standard interfaces to be used with PowerPC microprocessors. The MPC105 uses an advanced, 3.3 V CMOS process technology and is fully compatible with TTL devices.

This document describes the MPC105, its interfaces and its signals.

1.2 MPC105 PCIB/MC Features

The MPC105 provides an integrated high bandwidth, high performance, TTL-compatible interface between a 60x processor, a secondary (L2) cache or secondary 60x processor, the PCI bus, and main memory. This section summarizes the features of the MPC105 and provides a block diagram showing the major functional units.

Figure 1 shows the MPC105 in a typical system implementation. The major functional units within the MPC105 are also shown in Figure 1. Note that this is a conceptual block diagram intended to show the basic features rather than an attempt to show how these features are physically implemented on the device.

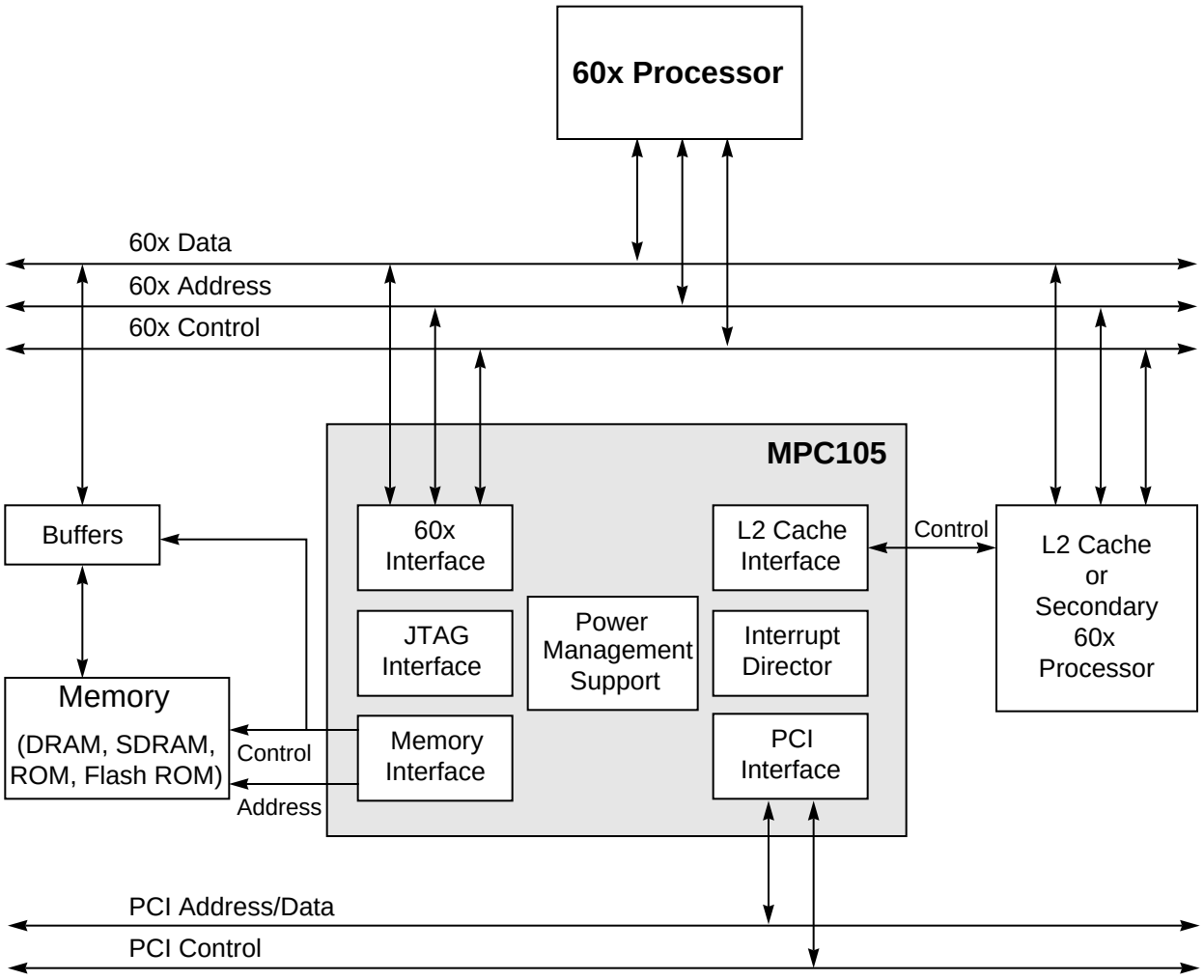

Figure 1. System Implementation and Block Diagram

Major features of the MPC105 are as follows:

- Processor interface
  - 60x processors supported at a wide range of frequencies
  - 32-bit address bus
  - Configurable 64- or 32-bit data bus
  - Accommodates an upgrade of either an external L2 cache or a secondary processor
  - Arbitration for secondary processor on-chip
  - Full memory coherency supported
  - Pipelining of 60x accesses
  - Store gathering on 60x to PCI writes
- Secondary (L2) cache control
  - Configurable for write-through or write-back operation
  - 256K, 512K, 1M sizes
  - Up to 4 Gbytes of cacheable space
  - Direct-mapped
  - Parity supported
  - Supports external byte decode or on-chip byte decode for write enables
  - Programmable timing supported
  - Synchronous burst and asynchronous SRAMs supported
- PCI interface
  - Compliant with *PCI Local Bus Specification, Revision 2.0*
  - Supports PCI interlocked accesses to memory using $\overline{\text{LOCK}}$ signal and protocol
  - Supports accesses to all PCI address spaces
  - Selectable big- or little-endian operation
  - Store gathering on PCI writes to memory
  - Selectable memory prefetching of PCI read accesses
  - Only one external load presented by the MPC105 to the PCI bus
  - PCI configuration registers
  - Interface operates at 20–33 MHz
  - Data buffering (in/out)
  - Parity supported
  - 3.3 V/5.0 V-compatible
- Concurrent transactions on 60x and PCI buses supported
- Memory interface
  - Programmable timing supported
  - Supports either DRAM or synchronous DRAM (SDRAM)
  - High bandwidth (64-bit) data bus
  - Supports self-refreshing DRAM in sleep and suspend modes
  - Supports 1 to 8 banks built of x1, x4, x8, x9, x16, or x18 DRAMs
  - Supports PowerPC reference platform compliant contiguous or discontiguous memory maps
  - 1 Gbyte of RAM space, 16 Mbytes of ROM space
  - Supports 8-bit asynchronous ROM or 32-/64-bit burst-mode ROM

  - — Supports writing to Flash ROM
  - — Configurable external buffer control logic
  - — Parity supported
  - — TTL compatible
- Power management
  - — Fully-static 3.3 V CMOS design
  - — Supports 60x nap, doze, and sleep power management modes, and suspend mode
- IEEE 1149.1-compliant, JTAG boundary scan interface
- 304-pin ball grid array (BGA) package

1.3 MPC105 Major Functional Units

The MPC105 consists of the following major functional units:

- 60x processor interface
- Secondary (L2) cache/processor interface
- PCI interface
- Memory interface

This section describes each of these functional units.

1.3.1 60x Processor Interface

The MPC105 supports a programmable interface to a variety of PowerPC microprocessors operating at various bus speeds. The 60x processor interface uses a subset of the 60x bus protocol, which enables the interface between the processor and MPC105 to be optimized for performance.

Depending on the system implementation, the processor may operate at the PCI bus clock rate, or at two or three times the PCI bus clock rate. The bus is synchronous, with all timing relative to the rising edge of the bus clock. Inputs are sampled at, and outputs are driven from, this edge. The address bus is 32 bits wide and the data bus is 64 bits wide (or 32 bits in 32-bit mode). The MPC105 supports single-beat and burst data transfers. The processor interface has decoupled address and data buses to support pipelined transactions.

PCI bus accesses to the system memory space are passed to the 60x processor(s) and/or L2 cache for snooping purposes.

1.3.2 Secondary (L2) Cache/Processor Interface

The MPC105's 60x interface allows for a variety of system configurations by providing support for either a direct-mapped, lookaside, L2 cache or a secondary 60x processor. The MPC105 uses snoop operations to ensure data coherency between the caches (one or two L1 caches, or one L1 and one L2) and main memory.

The L2 cache interface generates the arbitration and support signals necessary to maintain a write-through or write-back L2 cache. The L2 cache interface supports either burst SRAMs or asynchronous SRAMs, and L2 data parity on a per-byte basis. The MPC105 features on-chip byte decoding for L2 data write enables or can be configured to use external logic for data write enable generation.

The L2 cache interface handles the following types of bus cycles:

- Normal 60x bus cycles
- 60x internal cache copy-back cycles
- L2 copy-back cycles
- Snoop cycles

When a secondary 60x processor is used instead of an L2 cache, three signals ($\overline{\text{DIRTY\_IN/BR1}}$, $\overline{\text{DIRTY\_OUT/BG1}}$, and $\overline{\text{TOE/DBG1}}$) change their functions to allow for arbitration between two 60x processors. Excepting the bus request, bus grant, and data bus grant signals, all other 60x interface signals are shared by both 60x processors.

1.3.3 PCI Interface

The PCI interface connects the processor and memory buses to the PCI bus, to which I/O components are connected, without the need for "glue" logic. This interface acts as both a master and slave device. The PCI interface supports a 32-bit multiplexed, address/data bus that can operate from 20 MHz to 33 MHz. Buffers are provided for I/O operations between the PCI bus and the 60x processor or memory. Processor read and write operations each have a 32-byte buffer, and memory operations have one 32-byte read buffer and two 32-byte write buffers. The PCI interface supports address and data parity with error checking and reporting. The interface also supports three physical address spaces—32-bit address memory, 32-bit address I/O, and some of the PCI 256-byte configuration space. Mode selectable big-endian to little-endian conversion is also supplied at the PCI interface.

The MPC105's PCI interface is compliant with the *PCI Local Bus Specification, Revision 2.0*, and follows the guidelines in the *PCI System Design Guide, Revision 1.0* for host bridge architecture.

1.3.4 Memory Interface

The memory interface controls processor and PCI interactions to main memory. It is capable of supporting a variety of DRAM or SDRAM, and ROM or Flash ROM configurations as main memory. The maximum supported memory size is 1 Gbyte of DRAM or SDRAM, with 16 Mbytes of ROM or 1 Mbyte of Flash ROM. The MPC105 configures its memory control to support the various memory sizes through software initialization of on-chip configuration registers. Parity protection is provided for the DRAM or SDRAM. If SDRAM is used, it must comply with the JEDEC specification for SDRAM.

The MPC105 can control either a 64- or 32-bit data path to main memory; SDRAM systems support 64-bit data paths only. To reduce loading on the data bus, system designers may implement buffers between the 60x bus and memory. The MPC105 features configurable data buffer control logic to accommodate several buffer types. The MPC105 handles parity checking and generation, with four parity bits checked or generated for a 32-bit data path, and eight parity bits checked or generated for a 64-bit data path.

The MPC105 is capable of supporting a variety of DRAM or SDRAM configurations. Twelve multiplexed address signals provide for device densities to 16 M. Eight row address strobe/command select ($\overline{\text{RAS/CS}}$) signals support up to eight banks of memory. Each bank can be 8 bytes wide. Eight column address strobe/data qualifier ($\overline{\text{CAS/DQM}}$) signals are used to provide byte selection for memory accesses.

DRAM or SDRAM banks can be built of SIMMs or directly attached memory chips. The data path to the memory banks must be either 32 or 64 bits wide (36 or 72 with parity). The banks can be constructed using x1, x4, x8, x9, x16, or x18 memory chips. Regardless of whether DRAMs or SDRAMs are used, the memory design must be byte-selectable for writes using the $\overline{\text{CAS/DQM}}$ signals.

The MPC105 memory interface provides for doze, nap, sleep, and suspend power saving modes, defined in Section 1.4, “Power Management.” In the sleep and suspend power saving modes, the MPC105 can be configured to put the DRAM array into a self-refresh mode, (if supported by the DRAMs). The MPC105 may be configured to use the RTC input as its refresh time base in suspend mode. If self-refreshing DRAMs are not available or the RTC input is not used (in suspend mode), system software must preserve DRAM data (such as by copying the data to disk) in the sleep or suspend mode. In the doze and nap power saving modes and in the full-on mode, the MPC105 supplies CAS before RAS (CBR) refresh to DRAM.

An MPC105 configuration signal (sampled at reset) determines whether the MPC105 accesses boot code from ROM or Flash ROM. If the MPC105 is configured to access boot code from ROM, the corresponding data path must be the same bit width as the DRAM or SDRAM data path (32 or 64 bits). Twenty address bits and two bank selects are provided for ROM systems. If the MPC105 is configured to access boot code from Flash ROM, the corresponding data path must be 8 bits wide and must be connected to the most significant byte of the data bus. Twenty address bits, one bank select signal, one write enable signal, and one output enable signal are provided for Flash ROM systems.

1.4 Power Management

The MPC105 provides hardware support for four levels of power reduction; the doze, nap, and sleep modes are invoked by register programming, and the suspend mode is invoked by assertion of an external signal. The design of the MPC105 is fully static, allowing internal logic states to be preserved during all power saving modes. The following sections describe the programmable power modes provided by the MPC105.

1.4.1 Full-On Mode

This is the default power state of the MPC105 following a hard reset, with all internal functional units fully powered and operating at full clock speed.

1.4.2 Doze Mode

In this power saving mode, all the MPC105 functional units are disabled except for PCI address decoding, system RAM refreshing, and the CPU bus request monitoring (through $\overline{\text{BRx}}$). Once the doze mode is entered, a hard reset, a PCI transaction referenced to the system memory, or a bus request can bring the MPC105 out of the doze mode and into the full-on state. If the MPC105 is awakened for a processor or PCI bus access, the access is completed and the MPC105 returns to the doze mode. The MPC105’s doze mode is totally independent of the power saving mode of the processor.

1.4.3 Nap Mode

Further power savings can be achieved through the nap mode, when both the processor and the MPC105 are placed in a power reduction mode. In this mode, only the PCI address decoding, system RAM refresh, and the processor bus request monitoring are still operating. Hard reset, a PCI bus transaction referenced to the system memory, or a bus request can bring the MPC105 out of the nap mode. If the MPC105 is awakened by a PCI access, the access is completed, and the MPC105 returns to the nap mode. If the MPC105 is awakened by a processor access, the access is completed, but the MPC105 remains in the full-on state. When in the nap mode, the PLL is required to be running and locked to the system clock (SYSCLK).

1.4.4 Sleep Mode

Sleep mode provides further power savings compared to the nap mode. As in nap mode, both the processor and the MPC105 are placed in a reduced power mode concurrently. In sleep mode, no functional units are operating except the system RAM refresh logic, which can continue (optionally) to perform the refresh cycles. A hard reset or a bus request wakes the MPC105 from the sleep mode. The PLL and SYSCLK inputs may be disabled by an external power management controller (PMC). For additional power savings, the PLL can be disabled by configuring the PLL0–PLL3 signals into the PLL bypass mode. When recovering from sleep mode, the external PMC has to re-enable the PLL and SYSCLK first, and then wake up the system after allowing the PLL time to relock.

1.4.5 Suspend Mode

Suspend mode is activated through assertion of the $\overline{\text{SUSPEND}}$ signal. In suspend mode, the MPC105 may have its clock input and PLL shut down for additional power savings. Memory refresh can be accomplished in two ways—either by using self-refresh mode DRAMs or by using the RTC input. To exit the suspend mode, the system clock must be turned on in sufficient time to restart the PLL. After this time, $\overline{\text{SUSPEND}}$ may be negated. In suspend mode, all outputs (except memory refresh) are high impedance and all inputs (including $\overline{\text{HRST}}$) are ignored.

1.5 Signals

The MPC105's signals, shown in Figure 2, are grouped as follows:

- 60x processor interface signals
- Secondary cache/processor interface signals
- PCI interface signals
- Memory interface signals
- Interrupt, clock, and power management signals
- IEEE 1149.1 interface signals
- Configuration signals

NOTE

A bar over a signal name indicates that the signal is active low—for example, $\overline{\text{ARTRY}}$ (address retry) and $\overline{\text{TS}}$ (transfer start). Active-low signals are referred to as asserted (active) when they are low and negated when they are high. Signals that are not active low, such as PAR (PCI bus parity signal) and TT0–TT4 (transfer type signals) are referred to as asserted when they are high and negated when they are low.

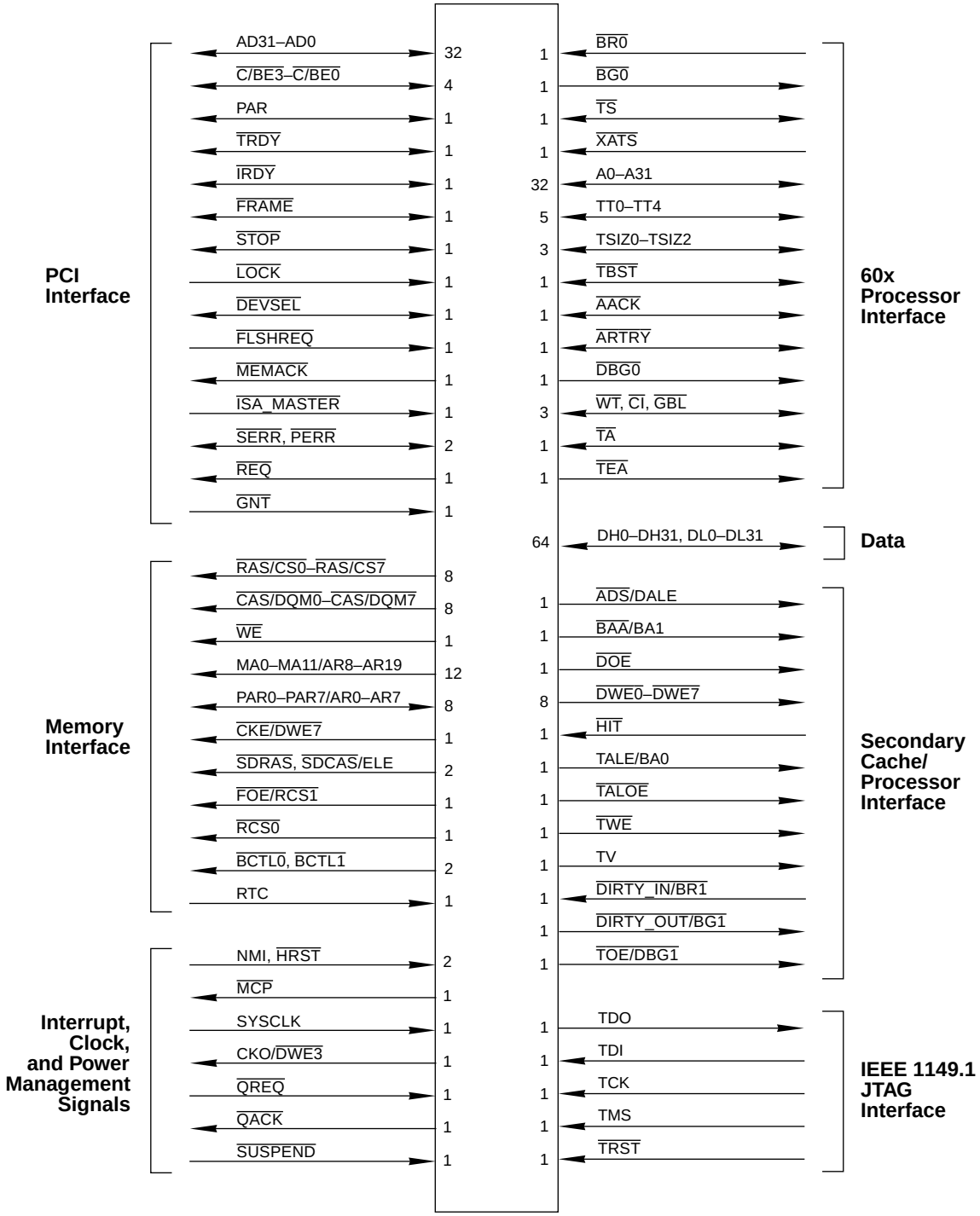

Figure 2. MPC105 Signal Groupings

1.5.1 60x Processor Interface Signals

Table 1 lists the 60x processor interface signals on the MPC105 and provides a brief description of their functions.

Table 1. 60x Processor Interface Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
$\overline{\text{BR0}}$	Bus request 0	1	I	Indicates that the primary 60x requires the bus for a transaction
$\overline{\text{BG0}}$	Bus grant 0	1	O	Indicates that the primary 60x may, with the proper qualification, begin a bus transaction and assume mastership of the address bus
$\overline{\text{TS}}$	Transfer start	1	O	Indicates that the MPC105 has started a bus transaction, and that the address and transfer attribute signals are valid. Note that the MPC105 only initiates a transaction to broadcast the address of a PCI access to memory for snooping purposes.
			I	Indicates that a 60x bus master has begun a transaction, and that the address and transfer attribute signals are valid
$\overline{\text{XATS}}$	Extended address transfer start	1	I	Indicates that the 60x has started a direct-store access (using the extended transfer protocol). Since direct-store accesses are not supported by the MPC105, the MPC105 automatically asserts $\overline{\text{TEA}}$ when $\overline{\text{XATS}}$ is asserted (provided $\overline{\text{TEA}}$ is enabled).
A0–A31	Address bus	32	O	Specifies the physical address for 60x bus snooping or for an L2 copy-back operation
			I	Specifies the physical address of the bus transaction. For burst reads, the address is aligned to the critical double-word address that missed in the instruction or data cache. For burst writes, the address is aligned to the double-word address of the cache line being pushed from the data cache.
TT0–TT4	Transfer type	5	O	Specifies the type of 60x bus transfer in progress for snooping
			I	Specifies the type of 60x bus transfer in progress
TSIZ0–TSIZ2	Transfer size	3	O	Specifies the data transfer size for the 60x bus transaction
			I	Specifies the data transfer size for the 60x bus transaction
$\overline{\text{TBST}}$	Transfer burst	1	O	Indicates that a burst transfer is in progress
			I	Indicates that a burst transfer is in progress

Table 1. 60x Processor Interface Signals (Continued)

Signal	Signal Name	Number of Pins	I/O	Signal Description
$\overline{\text{AACK}}$	Address acknowledge	1	O	Indicates that the address tenure of a transaction is terminated. On the cycle following the assertion of $\overline{\text{AACK}}$, the bus master releases the address-tenure-related signals to a high impedance state and samples $\overline{\text{ARTRY}}$.
			I	Indicates that a 60x bus slave is terminating the address tenure. On the cycle following the assertion of $\overline{\text{AACK}}$, the bus master releases the address tenure related signals to a high impedance state and samples $\overline{\text{ARTRY}}$.
$\overline{\text{ARTRY}}$	Address retry	1	O	Indicates that the initiating 60x bus master must retry the current address tenure
			I	During a snoop operation, indicates that the 60x either requires the current address tenure to be retried due to a pipeline collision or needs to perform a snoop copy-back. During normal 60x bus cycles in a multiprocessor system, indicates that the other 60x requires the address tenure to be retried.
$\overline{\text{DBG0}}$	Data bus grant 0	1	O	Indicates that the 60x may, with the proper qualification, assume mastership of the data bus. A qualified data bus grant is the assertion of $\overline{\text{BG0}}$, negation of $\overline{\text{DBB}}$, and negation of $\overline{\text{ARTRY}}$. The address retry ($\overline{\text{ARTRY}}$) is only for the address bus tenure associated with the data bus tenure about to be granted (that is, not for another address tenure available because of address pipelining).
DH0–DH31, DL0–DL31	Data bus	64		The data bus is comprised of two halves—data bus high (DH) and data bus low (DL). The data bus has the following byte lane assignments: Data Byte — Byte Lane DH0–DH7 — 0 DH8–DH15 — 1 DH16–DH23 — 2 DH24–DH31 — 3 DL0–DL7 — 4 DL8–DL15 — 5 DL16–DL23 — 6 DL24–DL31 — 7
			O	Represents the value of data during a processor-read-from-PCI transaction, a PCI-write-to-memory transaction, or when the MPC105 flushes the L2 copy-back buffer
			I	Represents the state of data during a processor-write-to-PCI transaction, a PCI-read-from-memory transaction, or when the L2 is loading the copy-back buffer

Table 1. 60x Processor Interface Signals (Continued)

Signal	Signal Name	Number of Pins	I/O	Signal Description
$\overline{CI}$	Cache inhibit	1	I/O	Indicates that an access is caching-inhibited
$\overline{WT}$	Write through	1	I/O	Indicates that an access is write-through
$\overline{GBL}$	Global	1	I/O	Indicates that an access is global (that is, coherency needs to be enforced by hardware)
$\overline{TA}$	Transfer acknowledge	1	O	Indicates that the data has been latched for a write, or that the data is valid for a read, thus terminating the current data beat. If it is the last or only data beat, this also terminates the data tenure.
			I	Indicates that a 60x bus slave has latched data for a write operation, or is indicating the data is valid for a read operation. If it is the last or only data beat, then the data tenure is terminated.
$\overline{TEA}$	Transfer error acknowledge	1	O	Indicates that a bus error has occurred. Assertion of $\overline{TEA}$ terminates the transaction in progress; that is, it is not necessary to assert $\overline{TA}$ because it will be ignored by the target processor. An unsupported memory transaction, such as a direct-store access or a graphics read or write, will cause the assertion of $\overline{TEA}$ (provided $\overline{TEA}$ is enabled).

1.5.2 Secondary Cache/Processor Interface Signals

The MPC105 provides support for either a secondary lookaside L2 cache or an additional 60x processor.

1.5.2.1 Secondary Cache (L2) Interface Signals

Table 2 lists the secondary cache interface signals and provides a brief description of their functions. The L2 cache interface supports either burst SRAMs or asynchronous SRAMs. Some of the L2 interface signals perform different functions depending on the SRAM configuration and whether the on-chip byte decode logic is enabled.

Table 2. Secondary Cache Interface Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
$\overline{\text{ADS}}$/DALE	Address strobe/ data address latch enable	1	O	For a burst SRAM configuration, indicates to the burst SRAM that the address is valid to be latched –or– For an asynchronous SRAM configuration, indicates to the external address latch that the address is valid to be latched
$\overline{\text{BAA}}$/BA1	Bus address advance/burst address 1	1	O	For a burst SRAM configuration, indicates that the burst RAMs should increment their internal addresses –or– For an asynchronous SRAM configuration, indicates the least significant bit of the burst address
$\overline{\text{DIRTY\_IN/BR1}}$	Dirty in	1	I	Indicates that the selected L2 cache line is modified. The polarity of $\overline{\text{DIRTY\_IN/BR1}}$ is programmable.
$\overline{\text{DIRTY\_OUT/BG1}}$	Dirty out	1	O	Indicates that the L2 cache line should be marked as modified. The polarity of $\overline{\text{DIRTY\_OUT/BG1}}$ is programmable.
$\overline{\text{DOE}}$	Data RAM output enable	1	O	Indicates that the L2 data RAMs should drive the data bus
$\overline{\text{HIT}}$	Hit	1	I	Indicates that the L2 cache has detected a hit. The polarity of $\overline{\text{HIT}}$ is programmable.
TALE/BA0	Tag address latch enable/ burst address 0	1	O	For a burst SRAM configuration, indicates that the address latch should be in the transparent state for the L2 local address bus –or– For an asynchronous SRAM configuration, indicates the most significant bit of the burst address
$\overline{\text{TALOE}}$	Tag address latch output enable	1	O	Indicates that the address latch should drive the L2 local address bus for tag lookup or tag write
$\overline{\text{TOE}}$ /$\overline{\text{DBG1}}$	Tag output enable	1	O	Indicates that the tag RAM should drive the L2 tag address onto the address bus
$\overline{\text{TWE}}$	Tag write enable	1	O	Indicates that the L2 tag address, valid, and dirty bits should be updated

Table 2. Secondary Cache Interface Signals (Continued)

Signal	Signal Name	Number of Pins	I/O	Signal Description
TV	Tag valid	1	O	Indicates that the current L2 cache line should be marked valid. The polarity of TV is programmable.
FNR/$\overline{\text{DWE0}}$, $\overline{\text{DWE/DWE1}}$, $\overline{\text{DWE2}}$, CKO/$\overline{\text{DWE3}}$, $\overline{\text{DWE4}}$–$\overline{\text{DWE6}}$, $\overline{\text{CKE/DWE7}}$	Data RAM write enable ($\overline{\text{DWE0}}$–$\overline{\text{DWE7}}$)	8	O	For external byte decode configurations, $\overline{\text{DWE/DWE1}}$ indicates that a write to the L2 data RAMs is in progress –or– For on-chip byte decode configurations, $\overline{\text{DWE0}}$–$\overline{\text{DWE7}}$ function as individual byte lane (0–7) write enables for the L2 data RAMs

1.5.2.2 Secondary Processor Signals

When a secondary 60x processor is used instead of an L2 cache, three signals change their functions. Table 3 lists the secondary processor interface signals and provides a brief description of their functions.

Table 3. Secondary Processor Interface Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
$\overline{\text{DIRTY\_IN/BR1}}$	Bus request 1	1	I	Indicates that the secondary processor requires mastership of the 60x bus for a transaction
$\overline{\text{DIRTY\_OUT/BG1}}$	Bus grant 1	1	O	Indicates that the secondary processor may, with the proper qualification, begin a 60x bus transaction and assume mastership of the address bus
$\overline{\text{TOE /DBG1}}$	Data bus grant 1	1	O	Indicates that the secondary processor may, with the proper qualification, assume mastership of the 60x data bus

1.5.3 PCI interface signals

Table 4 lists the PCI interface signals and provides a brief description of their functions. Note that the bits in Table 4 are referenced in little-endian format.

The PCI specification defines a sideband signal as any signal, not part of the PCI specification, that connects two or more PCI-compliant agents, and has meaning only to those agents. The MPC105 implements three PCI sideband signals—$\overline{\text{ISA\_MASTER}}$, $\overline{\text{FLSHREQ}}$, and $\overline{\text{MEMACK}}$.

Table 4. PCI Bus Interface Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
AD31–AD0	Address/data	32	O	Represents the physical address during the first clock of a transaction. During subsequent clocks, AD31–AD0 contain data being written. AD7–AD0 define the least significant byte and AD31–AD24 the most significant byte.
			I	Represents the address to be decoded as check for device select or data being received
$\overline{\text{C/BE3}}$–$\overline{\text{C/BE0}}$	Command/byte enables	4	O	During the address phase, $\overline{\text{C/BE3}}$–$\overline{\text{C/BE0}}$ define the bus command. During the data phase, $\overline{\text{C/BE3}}$–$\overline{\text{C/BE0}}$ are used as byte enables. Byte enables determine which byte lanes carry meaningful data. $\overline{\text{C/BE0}}$ applies to the least significant byte.
			I	Indicates the command that another master is running, or which byte lanes are valid
PAR	Parity	1	O	Asserted indicates odd parity across the AD31–AD0 and $\overline{\text{C/BE3}}$–$\overline{\text{C/BE0}}$ signals during address and data phases. Negated indicates even parity.
			I	Asserted indicates odd parity driven by another PCI master or the PCI target during read data phases. Negated indicates even parity.
$\overline{\text{TRDY}}$	Target ready	1	O	Indicates that the MPC105, acting as a PCI target, can complete the current data phase of a PCI transaction. During a read, the MPC105 asserts $\overline{\text{TRDY}}$ to indicate that valid data is present on AD31–AD0. During a write, the MPC105 asserts $\overline{\text{TRDY}}$ to indicate that it is prepared to accept data.
			I	Indicates another PCI target is able to complete the current data phase of a transaction
$\overline{\text{IRDY}}$	Initializer ready	1	O	Indicates that the MPC105, acting as a PCI master, can complete the current data phase of a PCI transaction. During a write, the MPC105 asserts $\overline{\text{IRDY}}$ to indicate that valid data is present on AD31–AD0. During a read, the MPC105 asserts $\overline{\text{IRDY}}$ to indicate that it is prepared to accept data.
			I	Indicates another PCI master is able to complete the current data phase of the transaction

Table 4. PCI Bus Interface Signals (Continued)

Signal	Signal Name	Number of Pins	I/O	Signal Description
$\overline{\text{FRAME}}$	Frame	1	O	Indicates that the MPC105, acting as a PCI master, is initiating a bus transaction. While $\overline{\text{FRAME}}$ is asserted, data transfers continue.
			I	Indicates that another PCI master is initiating a bus transaction
$\overline{\text{STOP}}$	Stop	1	O	Indicates that the MPC105 is requesting that the PCI bus master stop the current transaction
			I	Indicates that some other PCI agent is requesting that the MPC105, acting as the PCI master, stop the current transaction
$\overline{\text{LOCK}}$	Lock	1	I	Indicates that a master is requesting exclusive access to memory, which may require multiple transactions to complete
$\overline{\text{DEVSEL}}$	Device select	1	O	Indicates that the MPC105 has decoded the address and is the target of the current access
			I	Indicates that some PCI agent (other than the MPC105) has decoded its address as the target of the current access
$\overline{\text{REQ}}$	PCI bus request	1	O	Indicates that the MPC105 is requesting control of the PCI bus. Note that $\overline{\text{REQ}}$ is a point-to-point signal. Every master has its own $\overline{\text{REQ}}$ signal.
$\overline{\text{GNT}}$	PCI bus grant	1	I	Indicates that the MPC105 has been granted control of the PCI bus. Note that $\overline{\text{GNT}}$ is a point-to-point signal. Every master has its own $\overline{\text{GNT}}$ signal.
$\overline{\text{SERR}}$	System error	1	O	Indicates that an address parity error or some other system error (where the result will be a catastrophic error) was detected
			I	Indicates that another target has determined a catastrophic error
$\overline{\text{PERR}}$	Parity error	1	O	Indicates that the MPC105, acting as a PCI target, detected a data parity error
			I	Indicates that another target detected a data parity error while the MPC105 was the master
$\overline{\text{ISA\_MASTER}}$	ISA master	1	I	Indicates that an ISA master is requesting system memory

Table 4. PCI Bus Interface Signals (Continued)

Signal	Signal Name	Number of Pins	I/O	Signal Description
$\overline{\text{FLSHREQ}}$	Flush request	1	I	Indicates that a device needs to have the MPC105 flush all of its current operations
$\overline{\text{MEMACK}}$	Flush acknowledge	1	O	Indicates that the MPC105 has flushed all of its current operations and has blocked all 60x transfers except snoop copy-back operations. The MPC105 will assert $\overline{\text{MEMACK}}$ after the flush is complete.

1.5.4 Memory Interface Signals

Table 5 lists the memory interface signals and provides a brief description of their functions. The memory interface supports either standard DRAMs or synchronous DRAMs (SDRAMs), and either standard ROMs or Flash ROMs. Some of the memory interface signals perform different functions depending on the RAM and ROM configurations.

Table 5. Memory Interface Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
$\overline{\text{RAS/CS0}}$–$\overline{\text{RAS/CS7}}$	Row address strobe for DRAM/ command select for SDRAM	8	O	Indicates a DRAM row address is valid and selects one of the rows in the bank –or– Selects an SDRAM bank to perform a memory operation
$\overline{\text{CAS/DQM0}}$–$\overline{\text{CAS/DQM7}}$	Column address strobe/ data qualifier	8	O	Indicates a DRAM column address is valid and selects one of the columns in the row. $\overline{\text{CAS/DQM0}}$ connects to the most significant byte select. $\overline{\text{CAS/DQM7}}$ connects to the least significant byte select. –or– Prevents writing to SDRAM.
$\overline{\text{WE}}$	Write enable	1	O	Enables writing to DRAM or Flash ROM –or– Part of SDRAM command encoding
MA0–MA11/ AR8–AR19	Memory address 0–11/ ROM address 8–19	12	O	Represents the row/column multiplexed physical address for DRAMs or SDRAMs (MA0 is the most significant address bit; MA11 is the least significant address bit) –or– Represents bits 8–19 of the ROM or Flash ROM address (the 12 lowest order bits, with AR19 as the lsb). Bits 0–7 of the ROM address are provided by PAR0–PAR7/AR0–AR7.

Table 5. Memory Interface Signals (Continued)

Signal	Signal Name	Number of Pins	I/O	Signal Description
PAR0–PAR7/ AR0–AR7	Data parity 0–7/ ROM address 0–7	8	O	Represents the byte parity being written to memory (PAR0 is the most significant parity bit) –or– Represents bits 0–7 of the ROM or Flash ROM address (the eight highest order bits, with AR0 as the msb). Bits 8–19 of the ROM address are provided by MA0–MA11/AR8–AR19.
			I	Represents the byte parity being read from memory (PAR0 is the most significant parity bit)
$\overline{\text{CKE}}/\overline{\text{DWE7}}$	Memory clock enable	1	O	Enables the internal clock circuit of the SDRAM memory. Also $\overline{\text{CKE}}/\overline{\text{DWE7}}$ is part of the SDRAM command encoding. Note that the MPC105 negates $\overline{\text{CKE}}/\overline{\text{DWE7}}$ during certain system power down situations.
$\overline{\text{SDRAS}}$	Row address strobe for SDRAM	1	O	$\overline{\text{SDRAS}}$ is part of the SDRAM command encoding used for SDRAM bank selection during read or write operations
$\overline{\text{SDCAS}}$/ELE	Column address strobe for SDRAM/ external latch enable	1	O	$\overline{\text{SDCAS}}$/ELE is part of the SDRAM command encoding used for SDRAM column selection during read or write operations –or– Enables the external data buffer for read operations, if such a buffer is used in the system
$\overline{\text{RCS0}}$	ROM/Flash ROM bank 0 select	1	O	Selects the first ROM bank or Flash ROM for a read access
$\overline{\text{FOE}}/\overline{\text{RCS1}}$	Flash ROM output enable/ ROM second bank select	1	O	Enables Flash ROM output for the current read access –or– Selects the second ROM bank for a read access
$\overline{\text{BCTL0}}$ $\overline{\text{BCTL1}}$	Buffer control 0, buffer control 1	2	O	Used to control external data bus buffers (directional control and high-impedance state) between the 60x bus and memory. Note that external data buffers may be optional for lightly loaded data buses, but buffers are required whenever an L2 cache and ROM/Flash ROM are both in the system.
RTC	Real-time clock	1	I	External clock source for the memory refresh logic when the MPC105 is in the suspend power-saving mode

1.5.5 Interrupt, Clock, and Power Management Signals

The MPC105 coordinates a few miscellaneous signals across the memory bus, the PCI bus, and the 60x bus. These include interrupt, clocking, and power management signals. Table 6 lists these signals and provides a brief description of their functions.

Table 6. Interrupt, Clocking, and Power Management Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
NMI	Nonmaskable interrupt	1	I	Indicates that the MPC105 should signal a machine check interrupt to the 60x processor
$\overline{\text{MCP}}$	Machine check	1	O	Indicates that the MPC105 detected an illegal transaction, a memory select error, or a parity error on a memory read cycle. Assertion of $\overline{\text{SERR}}$, $\overline{\text{PERR}}$, or NMI may also trigger $\overline{\text{MCP}}$.
$\overline{\text{HRST}}$	Hard reset	1	I	Indicates that a complete hard reset must be initiated by the MPC105 (perform circuit initialization followed by a system reset interrupt). During assertion, all bidirectional signals are released to the high impedance state and all output signals are either in a high impedance or inactive state.
SYSCLK	System clock	1	I	SYSCLK set the frequency of operation for the PCI bus, and provides a reference clock for the phase-locked loops (PLLs) in the 60x and the MPC105. SYSCLK is used to synchronize bus operations. Refer to Section 1.5.8, “Clocking,” for more information.
CK0/$\overline{\text{DWE3}}$	Test clock	1	O	This signal provides a means to test or monitor the internal PLL output, or the bus clock frequency. The test clock should be used for testing purposes only. It is not intended to be used as a reference clock.
$\overline{\text{QREQ}}$	Quiesce request	1	I	Indicates that a 60x processor is requesting that all bus activity involving snoop operations pause or terminate so that the 60x processor may enter a low-power state
$\overline{\text{QACK}}$	Quiesce acknowledge	1	O	Indicates that the MPC105 is in a low-power state. All bus activity that requires snooping has terminated, and the 60x processor may enter a low-power state.
$\overline{\text{SUSPEND}}$	Suspend	1	I	Activates the suspend power-saving mode

1.5.6 IEEE 1149.1 Interface Signals

To facilitate system testing, the MPC105 provides a JTAG test port that complies with the IEEE 1149.1 boundary scan specification. Table 7 describes the JTAG test port signals.

Table 7. IEEE 1149.1 Boundary Scan Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
TDO	JTAG test data output	1	O	The contents of the selected internal instruction or data register are shifted out onto this signal on the falling edge of TCK. TDO will remain in a high impedance state except when scanning of data is in progress.
TDI	JTAG test data Input	1	I	The value presented on this signal on the rising edge of TCK is clocked into the selected JTAG test instruction or data register.
TCK	JTAG test clock	1	I	This input should be driven by a free-running clock signal. Input signals to the test access port (TAP) are clocked in on the rising edge of TCK. Changes to the TAP output signals occur on the falling edge of TCK. The test logic allows TCK to be stopped.
TMS	JTAG test mode select	1	I	This signal is decoded by the internal JTAG TAP controller to distinguish the primary operation of the test support circuitry.
$\overline{\text{TRST}}$	JTAG test reset	1	I	This input causes asynchronous initialization of the internal JTAG TAP controller.

1.5.7 Configuration Signals

Several of the MPC105 signals are sampled during a power-on reset to determine the configuration of the ROM, Flash ROM, and dynamic memory, the data-bus width, and the phased-locked loop clock mode. Weak pull-up or pull-down resistors should be used so as not to interfere with the normal operation of the signals. Table 8 describes the signals sampled during a power-on reset, and how they are configured.

Table 8. Power-On Configuration Signals

Signal	Number of Pins	I/O	Configuration
FNR/$\overline{\text{DWE0}}$	1	I	High—configures the MPC105 for Flash (8-bit interface) memory. Low—configures the MPC105 for ROM (32- or 64- bit interface) memory
$\overline{\text{RCS0}}$	1	I	High—indicates ROM is located on the 60x processor/ memory data bus Low—indicates ROM is located on the PCI bus

Table 8. Power-On Configuration Signals (Continued)

Signal	Number of Pins	I/O	Configuration
DL[0]	1	I	High—configures the MPC105 for 64-bit processor/memory data bus width Low— configures the MPC105 for 32-bit processor/memory data bus width
$\overline{\text{XATS}}$	1	I	High—configures the MPC105 for address map A Low—configures the MPC105 for address map B
PLL0–PLL3	4	I	High/Low—configuration for the PLL clock mode

1.5.8 Clocking

The MPC105 can be configured to operate internally at x1 or x2 of the PCI bus clock (SYSCLK) by using the PLL0–PLL3 signals. Table 9 shows the clock combinations supported by an MPC105-based system.

Table 9. Clock Frequencies

60x Processor External Clock Frequency	60x Processor Internal Clock Frequency	MPC105 External Clock Frequency (SYSCLK)[1]	MPC105 Internal Clock Frequency	PCI Bus Clock (SYSCLK)[1]
40 MHz	80 MHz	20 MHz	40 MHz	20 MHz
25 MHz	75 MHz[2]	25 MHz	25 MHz	25 MHz
33 MHz	66 MHz	33 MHz	33 MHz	33 MHz
33 MHz	100 MHz	33 MHz	33 MHz	33 MHz
66 MHz	66 MHz	33 MHz	66 MHz	33 MHz
66 MHz	100 MHz[3]	33 MHz	66 MHz	33 MHz

[1] The MPC105 external clock and the PCI bus clock are the same signal (SYSCLK).
[2] 80 MHz processor operating at 75 MHz.
[3] PowerPC 604™ microprocessor only.

1.6 Configuration Registers

The MPC105 provides user accessible registers for configuration, initialization, and error handling. These registers are generally set by initialization software following a power-on reset or hard reset, or by error handling routines. Table 10 describes the configuration registers provided by the MPC105. Figure 3 shows the registers in the configuration space of the MPC105.

Table 10. MPC105 Configuration Registers

Address Offset	Register Size	Program Accessible Size	Register	Register Access	Reset Value
00	2 bytes	2 bytes	Vendor ID =1057h	Read	0x1057
02	2 bytes	2 bytes	Device ID = 0001h	Read	0x0001
04	2 bytes	2 bytes	PCI command	Read/write	0x0006
06	2 bytes	2 bytes	PCI status	Read/bit-reset	0x0080
08	1 byte	1 byte	Revision ID	Read	0x*nn*
09	1 byte	1 byte	Standard programming interface	Read	0x00
0A	1 byte	1 byte	Subclass code	Read	0x00
0B	1 byte	1 byte	Class code	Read	0x06
0C	1 byte	1 byte	Cache line size	Read	0x00
0D	1 byte	1 byte	Latency timer	Read	0x00
0E	1 byte	1 byte	Header type	Read	0x00
0F	1 byte	1 byte	BIST control	Read	0x00
3C	1 byte	1 byte	Interrupt line	Read	0x00
3D	1 byte	1 byte	Interrupt pin	Read	0x00
3E	1 byte	1 byte	MIN GNT	Read	0x00
3F	1 byte	1 byte	MAX GNT	Read	0x00
40	1 byte	1 byte	Bus number	Read	0x00
41	1 byte	1 byte	Subordinate bus number	Read	0x00
42	1 byte	1 byte	Disconnect counter	Read	0x00
44	2 bytes	2 bytes	Special cycle address	Read	0x0000
70	2 bytes	1 or 2 bytes	Power management configuration	Read/write	0x00
80–87	8 bytes	1, 2, or 4 bytes	Memory starting address	Read/write	
88–8F	8 bytes	1, 2, or 4 bytes	Extended memory starting address	Read/write	
90–97	8 bytes	4 bytes	Memory ending address	Read/write	
98–9F	8 bytes	1, 2, or 4 bytes	Extended memory ending address	Read/write	

Table 10. MPC105 Configuration Registers (Continued)

Address Offset	Register Size	Program Accessible Size	Register	Register Access	Reset Value
A0	1 byte	1 byte	Memory enable	Read/write	
A8	4 bytes	1, 2, or 4 bytes	Processor interface configuration 1	Read/write	0xFF00_0410
AC	4 bytes	1, 2, or 4 bytes	Processor interface configuration 2	Read/write	0x000C_060C
BA	1 byte	1 byte	Alternate OS visible parameters 1	Read/write	0x04
BB	1 byte	1 byte	Alternate OS visible parameters 2	Read/write	0x00
C0	1 byte	1 byte	Error enabling 1	Read/write	0x01
C1	1 byte	1 byte	Error detection 1	Read/bit-reset	0x00
C3	1 byte	1 byte	60x bus error status	Read/bit-reset	0x00
C4	1 byte	1 byte	Error enabling 2	Read/write	0x00
C5	1 byte	1 byte	Error detection 2	Read/bit-reset	0x00
C7	1 byte	1 byte	PCI bus error status	Read/bit-reset	0x00
C8–CB	4 byte	4 bytes	60x/PCI error address	Read	0x00
F0	4 bytes	1, 2, or 4 bytes	Memory control configuration 1	Read/write	0xFF*n*2_0000
F4	4 bytes	1, 2, or 4 bytes	Memory control configuration 2	Read/write	0x0000_0003
F8	4 bytes	1, 2, or 4 bytes	Memory control configuration 3	Read/write	0x0000_0000
FC	4 bytes	1, 2, or 4 bytes	Memory control configuration 4	Read/write	0x0010_0000

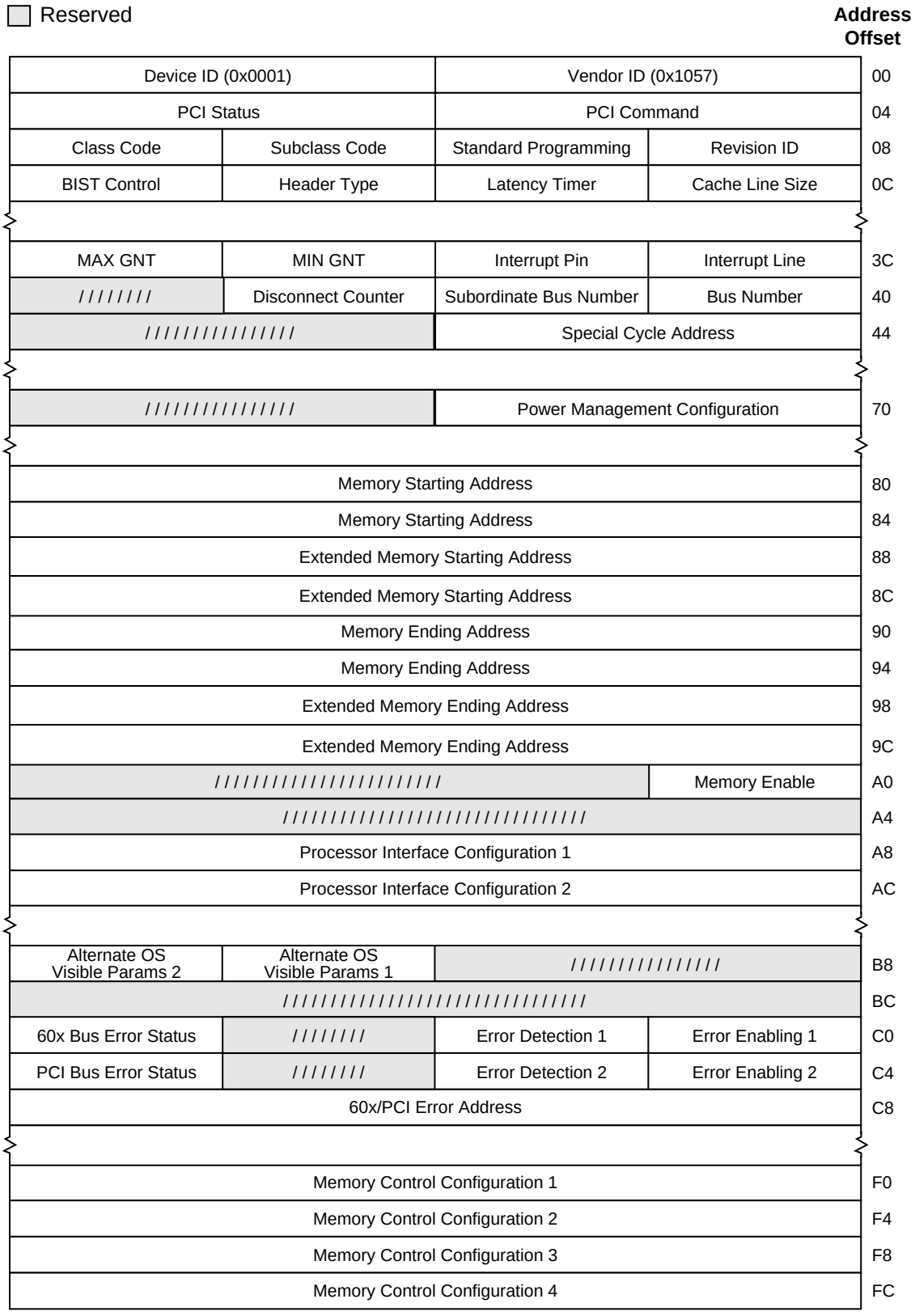

Figure 3. MPC105 Configuration Space

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