PowerPC™

Advance Information
MPC105 PCI Bridge/Memory Controller Hardware Specifications

The MPC105 provides a PowerPC™ reference platform compliant-bridge between the PowerPC microprocessor family and the Peripheral Component Interconnect (PCI) bus. This document contains pertinent physical characteristics of the MPC105. For functional characteristics refer to the *MPC105 PCI Bridge/Memory Controller User's Manual*.

This document contains the following topics:

In this document, the term "60x" is used to denote a 32-bit microprocessor from the PowerPC Architecture™ family. 60x processors implement the PowerPC architecture as it is specified for 32-bit addressing, which provides 32-bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits (single-precision and double-precision).

105 Hardware Specifications

Ⓜ MOTOROLA

1.1 MPC105 Overview

The MPC105 provides a PowerPC reference platform-compliant bridge between PowerPC 601™, PowerPC 603™, and PowerPC 604™ microprocessors and the PCI bus. PCI support allows system designers to rapidly design systems using peripherals already designed for PCI and the other standard interfaces available in the personal computer hardware environment. The MPC105 integrates secondary cache control and a high-performance memory controller that supports DRAM, synchronous DRAM (SDRAM), ROM, and Flash ROM. The MPC105 uses an advanced, 3.3 V CMOS process technology and is fully compatible with TTL devices.

The MPC105 supports a programmable interface to a variety of PowerPC microprocessors operating at various bus speeds. The MPC105's 60x interface allows for a variety of system configurations by providing support for either a second processor or a secondary (L2) cache. The L2 cache control unit generates the arbitration and support signals necessary to maintain a write-through or write-back lookaside cache.

The MPC105's PCI interface is designed to connect the processor and memory system to the PCI local bus without the need for "glue" logic. The MPC105 acts as both a master and slave device on the PCI bus.

The memory interface controls processor and PCI interactions to main memory. It is capable of supporting a variety of DRAM or SDRAM, and ROM or Flash ROM configurations.

The MPC105 provides hardware support for four levels of power reduction—nap, doze, sleep, and suspend. The MPC105's design is fully static, allowing internal logic states to be preserved during all power saving modes.

1.1.1 MPC105 Features

Major features of the MPC105 are as follows:

- Processor interface
    - 60x processors supported at a wide range of frequencies
    - 32-bit address bus
    - Configurable 64- or 32-bit data bus
    - Accommodates an upgrade of either an external L2 cache or a secondary processor
    - Arbitration for secondary processor on-chip
    - Full memory coherency supported
    - Pipelining of 60x accesses
    - Store gathering on 60x-to-PCI writes
- Secondary (L2) cache control
    - Configurable for write-through or write-back operation
    - 256K, 512K, 1M sizes
    - Up to 4 Gbytes of cacheable space
    - Direct-mapped
    - Parity supported
    - Supports external byte decode or on-chip byte decode for write enables
    - Programmable timing supported
    - Synchronous burst and asynchronous SRAMs supported

Preliminary/Subject to Change without Notice

- PCI interface

  — Compliant with *PCI Local Bus Specification, Revision 2.0*

  — Supports PCI interlocked accesses to memory using $\overline{\text{LOCK}}$ signal and protocol

  — Supports accesses to all PCI address spaces

  — Selectable big- or little-endian operation

  — Store gathering on PCI writes to memory

  — Selectable memory prefetching of PCI read accesses

  — Only one external load presented by the MPC105 to the PCI bus

  — PCI configuration registers

  — Interface operates at 16–33 MHz

  — Data buffering (in/out)

  — Parity supported

  — 3.3 V/5.0 V compatible

- Concurrent transactions on 60x and PCI buses supported

- Memory interface

  — Programmable timing supported

  — Supports either DRAM or SDRAM

  — High bandwidth (64-bit) data bus

  — Supports self-refreshing DRAM in sleep and suspend modes

  — Supports 1 to 8 banks built of x1, x4, x8, x9, x16, or x18 DRAMs

  — Supports PowerPC reference platform-compliant contiguous or discontiguous memory maps

  — 1 Gbyte of RAM space, 16 Mbytes of ROM space

  — Supports 8-bit asynchronous ROM or 32-/64-bit burst-mode ROM

  — Supports writing to Flash ROM

  — Configurable external buffer control logic

  — Parity supported

  — TTL compatible

- Power management

  — Fully-static 3.3 V CMOS design

  — Supports 60x nap, doze, and sleep power management modes, and suspend mode

- IEEE 1149.1-compliant, JTAG boundary-scan interface

- 304-pin ball grid array (BGA) package

1.2 General Parameters

The following list provides a summary of the general parameters of the MPC105.

Technology	0.5 µm CMOS, four-layer metal
Chip size	6.69 mm x 5.82 mm (38.9 mm^2)
Chip performance	25 MHz, 33.33 MHz, 50 MHz, and 66.67 MHz
Package	Surface mount 304-pin C4 ceramic ball grid array (CBGA)
Power supplies	3.3 V ± 5%
Maximum input rating	5.0 V ± 10%

Preliminary/Subject to Change without Notice

1.3 MPC105 Electrical and Thermal Characteristics

This section provides both the AC and DC electrical specifications and thermal characteristics for the MPC105. The following specifications are preliminary and subject to change without notice. For the most recent specifications, contact your local Motorola sales office.

1.3.1 DC Electrical Characteristics

Table 1 and Table 2 provide the absolute maximum rating and thermal characteristics for the MPC105.

Table 1. Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply voltage	Vdd	−0.3 to 3.6	V
Input voltage	V_{in}	−0.3 to 5.5	V
Junction temperature	T_J	0 to 105	°C
Storage temperature range	T_{stg}	−55 to 150	°C

Notes:
1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** Input voltage must not be greater than the supply voltage by more than 2.5 V at all times including during power-on reset.

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Rating
CBGA package thermal resistance, junction to case	θ_{JC}	0.133	°C/W

Note: $T_J = T_A + P_D \times \theta_{JA}$ where $\theta_{JA} = \theta_{JC} + \theta_{CA}$, see Section 1.6, "System Design Information," for additional information.

Table 3 provides the DC electrical characteristics for the MPC105.

Table 3. DC Electrical Specifications

Vdd = 3.3 ± 5% Vdc, GND = 0 Vdc

Characteristic	Symbol	Min	Max	Unit
Input high voltage (all inputs except SYSCLK)	V_{IH}	2	5.5	V
Input low voltage (all inputs except SYSCLK)	V_{IL}	GND	0.8	V
SYSCLK input high voltage	CV_{IH}	2.4	5.5	V
SYSCLK input low voltage	CV_{IL}	GND	0.4	V
Input leakage current	I_{in}	—	10	μA
Hi-Z (off-state) leakage current	I_{TSI}	—	10	μA
Output high voltage, $I_{OH} = 18$ mA	V_{OH}	2.4	—	V

Preliminary/Subject to Change without Notice

Table 3. DC Electrical Specifications (Continued)

Vdd = 3.3 ± 5% Vdc, GND = 0 Vdc

Characteristic	Symbol	Min	Max	Unit
Output low voltage, $I_{OL} = 14$ mA	V_{OL}	—	0.5	V
Capacitance, $V_{in} = 0$ V, f = 1 MHz[1]	C_{in}	—	7	pF

Note:
    1. Capacitance is periodically sampled rather than 100% tested.

Table 4 provides the power dissipation for the MPC105.

Table 4. Power Dissipation[1]

SYSCLK/Internal Clock Frequency (MHz)					
Power Management Mode	25/25	33.33/33.33	25/50	33.33/66.67	Unit
Max Values (Vdd = 3.47 V)					
Full-on mode	0.60	0.8	1.30	1.70	W
Doze mode	TBD	TBD	TBD	TBD	mW
Nap mode	TBD	TBD	TBD	TBD	mW
Sleep mode [2]	140	180	220	260	mW
Suspend mode [3]	50	50	90	90	mW
Typical Values (Vdd = 3.3 V)					
Full-on mode	0.40	0.50	0.70	0.90	W
Doze mode	TBD	TBD	TBD	TBD	mW
Nap mode	TBD	TBD	TBD	TBD	mW
Sleep mode[2]	70	110	140	180	mW
Suspend mode [3]	30	30	60	60	mW

Notes:
    1. Power dissipation for common system configurations assuming 50 pF loads
    2. Power saving modes assume system clock off.
    3. Suspend power saving mode assumes system clock off and PLL in clock bypass mode.

1.3.2 AC Electrical Characteristics

This section provides the clock AC electrical characteristics for the MPC105.

1.3.2.1 Input AC Specifications

Table 5 provides the clock AC timing specifications as defined in Figure 1. These specifications are for operation between 16.67 and 33.33 MHz bus clock (SYSCLK) frequencies.

Preliminary/Subject to Change without Notice

Table 5. Clock AC Timing Specifications

Vdd = 3.3 ± 5% Vdc, GND = 0 Vdc

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of operation	16.67	33.33	MHz	
1	SYSCLK cycle time	30.0	60.0	ns	
2,3	SYSCLK rise and fall time	—	2.0	ns	1
4	SYSCLK duty cycle measured at 1.4 V	40.0	60.0	%	
5a	SYSCLK pulse width high measured at 1.4 V	12	18	ns	2
5b	SYSCLK pulse width low measured at 1.4 V	12	18	ns	2
6	SYSCLK frequency stability	—	1000	ppm	
7	SYSCLK jitter	—	±150	ps	3
8	MPC105 internal PLL relock time	—	100	µs	4
9	Phase-lock loop VCO operating range	120	200	MHz	5

Notes:
1. Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4 V.
2. Specification value is at maximum frequency of operation.
3. Cycle-to-Cycle Jitter
4. Relock timing is guaranteed by design and is not tested.
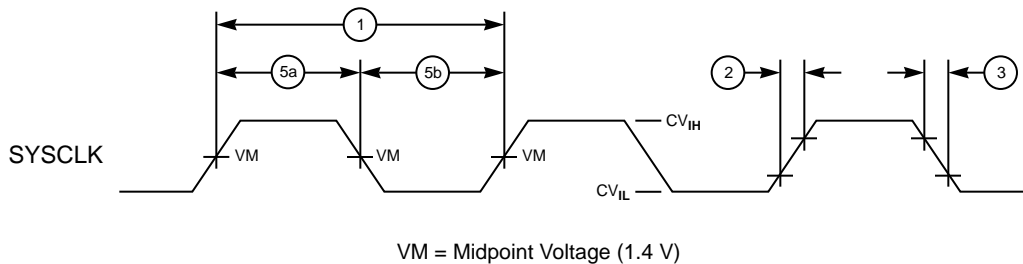5. For configuration of the VCO, see Table 10.

VM = Midpoint Voltage (1.4 V)

Figure 1. SYSCLK Input Timing Diagram

1.3.2.2 Input AC Specifications

Table 6 provides the input AC timing specifications for the MPC105 as defined in Figure 2 and Figure 3. These specifications are for operation between 16.67 and 33.33 MHz bus clock (SYSCLK) frequencies.

Preliminary/Subject to Change without Notice

Table 6. Input AC Timing Specifications

Vdd = 3.3 ± 5% Vdc, GND = 0 Vdc

Num	Characteristic	Min	Max	Unit	Notes
10	A0–A31, PAR0–PAR7, TT0–TT4, $\overline{AACK}$, $\overline{TA}$, $\overline{GBL}$, $\overline{CI}$, $\overline{WT}$, TV input valid to SYSCLK (input setup)	4.0	—	ns	1
11	DL0–DL31, DH0–DH31, $\overline{TBST}$, TSIZ0–TSIZ2. Input valid to SYSCLK (input setup)	2.5	—	ns	2
12	$\overline{HIT}$, $\overline{TS}$, $\overline{ARTRY}$, $\overline{BR0}$, $\overline{BR1}$, $\overline{XATS}$ input signals valid to SYSCLK (input setup)	5.0	—	ns	3
13	Mode select inputs valid to $\overline{HRST}$ (input setup)	3 * t_{SYS}	—	ns	4, 5
14	$\overline{LOCK}$, $\overline{FLSHREQ}$, $\overline{ISA\_MASTER}$, $\overline{C/BE0}$–$\overline{C/BE3}$, PAR, $\overline{TRDY}$, $\overline{IRDY}$, $\overline{FRAME}$, $\overline{STOP}$, $\overline{DEVSEL}$, $\overline{PERR}$, $\overline{SERR}$, AD0–AD31 input signals valid to SYSCLK (input setup)	7.0	—	ns	6
15	PCI point-to-point signals input signals valid to SYSCLK (input setup)	10.0	—	ns	7
16	SYSCLK to inputs invalid (input hold)	1.0	—	ns	1–3,
17	SYSCLK to PCI inputs invalid (input hold)	0.0	—	ns	6,7
18	$\overline{HRST}$ to mode select inputs invalid (input hold)	1.0	—	ns	4, 8

Notes:

All input specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V of the rising edge of SYSCLK. Processor and memory interface signals are specified from the rising edge of the processor and memory bus clock, which is the same as SYSCLK in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of SYSCLK). Both input and output timings are measured at the pin.

1. Inputs are composed of the following processor interface signals—A0–A31, PAR0–PAR7, TT0–TT4, $\overline{AACK}$, $\overline{TA}$, $\overline{GBL}$, $\overline{CI}$, $\overline{WT}$, TV.
2. Inputs are composed of the following processor interface signals—DL0–DL31, DH0–DH31, $\overline{TBST}$, TSIZ0–TSIZ2.
3. Inputs are composed of the following processor and L2 interface signals—$\overline{HIT}$, $\overline{TS}$, $\overline{ARTRY}$, $\overline{BR0}$, $\overline{BR1}$, $\overline{XATS}$.
4. The setup and hold time is with respect to the rising edge of $\overline{HRST}$; see Figure 3. The following signals encompass the mode (or configuration) pins for MPC105—$\overline{RCS0}$, $\overline{BCTL0}$, DL0, $\overline{XATS}$, and FNR.
5. t_{SYS} is the period of the external clock (SYSCLK) in nanoseconds
6. Inputs are composed of all PCI bus signals: $\overline{LOCK}$, $\overline{FLSHREQ}$, $\overline{ISA\_MASTER}$, $\overline{C/BE0}$–$\overline{C/BE3}$, PAR, $\overline{TRDY}$, $\overline{IRDY}$, $\overline{FRAME}$, $\overline{STOP}$, $\overline{DEVSEL}$, $\overline{PERR}$, $\overline{SERR}$, AD0–AD31.
7. Inputs are composed of all PCI point-to-point signals. $\overline{GNT}$ has a setup time of 10.0 ns for a 33 MHZ PCI clock.
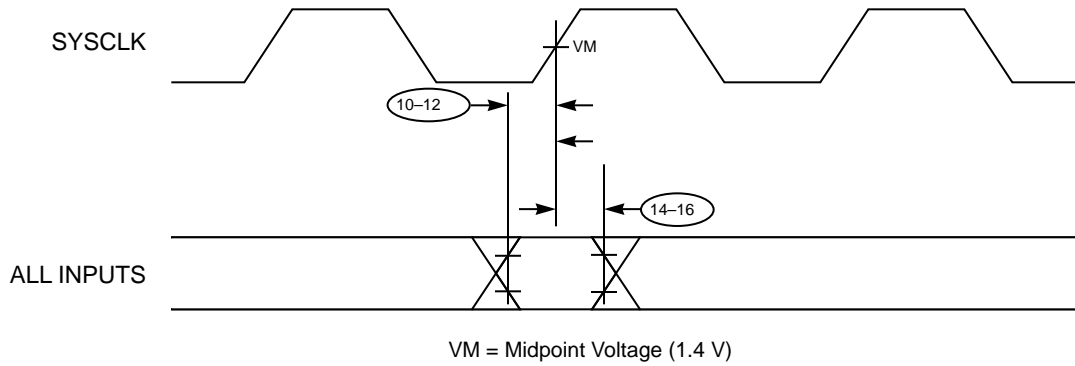8. Guaranteed by design, not tested.

Preliminary/Subject to Change without Notice

VM = Midpoint Voltage (1.4 V)

Figure 2. Input Timing Diagram
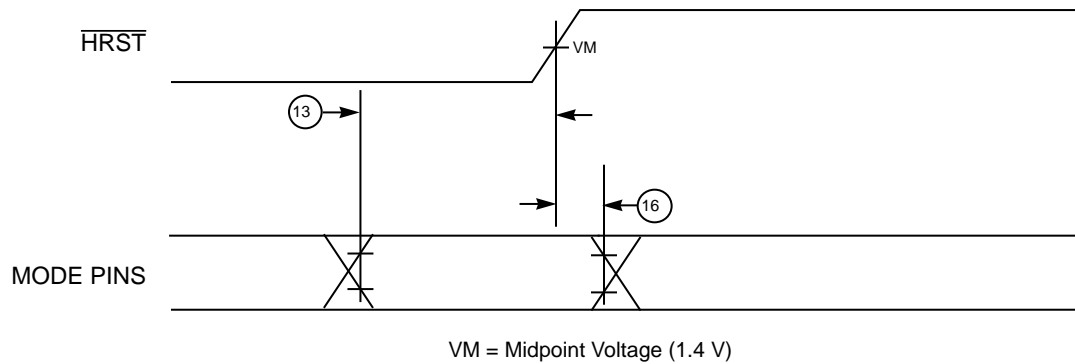

VM = Midpoint Voltage (1.4 V)

Figure 3. Mode Select Input Timing Diagram

1.3.2.3 Output AC Specifications

Table 7 provides the output AC timing specifications for the MPC105 as defined in Figure 4. These specifications are for operation between 16.67 MHz and 33.33 MHz bus clock (SYSCLK) frequencies.

Table 7. Output AC Timing Specifications

Vdd = 3.3 ± 5% Vdc, GND = 0 Vdc

Num	Characteristic	Min	Max	Unit	Notes
19	SYSCLK to output driven (output enable time)	2.0	—	ns	
20	SYSCLK to output valid (for PCI bus signals)	—	11	ns	1, 2, 3
21	SYSCLK to output valid (for PCI point-to-point signals)	—	12	ns	1, 2, 4
22	SYSCLK to output valid (for $\overline{TS}$, $\overline{ARTRY}$, all non-PCI signals except TALE, $\overline{BAA}$, $\overline{RAS}/\overline{CS0}$–$\overline{RAS}/\overline{CS7}$, $\overline{CAS}/DQM0$–$\overline{CAS}/DQM7$)	—	8.0	ns	1, 2, 7
23	SYSCLK to output valid (for TALE, $\overline{BAA}$)	—	10.0	ns	1, 2
24	SYSCLK to output valid (for $\overline{RAS}/\overline{CS0}$–$\overline{RAS}/\overline{CS7}$, $\overline{CAS}/DQM0$–$\overline{CAS}/DQM7$)	—	9.0	ns	1, 2

Preliminary/Subject to Change without Notice

Table 7. Output AC Timing Specifications (Continued)

Vdd = 3.3 ± 5% Vdc, GND = 0 Vdc

Num	Characteristic	Min	Max	Unit	Notes
25	SYSCLK to output invalid (output hold)	0.0	—	ns	
26	SYSCLK to output high impedance (all except $\overline{ARTRY}$)	—	8.0	ns	
27	SYSCLK to $\overline{ARTRY}$ high impedance before precharge (output hold)	—	8.0	ns	
28	SYSCLK to $\overline{ARTRY}$ precharge enable (1X, 2X, PLL mode)	$0.4 * t_{SYS}$ + 2.0	—	ns	5, 6
29	Precharge width for $\overline{ARTRY}$	1.0		t_{SYS}	5, 6
30	SYSCLK to $\overline{ARTRY}$ high impedance after precharge (1X, 2X PLL modes)	—	$1.5 * t_{SYS}$ + 8.0	ns	5

Notes:

All output specifications are measured from the TTL level (0.8 V or 2.0 V) of the signal in question to the 1.4 V of the rising edge of SYSCLK. Processor and memory interface signals are specified from the rising edge of the processor and memory bus clock, which is the same as SYSCLK in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of SYSCLK). Both input and output timings are measured at the pin.

1. All output specifications are measured from the 1.4 V of the rising edge of SYSCLK to the TTL level (0.8 V or 2.0 V) of the signal in question. The output timings are measured at the pin.
2. Maximum timing specifications assume C_L = 50 pF.
3. PCI bus signals are composed of the following signals—$\overline{LOCK}$, $\overline{MEMACK}$, $\overline{ISA\_MASTER}$, $\overline{C/BE0}$–$\overline{C/BE3}$, PAR, $\overline{TRDY}$, $\overline{FRAME}$, $\overline{STOP}$, $\overline{DEVSEL}$, $\overline{PERR}$, $\overline{SERR}$, and AD0–AD31.
4. PCI point-to-point signals are composed of the $\overline{GNT}$ signal.
5. t_{SYS} is the period of the external bus clock (SYSCLK) in nanoseconds. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. These specifications are nominal values.
7. Shared outputs, $\overline{TS}$ and $\overline{ARTRY}$, require pull-up resistors to hold them negated when there is no bus master driving.
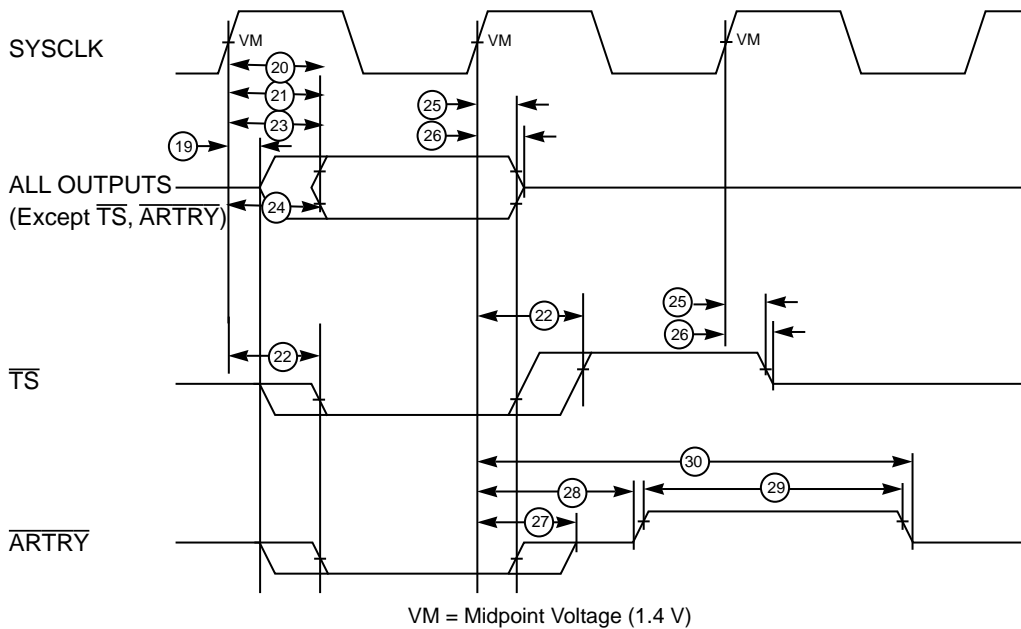
VM = Midpoint Voltage (1.4 V)

Figure 4. Output Timing Diagram

1.3.3 JTAG AC Timing Specifications

Table 8 provides the JTAG AC timing specifications.

Table 8. JTAG AC Timing Specifications (Independent of SYSCLK)

Num	Characteristic	Min	Max	Unit
	TCK frequency of operation	0	25	MHz
1	TCK cycle time	40	—	ns
2	TCK clock pulse width measured at 1.5 V	20	—	ns
3	TCK rise and fall times	0	3	ns
4	$\overline{\text{TRST}}$ setup time to TCK falling edge	10	—	ns
5	$\overline{\text{TRST}}$ assert time	10	—	ns
6	Boundary-scan input data setup time	5	—	ns
7	Boundary-scan input data hold time	15	—	ns
8	TCK to output data valid	0	30	ns
9	TCK to output high impedance	0	30	ns
10	TMS, TDI data setup time	5	—	ns
11	TMS, TDI data hold time	15	—	ns
12[1]	TCK to TDO data valid	0	15	ns

Preliminary/Subject to Change without Notice

Table 8. JTAG AC Timing Specifications (Independent of SYSCLK) (Continued)

Num	Characteristic	Min	Max	Unit
13[1]	TCK to TDO high impedance	0	15	ns

Note:
　　1. Load capacitance = 20 pF

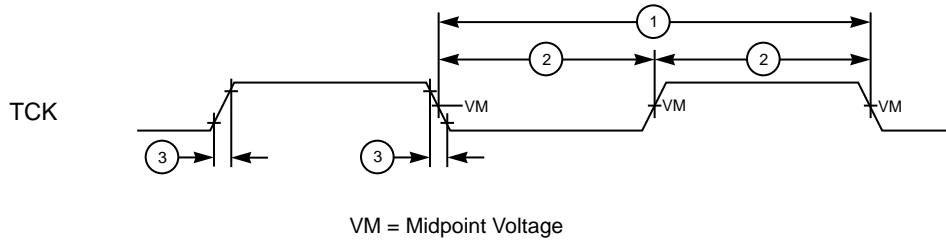Figure 5 provides the JTAG clock input timing diagram.

VM = Midpoint Voltage

Figure 5. Clock Input Timing Diagram

Figure 6 provides the $\overline{\text{TRST}}$ timing diagram.
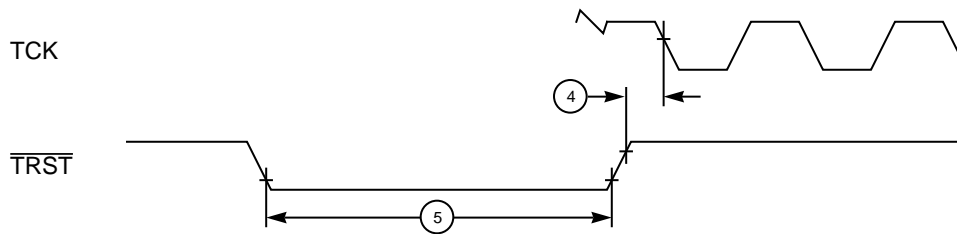
Figure 6. $\overline{\text{TRST}}$ Timing Diagram

Figure 7 provides the boundary-scan timing diagram.
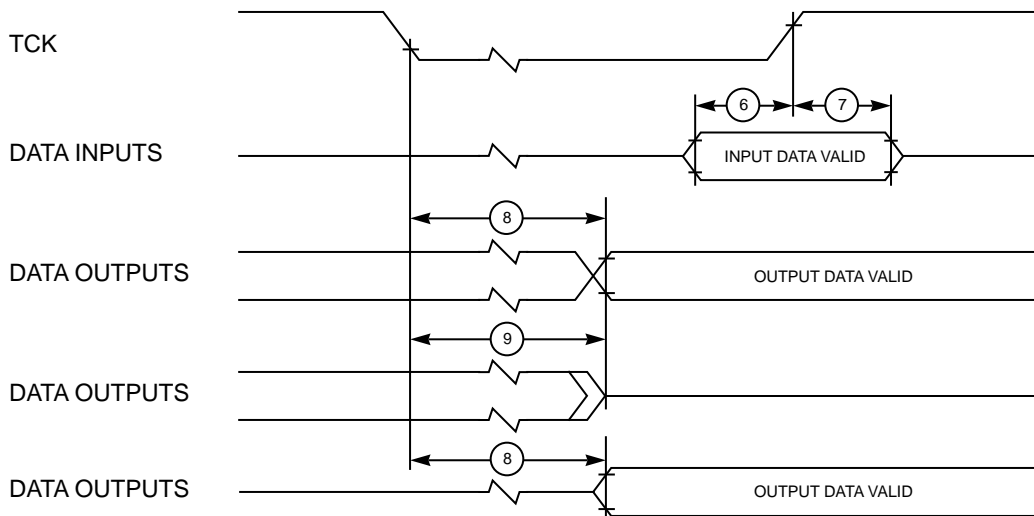
Figure 7. Boundary-Scan Timing Diagram

Preliminary/Subject to Change without Notice

Figure 8 provides the test access port timing diagram.
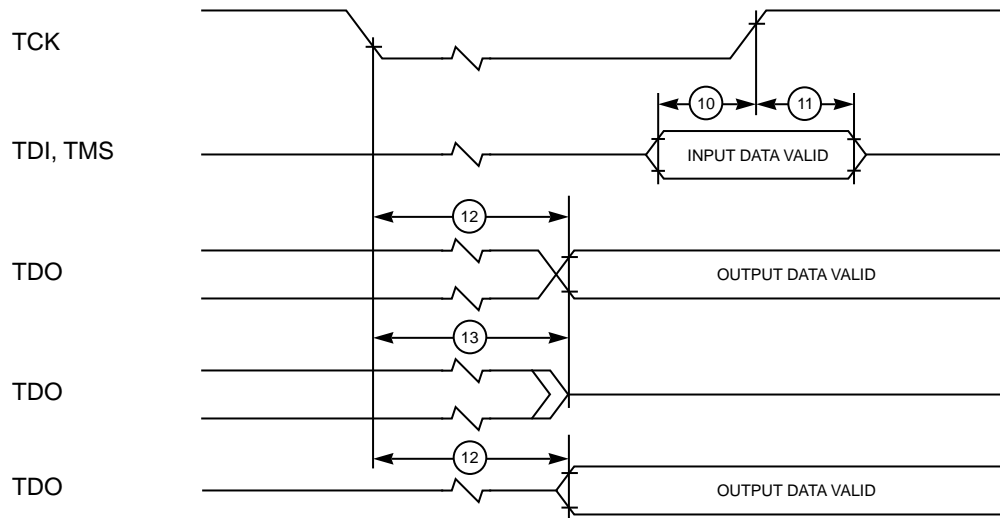
Figure 8. Test Access Port Timing Diagram

Preliminary/Subject to Change without Notice

1.4 MPC105 Pinout Diagram

Figure 9 contains the pin assignments for the MPC105.

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
W	DL26	DL28	DL30	DH31	DH29	DH27	DH25	DH23	DH21	DH19	DH17	DH15	DH13	DH11	DH9	DH7	W
V	DL24	DL27	DL29	DL31	DH30	DH28	DH26	DH24	DH20	DH18	DH16	DH14	DH12	DH10	DH8	DL22	V
U	MA0	DL23	DL25	DL14	PLL2	PLL0	DL12	DL10	DL4	DL2	DL0	DOE	DBG1	DH6	DL21	DL20	U
T	MA1	WE	DH0	DL15	PLL3	PLL1	DL13	DL11	DL3	DL1	TV	TALOE	HIT	BR1	DL19	TALE	T
R	MA2	RCS0	DH2	DH1	DL16	Vss	Vdd	DL9	DL5	Vss	Vdd	TWE	BG1	ADS	A0	TS	R
P	MA4	MA3	DH4	DH3	Vss	Vdd	Vss	DL8	DL6	Vdd	Vss	Vdd	BAA	DWE	A1	XATS	P
N	MA5	DWE7	DL17	DH5	Vdd	Vss	Vdd	DL7	DH22	Vss	Vdd	Vss	DWE2	CI	A2	TA	N
M	MA7	MA6	RAS/CS0	DL18	Vss	Vdd	Vss	NC	NC	Vdd	Vss	Vdd	WT	GBL	A3	TT4	M
L	HRST	MA8	QACK	RAS/CS1	Vdd	DWE3	RAS/CS5	Vss	Vdd	Vss	SYSCLK	DBG0	TBST	BR0	A4	TT3	L
K	MA10	MA9	RAS/CS3	RAS/CS2	RAS/CS4	RAS/CS7	Vdd	AVdd	Vss	Vdd	A9	A8	A7	BG0	A5	TT2	K
J	MA11	CAS/DQM0	SDRAS	DWE0	RAS/CS6	MCP	DWE4	Vss	Vdd	Vss	A11	A6	A13	A12	A10	TEA	J
H	QREQ	CAS/DQM1	SUSPEND	TRST	Vss	DWE6	DWE5	NC	NC	Vdd	Vss	Vdd	A15	A14	A16	TT1	H
G	CAS/DQM2	RTC	CAS/DQM4	CAS/DQM5	Vdd	LSSD_MODE	Vdd	PAR	LOCK	Vss	Vdd	Vss	TSIZ1	TSIZ0	A17	TT0	G
F	BCTL0	BCTL1	CAS/DQM6	TCK	Vss	Vdd	Vss	PERR	DEVSEL	Vdd	Vss	Vdd	A21	TSIZ2	ARTRY	A18	F
E	CAS/DQM3	NMI	CAS/DQM7	SDCAS	TDO	Vss	Vdd	SERR	IRDY	Vss	Vdd	A31	A29	A22	A20	A19	E
D	PAR0	PAR1	TMS	FOE/RCS1	AD28	AD24	AD21	AD17	AD14	AD10	C/BE0	AD4	AD0	A30	AACK	A23	D
C	PAR2	PAR3	PAR5	AD30	AD26	AD23	AD19	C/BE2	C/BE1	AD12	AD8	AD6	AD2	A27	A25	A24	C
B	PAR4	PAR7	AD1	TDI	AD7	AD11	AD15	TRDY	AD18	AD22	AD25	AD29	REQ	ISA_MASTER	A28	A26	B
A	PAR6	GNT	AD3	AD5	AD9	AD13	FRAME	STOP	AD16	AD20	C/BE3	AD27	AD31	FLSHREQ	MEMACK		A
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 9. Pin Assignments

Figure 10 provides a key to the shading in Figure 9.

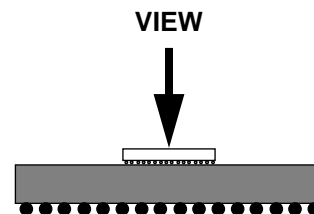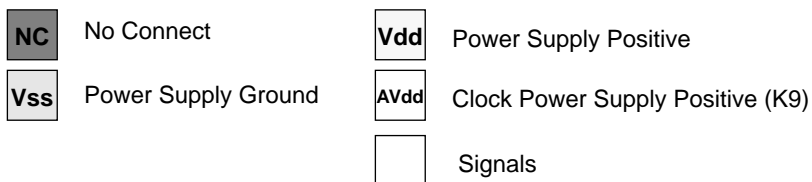| NC	No Connect		Vdd	Power Supply Positive
Vss	Power Supply Ground		AVdd	Clock Power Supply Positive (K9)
				Signals

VIEW

Figure 10. Pin Assignments Shading Key

Table 9 provides the pinout listing for the MPC105.

Table 9. Pinout Listing[1]

Signal Name	Pin Number	Active	I/O
60x Processor Interface Signals			
A0–A31	R2, P2, N2, M2, L2, K2, J5, K4, K5, K6, J2, J6, J3, J4, H3, H4, H2, G2, F1, E1, E2, F4, E3, D1, C1, C2, B1, C3, B2, E4, D3, E5	High	I/O
$\overline{AACK}$	D2	Low	I/O
$\overline{ARTRY}$	F2	Low	I/O
$\overline{BR0}$	L3	Low	Input
$\overline{BG0}$	K3	Low	Output
$\overline{BR1}$ ($\overline{DIRTY\_IN}$)	T3	Low	Input
$\overline{BG1}$ ($\overline{DIRTY\_OUT}$)	R4	Low	Output
$\overline{CI}$	N3	Low	I/O
$\overline{DBG0}$	L5	Low	Output
$\overline{DBG1}$ ($\overline{TOE}$)	U4	Low	Output
DH0–DH31	T14, R13, R14, P13, P14, N13, U3, W1, V2, W2, V3, W3, V4, W4, V5, W5, V6, W6, V7, W7, V8, W8, N8, W9, V9, W10, V10, W11, V11, W12, V12, W13	High	I/O
DL0–DL31	U6, T7, U7, T8, U8, R8, P8, N9, P9, R9, U9, T9, U10, T10, U13, T13, R12, N14, M13, T2, U1, U2, V1, U15, V16, U14, W16, V15, W15, V14, W14, V13	High	I/O
$\overline{GBL}$	M3	Low	I/O
$\overline{TA}$	N1	Low	I/O
$\overline{TBST}$	L4	Low	I/O
$\overline{TEA}$	J1	Low	Output
$\overline{TS}$	R1	Low	I/O
TSIZ0–TSIZ2	G3, G4, F3	High	I/O
TT0–TT4	G1, H1, K1, L1, M1	High	I/O
$\overline{WT}$	M4	Low	I/O
$\overline{XATS}$	P1	Low	Input

Preliminary/Subject to Change without Notice

Table 9. Pinout Listing[1] (Continued)

Signal Name	Pin Number	Active	I/O
PCI Interface Signals			
$\overline{C/BE0}$–$\overline{C/BE3}$	D6, C8, C9, A6	Low	I/O
$\overline{DEVSEL}$	F8	Low	I/O
$\overline{FLSHREQ}$	A3	Low	Input
$\overline{FRAME}$	A10	Low	I/O
$\overline{IRDY}$	E8	Low	I/O
$\overline{ISA\_MASTER}$	B3	Low	Input
$\overline{LOCK}$	G8	Low	Input
$\overline{MEMACK}$	A2	Low	Output
AD0–AD31	D4, B14, C4, A14, D5, A13, C5, B12, C6, A12, D7, B11, C7, A11, D8, B10, A8, D9, B8, C10, A7, D10, B7, C11, D11, B6, C12, A5, D12, B5, C13, A4	High	I/O
PAR	G9	High	I/O
$\overline{GNT}$	A15	Low	Input
$\overline{REQ}$	B4	Low	Output
$\overline{PERR}$	F9	Low	I/O
$\overline{SERR}$	E9	Low	I/O
$\overline{STOP}$	A9	Low	I/O
$\overline{TRDY}$	B9	Low	I/O
L2 Cache Interface Signals			
$\overline{ADS}$	R3	Low	Output
$\overline{BAA}$	P4	Low	Output
$\overline{DIRTY\_IN}$ ($\overline{BR1}$)	T3	Low	Input
$\overline{DIRTY\_OUT}$ ($\overline{BG1}$)	R4	Low	Output
$\overline{DOE}$	U5	Low	Output
$\overline{DWE0}$ (FNR)	J13	Low	Output
$\overline{DWE}$ ($\overline{DWE1}$)	P3	Low	Output
$\overline{DWE2}$	N4	Low	Output

Preliminary/Subject to Change without Notice

Table 9. Pinout Listing[1] (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{DWE3}$ (CKO)	L11	Low	Output
$\overline{DWE4}$	J10	Low	Output
$\overline{DWE5}$	H10	Low	Output
$\overline{DWE6}$	H11	Low	Output
$\overline{DWE7}$ (CKE)	N15	Low	Output
$\overline{HIT}$	T4	Low	Input
TALE	T1	High	Output
$\overline{TALOE}$	T5	Low	Output
$\overline{TOE}/\overline{DBG1}$	U4	Low	Output
TV	T6	High	I/O
$\overline{TWE}$	R5	Low	Output
Memory Interface Signals			
$\overline{BCTL0}$	F16	Low	Output
$\overline{BCTL1}$	F15	Low	Output
$\overline{CAS}/DQM0$–$\overline{CAS}/DQM7$	J15, H15, G16, E16, G14, G13, F14, E14	Low	Output
CKE/$\overline{DWE7}$	N15	High	Output
$\overline{FOE}/\overline{RCS1}$	D13	Low	Output
MA0–MA11 (AR0–AR11)	U16, T16, R16, P15, P16, N16, M15, M16, L15, K15, K16, J16	High	Output
PAR0–PAR7 (AR0–AR7)	D16, D15, C16, C15, B16, C14, A16, B15	High	I/O
$\overline{RAS}/\overline{CS0}$–$\overline{RAS}/\overline{CS7}$	M14, L13, K13, K14, K12, L10, J12, K11	Low	Output
$\overline{RCS0}$	R15	Low	I/O
RTC	G15	High	Input
$\overline{SDCAS}$	E13	Low	Output
$\overline{SDRAS}$	J14	Low	Output
$\overline{WE}$	T15	Low	Output

105 Hardware Specifications

Preliminary/Subject to Change without Notice

Table 9. Pinout Listing[1] (Continued)

Signal Name	Pin Number	Active	I/O
Interrupt, Clock, and Power Management Signals			
CK0/$\overline{\text{DWE3}}$	L11	High	Output
$\overline{\text{HRST}}$	L16	Low	Input
$\overline{\text{MCP}}$	J11	Low	Output
NMI	E15	High	Input
$\overline{\text{QACK}}$	L14	Low	Output
$\overline{\text{QREQ}}$	H16	Low	Input
SYSCLK	L6	Clock	Input
$\overline{\text{SUSPEND}}$	H14	Low	Input
Test/Configuration Signals			
FNR/$\overline{\text{DWE0}}$	J13	High	Input
PLL0–PLL3	U11, T11, U12, T12	High	Input
TCK	F13	Clock	Input
TDI	B13	High	Input
TDO	E12	High	Output
TMS	D14	High	Input
$\overline{\text{TRST}}$	H13	Low	Input
Power and Ground Signals			
AVdd	K9	High	Clock Power
Vdd	E10, E6, F11, F5, F7, G10, G12, G6, H5, H7, K10, K7, L12, M11, M5, M7, N10, N12, N6, P11, P5, P7, R10, R6, J8, L8	High	Power
$\overline{\text{LSSD\_MODE}}$ [2]	G11	Low	Input
Vss	E11, E7, F10, F12, F6, G5, G7, H12, H6, J7, L7, M10, M12, M6, N11, N5, N7, P10, P12, P6, R11, R7, K8, J9, L9	Low	Ground
NC	H8, H9, M8, M9	—	—

Note:

1. Some signals have dual functions and are shown more than once in this table.

2. This test signal is for factory use only. It must be pulled up to Vdd for normal machine operation.

Preliminary/Subject to Change without Notice

1.5 MPC105 Package Description

The following sections provide the package parameters and the mechanical dimensions for the MPC105.

1.5.1 Package Parameters

The package parameters are as provided in the following list. The package type is a 21 mm x 25 mm, 304-pin C4 ceramic ball grid array (CBGA).

Package outline	21 mm x 25 mm
Interconnects	303
Pitch	1.27 mm
Solder attach	63/37 Sn/Pb
Solder balls	10/90 Sn/Pb
Maximum module height	3.16 mm
Co-planarity specification	0.20 mm

Preliminary/Subject to Change without Notice

1.5.2 Mechanical Dimensions

Figure 11 shows the mechanical dimensions for the MPC105.

	MIN	MAX
A	25.0 BASIC	
B	21.0 BASIC	
C	2.3	3.16
D	0.82	0.93
G	1.27 BASIC	
H	0.79	0.99
K	0.635 BASIC	
N	5.8	6.3
P	6.7	6.9

Note: All measurements are in mm.
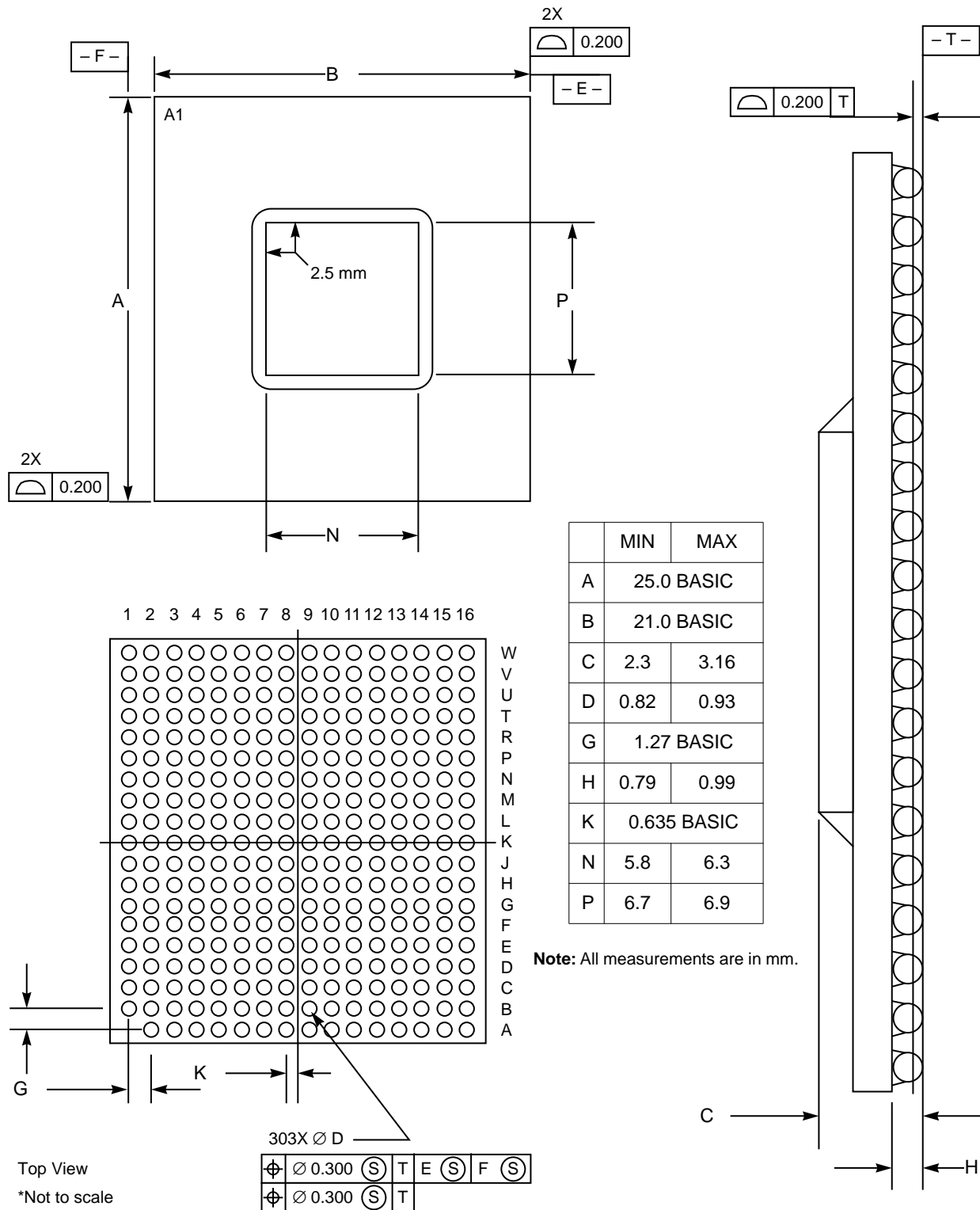
Figure 11. MPC105 Mechanical Dimensions

Preliminary/Subject to Change without Notice

1.6 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC105 PCI Bridge/Memory Controller.

1.6.1 PLL Configuration

The MPC105 is designed to operate over a wide range of processor and PCI bus frequencies. The PLL is configured by the PLL_CFG0–PLL_CFG3 pins. For a given SYSCLK (bus) frequency, the PLL configuration pins set the internal MPC105 frequency of operation. Table 10 describes the PLL configurations required for different ratios between the processor bus frequency and the PCI bus frequency.

Table 10. PLL Configuration

PLL_CFG0–PLL_CFG3	Processor Bus, PCI, and PLL Frequencies				
	Processor Bus: PCI Bus Ratio (SYSCLK)	PCI Bus 16.6 MHz	PCI Bus 20 MHz	PCI Bus 25 MHz	PCI Bus 33.3 MHz
0001	1:1	—	—	—	33.3 (133)
0010	1:1	16.6 (133)	20 (160)	25 (200)	—
0100	2:1	—	—	—	66.6 (133)
0101	2:1	33.3 (133)	40 (160)	50 (200)	—
0011	PLL bypass				
1111	Clock off				

Notes: 1. Some PLL configurations may select bus, CPU, or PLL frequencies which are not useful, not supported, or not tested for by the MPC105. PLL frequencies (shown in parenthesis in Table 10) should not fall below 120 MHz, and should not exceed 200 MHz.

2. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, and the bus is set for 1:1 mode operation. The PLL-bypass mode is for test only, and is not intended for functional use. In clock-off mode, no clocking occurs inside the MPC105 regardless of the SYSCLK input.

3. The PLL_CFG0–PLL_CFG1 signals select the CPU-to-bus ratio (1:1, 2:1) and the PLL_CFG2–PLL_CFG3 signals select the PCI-to-PLL multiplier (x2, x4, x8).

4. The level 2 cache and memory interfaces will function at the processor bus frequency.

1.6.2 PLL Power Supply Filtering

The AVdd power signal is provided on the MPC105 to provide power to the clock generation phase-lock loop. To ensure stability of the internal clock, the power supplied to the AVdd input signal should be filtered using a circuit similar to the one shown in Figure 12. The circuit should be placed as close as possible to the AVdd pin to ensure it filters out as much noise as possible.

Preliminary/Subject to Change without Notice
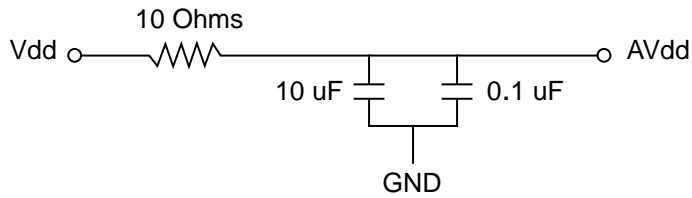
Figure 12. PLL Power Supply Filter Circuit

1.6.3 Decoupling Recommendations

The MPC105 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC105 system, and the MPC105 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place a decoupling capacitor with a low ESR (effective series resistance) rating to at least one Vdd pin of the MPC105.

This capacitor should be at least 0.1 µF to provide both high and low frequency filtering, and should be placed as close as possible to their associated Vdd pin. Surface-mount tantulum or ceramic devices are preferred. It is also recommended that these decoupling capacitors receive their power from Vdd and GND power planes in the PCB, utilizing short traces to minimize inductance in the traces. Power and ground connections must be made to all external Vdd and GND pins of the MPC105.

1.6.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active-low inputs should be connected to Vdd. Unused active-high inputs should be connected to GND.

Note that in 32-bit data bus mode, the unused processor bus data signals (DL0-DL31) must be connected to pull-up resistors for proper device operation.

1.6.5 MPC105 Thermal Management Information

The use of C4 die on a CBGA interconnect technology offers significant reduction in both the signal delay and the microelectronic packaging volume. Figure 13 shows the salient features of the C4/CBGA interconnect technology. The C4 interconnection provides both the electrical and the mechanical connections for the die to the ceramic substrate. After the C4 solder bump is reflowed, epoxy (encapsulant) is under-filled between the die and the substrate. Under-fill material is commonly used on large high-power die; however, this is not a requirement of the C4 technology. The package substrate is a 21 mm multilayer-cofired ceramic. The package-to-board interconnection is by an array of orthogonal 90/10 (lead/tin) solder balls on 1.27 mm pitch. During assembly of the C4/CBGA package to the board, the high-melt balls do not collapse.
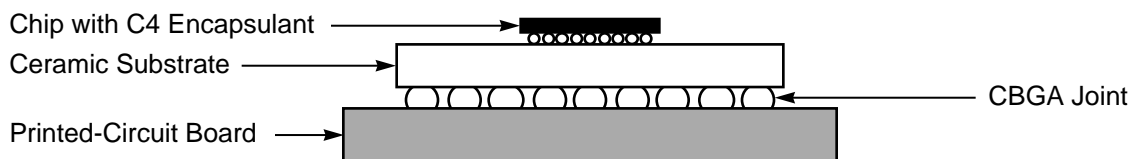
Figure 13. Exploded Cross-Sectional View

Preliminary/Subject to Change without Notice

1.6.5.1 Internal Package Conduction Resistance

For this C4/CBGA packaging technology, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lead thermal resistance

These parameters are shown in Table 11. In this C4/CBGA package, the silicon chip is exposed; therefore, the package "case" is the top of the silicon.

Table 11. Thermal Resistance

Thermal Metric	Effective Thermal Resistance
Junction-to-case thermal resistance	0.133 °C/W
Junction-to-lead (ball) thermal resistance	3.8 °C/W

Figure 14 provides a simplified thermal network in which a C4/CBGA package is mounted to a printed-circuit board.

(Note the internal versus external package resistance)
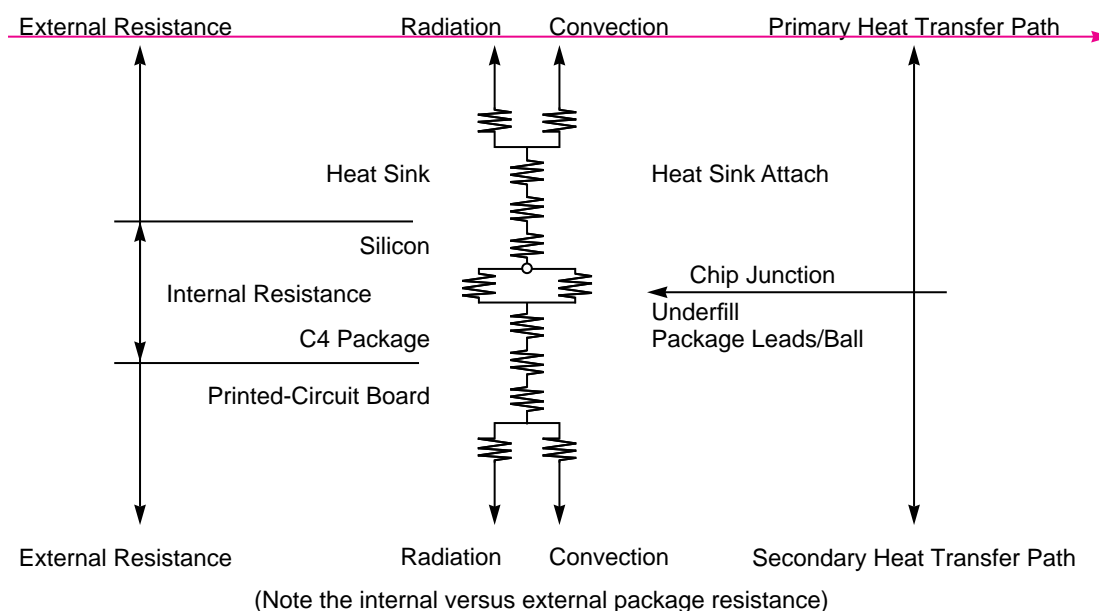
Figure 14. C4/CBGA Package Mounted to a Printed-Circuit Board

1.6.5.2 Board and System-Level Modeling

A common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies is the junction-to-ambient thermal resistance. The final chip-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power dissipation, a number of factors affect the final operating die-junction temperature. For example, these factors might include airflow, board population, heat sink efficiency, heat sink attach, next-level interconnect technology, and system air temperature rise.

Preliminary/Subject to Change without Notice

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For this reason, we recommend using conjugate heat transfer models for the board as well as system-level designs. To expedite system-level thermal analysis, several "compact" CBGA thermal models are available within FLOTHERM®. These are available upon request.

The die junction-to-ambient thermal resistance is shown in Table 12. The model results are in accordance with SEMI specification G38. This standard specifies a single component be placed on a 7.5 cm x 10 cm single-layer printed-circuit card. Note that this single metric may not adequately describe three-dimensional heat flow.

Table 12. Die Junction-to-Ambient Thermal Resistance

Airflow Velocity (Meter/Second)	Airflow Velocity (Feet/Minute)	Die Junction-to-Ambient Thermal Resistance (SEMI G38) ($^\circ$C/W)
1	196.8	22.0
2	393.7	18.5
3	590.0	17.0

Motorola Literature Distribution Centers:
USA: Motorola Literature Distribution, P.O. Box 20912, Phoenix, Arizona 85036; FAX (602) 994-6430.
JAPAN: Nippon Motorola Ltd., 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd., Silicon Harbour Centre, No. 2 Dai King Street, Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong.
Technical Information: Motorola Inc. Semiconductor Products Sector Technical Responsiveness Center; (800) 521-6274.
Document Comments: FAX (512) 891-2638, Attn: RISC Applications Engineering.

MOTOROLA