MPC561/MPC562

Product Preview
PowerPC™ RISC MCU Including Peripheral Pin Multiplexing with Code Compression Option

The MPC561/MPC562 are members of the Motorola MPC500 PowerPC^{TM} RISC Microcontroller family. As shown in the block diagram, they are composed of:

- High performance CPU system
    — High performance core
        - PowerPC single issue integer core
        - Precise exception model
        - Floating point
        - Extensive system development support
            — On-chip watchpoints and breakpoints
            — Program flow tracking
            — Background debug mode (BDM)
            — IEEE-ISTO 5001-1999 NEXUS Class 3 Debug Interface
                - Up to 16-pin interface
    — MPC500 PowerPC system interface (USIU, BBC, L2U)
    — Fully static design
    — Four major power saving modes
        - On, doze, sleep, deep sleep and power-down
    — 32-Kbyte static RAM (CALRAM)
    — General purpose I/O support
        - On address (24) and data (32) pins
        - 16 GPIO in MIOS14
        - Many peripheral pins can be used as GPIO when not used as primary functions
        - 2.6-V outputs on external bus pins
- PPM (peripheral pin multiplexing with parallel-to-serial driver) module
- Integrated I/O System
    — True 5-V I/O
    — Two time processing units (TPU3) with eight Kbytes DPTRAM
    — 22-channel MIOS timer (MIOS14)
    — Two queued analog-to-digital converter modules (QADC64_A, QADC64_B) providing a total of 32 analog channels
    — Three TouCAN modules (TOUCAN_A, TOUCAN_B, TOUCAN_C)
    — One queued serial module with one queued SPI and two SCIs (QSMCM)
- Available in plastic ball grid array (PBGA) packaging

Digital DNA
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MPC561/MPC562 Optional Features

The following are optional features of the MPC561/MPC562.

- 56-MHz operation (40 MHz is default)
- Code compression supported on the MPC562
    — Compression reduces instruction memory requirements by 40-50%
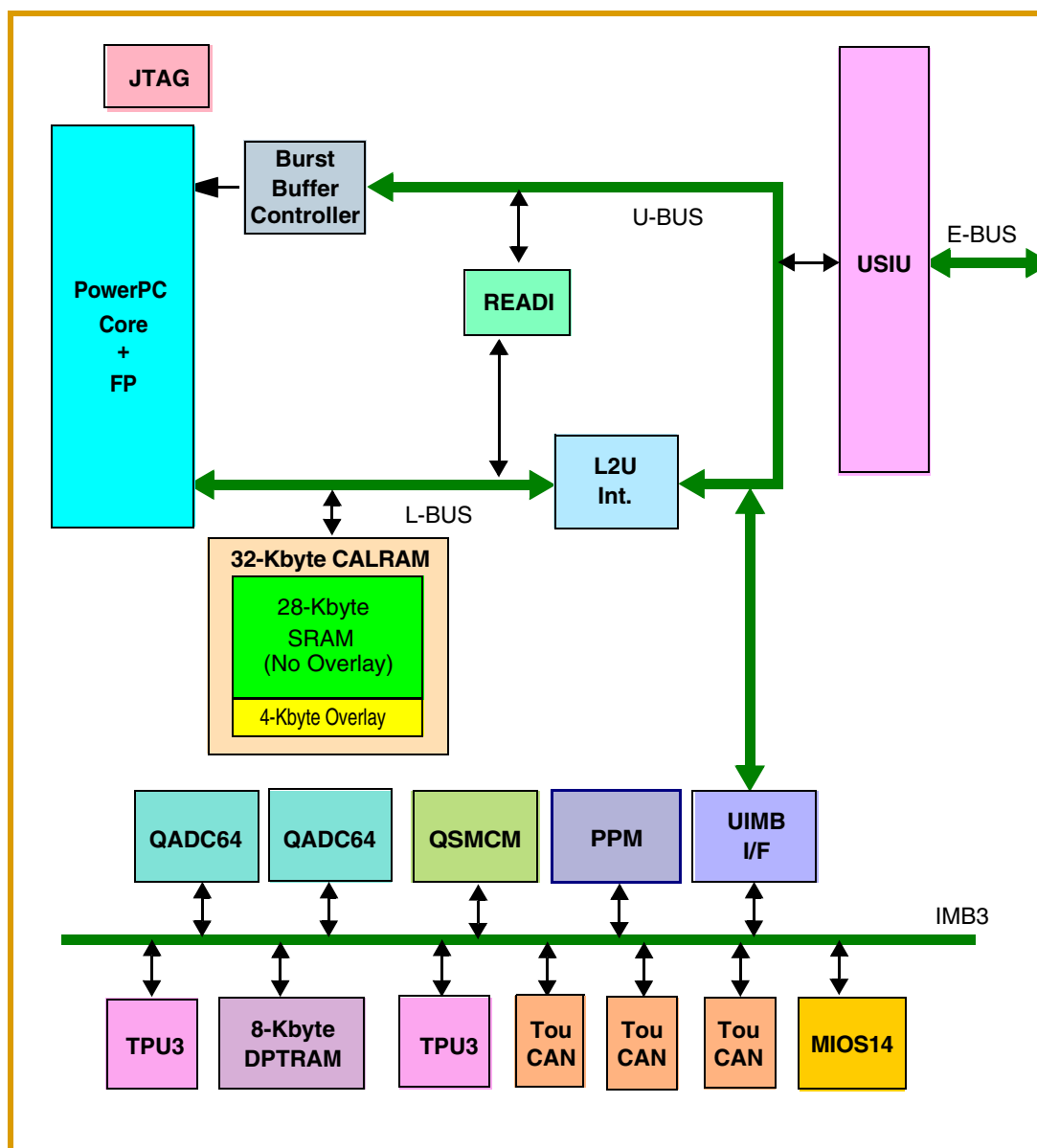   — Compression optimized for automotive (non-cached) applications

Figure 1 MPC561/MPC562 Block Diagram