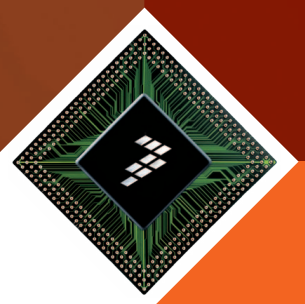

White Paper

Powertrain

Challenges and solutions in advanced powertrain controls

freescale™

Challenges and Solutions in Advanced Powertrain Controls

Overview

Each new generation of powertrain controls challenges systems designers with higher complexity and the need for increased computing performance. Driven by global regulations, performance requirements include increased throughput, memory, peripheral and advanced packaging capabilities. Increasingly tougher emission regulations, as well as unprecedented fuel efficiency targets, require sophisticated systems that extend well beyond traditional spark ignition (SI) engine and transmission control. The addition of hybrid electric vehicles and plug-in hybrid electric vehicles with motors, battery and system management electronics dictate control technologies that depart from traditional improvement trends.

As a leading supplier of automotive powertrain microcontrollers (MCUs), Freescale Semiconductor has addressed these challenges as it has facilitated automotive industry's pioneering efforts in electronics control. This white paper will provide background on the need for an advanced control architecture and a multicore solution that addresses current and future powertrain needs.

Global Regulations Impact Powertrain

According to the International Energy Agency (IEA) report "Transport Energy Efficiency," transportation represents 23 percent of global CO_2 emissions. Based on global concerns, governments in all regions have taken steps to reduce CO_2 and other emissions and increase vehicle fuel economy. (Reduced fuel consumption directly results in lower CO_2 emissions.)

In the U.S., recent legislation calls for carmakers to meet a corporate average fuel economy (CAFE) target of 54.5 miles per gallon by 2025. The reduction from today's passenger vehicles that average 27.8 mpg requires an average increase in fuel economy of five percent for cars and three and a half percent for light trucks per year through 2021, with a five percent increase for all vehicles after that. Already well ahead of the U.S. in lower fuel consumption, the European Union (EU) plans to achieve a fleet-wide average of 65 mpg by 2020.

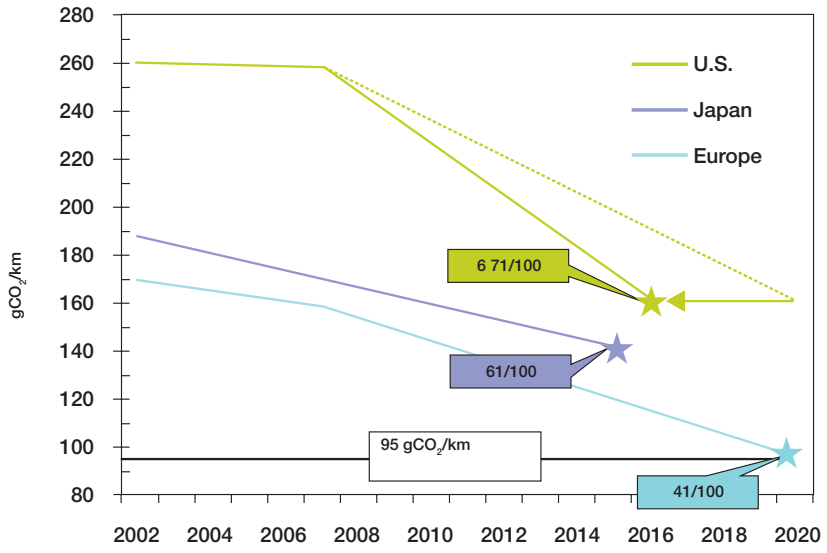

Figure 1. Global CAFE regulations vary but all require significant changes from the systems in today's fleet.

Figure 1 shows a phase-in of EU regulations to limit emissions to 120 g/km of CO_2 per car for 65 percent of new cars by 2012 and an increase in the requirements to 100 percent by 2015. Non-compliance can result in EU fines up to €95 for every gram of CO_2 above the target for each vehicle sold. Internal combustion engine improvements as well as electrification are required to meet the standards.

Europe is leading the way with regulations in this area but other regions, including the U.S. and Japan, have their own challenging requirements. In the U.S., changes to satisfy the 2016 goals (noted in Figure 1) will require the greatest improvements. Even if this level is achieved by 2016, the values will just match where Europe was five years ago. This opportunity for improvement requires higher performance in powertrain control.

While some of the improvements to reduce CO_2 can be achieved by reducing weight, rolling resistance and improving aerodynamic properties, powertrain has been identified as the system that can provide the greatest improvement with a 10 percent engine fuel consumption reduction and from 10 to 15g of CO_2 reduction. In this case, an increase in spending for additional MCU performance, such as an increase in DMIPS from 200 (the high-end capability on production vehicles) to 600 or 800 can avoid the €95 surcharge per car. As a result, performance has a direct impact on cost or penalty avoidance.

To meet these global government requirements, carmakers must significantly update their existing software and hardware but are challenged by limitations that include memory and throughput to run new algorithms as well as the cost impact of any new control. The solution to these restrictions

Feature	MPC5566	MPC5674F	MPC5676R
Process	130 nm	90 nm	90 nm
Core	z6	z7	z7
Number of Cores	1	1	2
Performance	132 MHz	264 MHz	2 x 180 MHz
Single Precision Floating Point	Yes	Yes	Yes
SIMD	Yes	Yes	Yes
VLE	Yes	Yes	Yes
Cache	32 KB Unified	16 KB Instruction + 16 KB Data	16 KB Instruction + 16 KB Data
Non-Maskable Interrupt	No	NMI, Critical	NMI, Critical
MMU Entries	32	64	32
MMU Tool Control	No	No	Yes
MPU	No	Yes	Yes
Semaphores	No	No	16
CRC Channels	No	No	3
Software Watchdog Timer	No	1	2
Core Nexus Class	3+	3+	3+
SRAM	128 KB (32K Standby)	256 KB (32K Standby)	384 KB (48K Standby)
Flash	3 MB	4 MB	6 MB
Flash Fetch Accelerator	2 x 256-bit	4 x 256-bit	4 x 256-bit
External Bus	32-bit	Yes	Yes
Calibration Bus	16-bit	16-bit non-mux, 16, 32-bit muxed	16-bit, 32-bit muxed
DMA Channels	64	64 + 32	64 + 64
DMA (Nexus Class)	3	3	3
Serial Interface (eSCI)	2	3	3
FlexCAN	4	4	4
SPI	4	4	5
Microsecond Bus	No	Yes	Yes
FlexRay™	No	Yes	Yes
Ethernet	Yes	No	No
System Timers	No	1x RTI, 4x PIT, 4x AUTOSAR	1x RTI, 4x PIT, 4x AUTOSAR
eMIOS Channels	24	32	32
eTPU Channels	64	64	96
eTPU Version	2 x eTPU	2 x eTPU2	3 x eTPU2
eTPU Code Memory	12 KB	24 KB	24 KB + 12 KB
eTPU Data Memory	3 KB	6 KB	6 KB + 3 KB
Interrupt Controller	308 Sources	448 Sources	500 Sources
ADC Input Pins	40	64	64
ADC Input Diagnostics	No	Yes	Yes
ADC Resolution	12-bit	12-bit	12-bit
ADC Quantity	2	4	4
ADC Variable Gain Amp	No	Yes	Yes
Temperature Sensor	No	Yes	Yes
Decimation Filters	No	8	12
Protected Port Output	No	No	4
Self-Test Controller	No	No	Yes
Dev Tool Semaphores	No	No	32
PLL	FM	FM	FM
Integrated Linear Voltage Regulator	1.5V	3.3V, 1.2V	3.3V, 1.2V
Integrated Switch Mode Voltage Regulator	No	1.2V	1.2V
External Power Supplies	5V, 3.3V	5V	5V
Low-Power Modes	No	StopMode, SlowMode	StopMode, SlowMode
DMIPS	200	600	818

Table 1. Feature comparison of the latest dual-core processor versus previous generation single core processors for powertrain applications shows the improved capabilities in several critical areas.

Due to the aggressive targets for emission reduction and fuel consumption, many superannuated control techniques are being revisited as potential options for production. In the past, the solution may have required a dedicated controller in a separate ECU. With today's MCU capabilities, it's simply an integrated add-on to a more powerful processor. Figure 2 shows the block diagram of the enabling dual-core MCU.

is a dual-core MCU built using the industry's most popular powertrain architecture.

As shown in Table 1, the dual-core Qorivva MPC5676R MCU, built on Power Architecture® technology, provides substantial improvements in numerous areas that specifically impact powertrain controls. Designed to provide the improvements that system designers have requested, the increased complexity of next-generation control systems now has a straightforward path from today's systems with several exciting possibilities.

The MPC5676R is the first dual-core Power Architecture device for powertrain applications, and provides virtually seamless compatibility with its single-core predecessor, the MPC5674F. At the same time, it introduces a powerful set of new dual-core features to combat the challenge of novel, computation intensive software such as that used for virtual sensing and heuristic control algorithms. These capabilities enable developers to eliminate the need for many external components, which can help reduce system cost by nearly 30 percent over conventional systems and make advanced fuel-saving technology more affordable.

Increased capability can be put into perspective through examples and concepts or possibilities of what can be accomplished with the new dual-core MCU that were difficult or impossible before.

Powertrain Control in Internal Combustion Engines

In addition to addressing the complex requirements of today's diesel engines, which include delivering multiple pulses of fuel to eliminate undesirable noises and reduce particulates in emissions, advanced dual-core MCUs can also improve spark-ignition engine controls. In the diesel engine, precise fuel control in the common-rail injection system requires complex calculations to determine fuel injection timing, air volume and pressure, engine temperature and more. Some of these same techniques are being added or modified for SI engines.

Gasoline Direct Injection

While approaches to deal with some of the advanced control requirements have existed for many years, addressing the combination of these approaches in one MCU was either very difficult or impossible due to performance limitations. For example, gasoline direct injection has been performed for many years in Europe and is increasingly being implemented in the U.S.

With a 10 to 15 percent improvement in fuel economy and horsepower and as much as a 25 percent reduction in hydrocarbon emissions, direct injection is projected to expand rapidly in powertrain applications—from slightly over 20 percent in 2010 to almost 40 percent by 2017 according to Strategy Analytics. Replacing the more forgiving but less fuel-efficient port injection requires an order of magnitude improvement in processing power. Instead of a single pulse that is on or off for a certain period of time and placed in one location, the MCU must handle a complex peak and hold waveform with methods for detecting valve motion. The process involves precise current measurements and significant high-speed switching to develop a current profile. And there may be more than one injection per cycle. As a result, the raw calculation power and raw timing requirements have increased exponentially.

The three 96-channel enhanced timing units with 45K of dedicated RAM within the dual-core MCU are designed to handle complex engine timing events with ease and flexibility. Mechanical gear teeth can typically achieve six-degree accuracy, however, 0.1-degree accuracy is required for optimal control of fuel spray and spark. Since the input data is less accurate than the required output, the MCU must predict when the spark is required.

As shown in Figure 3, one of the three second-generation enhanced time processor units (eTPU2s) of the MCU can be used to predict the precise time required for direct injection and compensate for mechanical limitations. The eTPU2 measures the time between the last two teeth and makes angle-to-time conversions—one of the chip's virtual sensing possibilities. To achieve approximately 36,000 conversions/sec per cylinder, significant performance is required. The dual-core processor provides this capability to improve fuel economy through much tighter control.

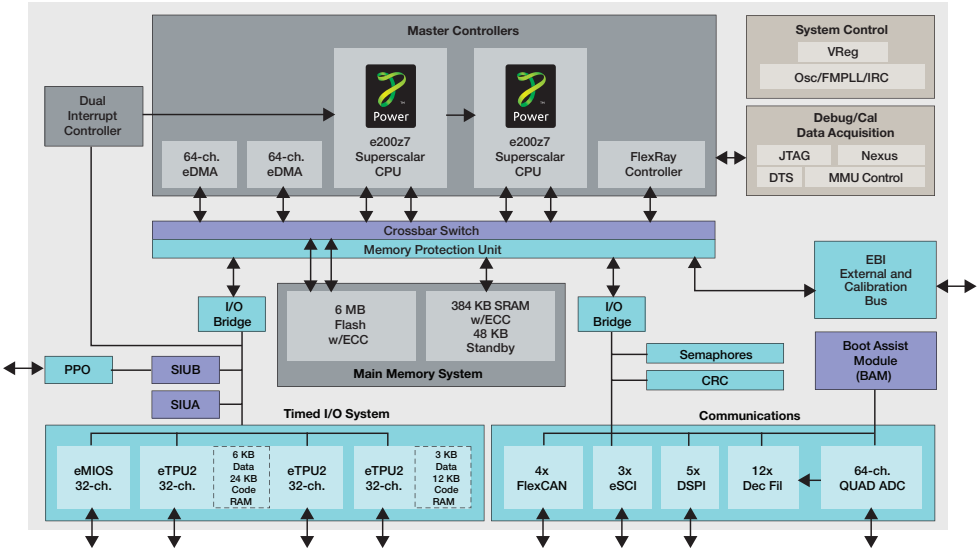

Figure 2. The MPC5676R block diagram shows the dual cores and added peripherals.

Start-Stop Systems

Start-stop (or stop-start) or idle-stop systems that turn the engine off at idle and automatically restart it when the driver presses the accelerator can improve fuel economy by four to 10 percent and even as much as 25 percent on some vehicles.

With direct injection, these systems will also experience strong growth and contribute to achieving legislation compliance for emissions. Initially implemented in Europe, where they are already widely used, start-stop systems are projected to have significant growth rate in all regions with some experts predicting as high as a 35 percent implementation in North America within the next four to five years.

Start-stop systems place an increased burden on the control electronics. To make these systems as seamless as possible, the system must detect the position where the engine stops. This may require detecting the reversal of the engine's direction to determine the exact position in the crankshaft cycle that the engine comes to rest. In addition to the standard crankshaft sensor, either an additional sensor or a more complex sensor is required to provide this information. The eTPU2 of the dual-core MCU provides the capability to solve the increased complexity of start-stop systems even when this aspect is combined with the timing requirements of direct injection.

Knock Detection

Knock control systems optimize the combustion cycle and improve fuel economy by as much as three to five percent. Control techniques for knock detection include in-cylinder pressure sensing, vibration sensors and spark plug ionization. In today's systems, a dedicated application-specific integrated circuit (ASIC) typically identifies the knock signal from other engine noise within a time window of a few milliseconds. The analog signal from the knock detection sensor(s) is sampled typically at 150 KHz and applied as an input parameter to the spark control system. Knock detection involves massive amounts of digital filtering and calculations.

A dual-core MCU with three enhanced time processor units can handle this complexity as well as other control tasks. As shown in Figure 4, once the analog signal is digitized, the eTPU2 predicts the knock window using virtual sensing.

The quad ADCs of the dual-core MCU are capable of continuous conversions at 800 KHz, allowing ample bandwidth to simultaneously sample knock and other analog inputs in the system. With twelve decimation filters, the dual core MCU has the capability to support the most advanced knock detection systems and still have several filters for other control functions. It can even handle complex pressure sensing techniques for knock detection that require multiple analog-to-digital (ADC) converters and large RAM and flash arrays to handle large quantities of data and complex algorithms. In addition, the MPC5676R hardware integrators, DMA and SPE code eliminate external hardware. The end result is lower

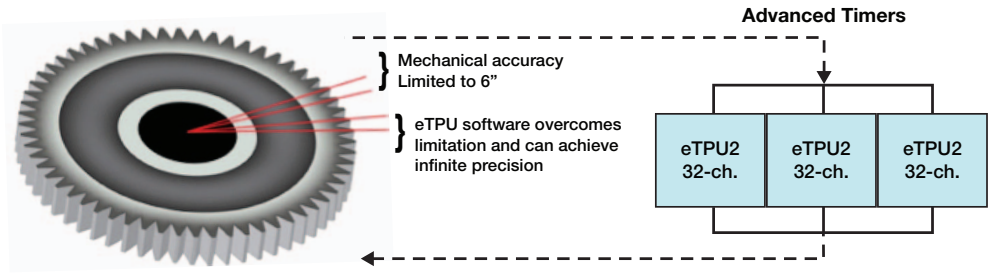

Figure 3. Advanced eTPU2 timers provide the precision for direct injection.

system cost through the elimination of an ASIC, filters, external ADC and multiplexer in the powertrain system.

In-Cylinder Pressure Sensing

In-cylinder pressure sensing can potentially replace knock/misfire detection, mass air flow and manifold absolute pressure sensors as well as cylinder balancing subsystems. However, acquiring up to eight pressure profiles over a full 720 degrees (one sensor per cylinder for an eight-cylinder engine) provides a challenge for closed-loop combustion control. With a dual-core MCU, one possible solution involves multiple parallel decimation filter paths and high-performance software on one dedicated core while the other core runs the application strategy. In current systems, knock and lambda sensors provide feedback for the next engine cycles. With the pressure control system, designers want to reduce the pressure in the current cycle. To meet proposed Euro 6 requirements for much lower NOx, reducing the pressure is the easiest way to reduce the temperature and avoid NOx creation.

MultiAir System

The Fiat-pioneered MultiAir system uses electro-hydraulic, instead of mechanical variable valve timing (VVT), technology controlling air intake to increase power up to 10 percent and torque up to 15 percent. In addition, it can reduce carbon dioxide emissions by 10 to 25 percent. The approach allows engine downsizing and provides even greater improvement when used with a supercharger.

The Fiat/Chrysler MultiAir system currently uses a separate ECU. Taking advantage of a dual-core system allows the MultiAir control functions to be integrated in the engine ECU, thus reducing overall cost.

Cylinder Deactivation

Hybrid systems need complete deactivation of the engine when the vehicle stops and the engine would normally idle and consume fuel without adding any miles to the MPG calculation. This requires more performance from the MCU. Cylinder deactivation when the engine is running involves turning an eight-cylinder into a four-cylinder or a six-cylinder into a three-cylinder engine under certain light-load driving conditions. Also called “variable displacement” or “displacement on command,” this technique is attributed to achieving improvements from 10 to 16 percent depending on highway and cruising conditions or test cycle. In these systems, digital control selectively deactivates the cylinders through electronically controlled throttle valves. This process requires improved computing power and precise timing from the powertrain microcontroller as well as additional software for torque matching. The dual-core MCU is more than up to the challenge for these systems.

Automatic Transmissions

Automatic transmission control has increasingly become a standard part of the modern complex powertrain systems. Today’s six-speed transmissions have six or more precision current controlled solenoids actuated by digital electronics. This requires over-sampling current waveforms by 32, 64 or 128 times, actuating at roughly 300 microseconds instead of one millisecond for previous-generation transmissions. This is a massive increase in computing and sensing power over what was previously required. Recently announced nine-speed automatic transmissions have been credited with a 16 percent fuel economy improvement over a standard six-speed automatic. Increasingly more complex transmissions can rely on the processing, timing and filtering capability of dual-core MCUs.

Dual-Clutch Transmissions

Dual-clutch six-speed transmissions provide fuel efficiency of a manual gearbox with the convenience and ease of a premium automatic transmission. The more efficient (up to nine percent less fuel consumption) dual-clutch transmissions (DCTs) engage very rapidly and shift gears in milliseconds, requiring more processing power to mesh properly and in a timely manner. Essentially an electromechanical version of the clutch, these advanced transmissions are projected to increase from about 10 percent in 2010 to over 20 percent by 2017 in the U.S. The DCT requires improved MCU performance to synchronize the speeds of different shafts as the clutch is applied. This can readily be accomplished by one of the eTPU2s in the dual-core MCU.

Powertrain Electrification

In the near-term, engine downsizing, gasoline direct injection conversion and start-stop implementation will play dominant roles in improving vehicle fuel economy and meeting emission standards. Vehicles that don’t have these last two features have an increased likelihood of transitioning to them within the next few years. In a slightly longer

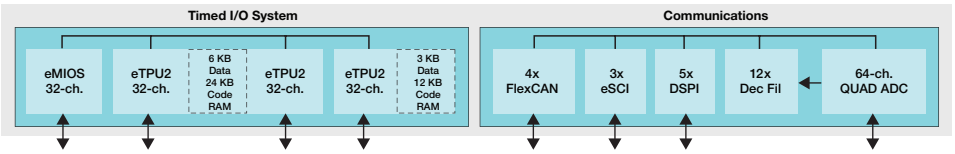

Figure 4. A knock detection example using decimation filters (DecFil), ADC, eTPU2 and additional dual-core MCU hardware and software capabilities.

timeframe, perhaps three to seven years, extreme downsizing will occur with full-car electrification as well as strong growth in plug-in HEVs and EVs. Beyond seven years, multi-technology emergence will occur.

Electronic controls in hybrids and EVs take the role of the MCU in vehicles to new levels. An electric motor's function can be as simple as a start-stop system in a mid- or even a micro-hybrid to a full-hybrid, plug-in hybrid or full-electric vehicle. In these vehicles, MCUs control the motors and manage the batteries. For hybrids that also have an engine for propulsion or charging, the control adds to the complexity of managing the internal combustion engine.

Motor Control

In HEVs and EVs, the inverter operation involves shaping precise waveforms. With a three-phase inverter control, smart peripherals are required to simplify the calculations and timing. The process is similar to the control of efficient three-phase motors that have been implemented in other vehicle systems such as electrical power steering (EPS), however, more calculation power is required.

The use of small and powerful motors requires a high number of poles and operation at a frequency, for example, of approximately 1 kHz. To meet these requirements, the dual-core MCU takes advantage of the high resolution capability of the eTPU2 as shown in Figure 5. At low speeds, less than 10 percent of the nominal voltage must be generated. The eTPU2 in the dual-core MCU can generate this low-voltage to achieve smooth torque control.

Multiple eTPUs provide system designers more options. With the three eTPUs in the MPC5676R, some system designers are considering controlling two DC motors with a single MCU.

Battery Management

The battery management in hybrid and electric vehicles is a complex task because it involves more than just managing the power going into or out of the battery. Monitoring the individual cells to safely put power in and get power out dictates the need for many inputs and outputs and extensive calculating power for the control. The powertrain MCU requires extensive communication with the battery management system. The dual-core MCU solution provides a range of serial communication protocols such as eSCI, DSPI, FlexRay, microsecond channel and CAN for a range of reliable communication design options.

Solving System Problems

In addition to addressing increased complexity in powertrain subsystems, the newest multicore powertrain architecture MCU has several powerful features that can have a significant impact on the powertrain system design. Examples of these include: self checking, simplified calibration, reduced power consumption, and software tasks and shared data management.

Self Checking

The dual-core MCU has extended self checking capabilities. The self-test control unit includes a programmable logic built-in self-test (LBIST) feature that has not been available on other powertrain MCUs. With this capability, the MPC5676R has improved fault coverage on the hardware logic associated with the execution of software, such as the core pipelines and cache controller.

The LBIST feature improves the ability to detect latent fault conditions, providing greater reliability to the MCU and the control system. Normally performed at start up, self-test involves a very extensive check of the hardware. Self-test operation prevents running any application code because the self-test takes control of all the logic on the chip. To achieve programmability, the LBIST is run on one core while the other core runs the application code. This provides system designers the opportunity of performing self checks on-the-fly to determine the logical state of the chip.

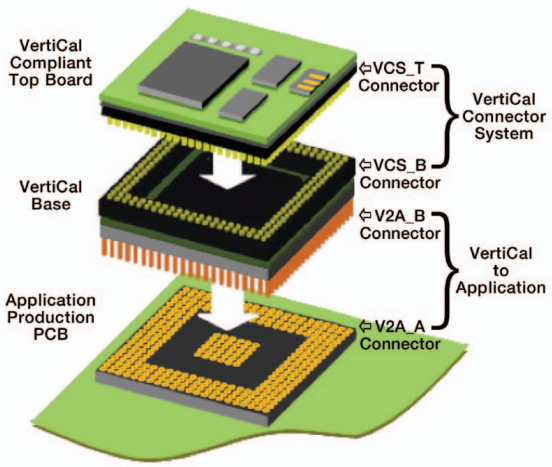

Figure 6. VertiCal System.

Simplified Calibration Process

The dual-core MPC5676R has a patented mechanism that makes it easier to calibrate engine maps by allowing an external calibration tool to non-intrusively interact directly with the memory management unit (MMU) of the MPC5676R. The approach greatly simplifies the A-B switching of memory maps performed during the engine calibration process and eliminates the need for external logic (for example, an external dual-ported RAM strictly for calibration), as well as the need to interrupt the processor's operation to switch memory.

Combining this patented mechanism with the proven VertiCal calibration system isolates the calibration process from the application code, resulting in a faster, more robust system development lifecycle.

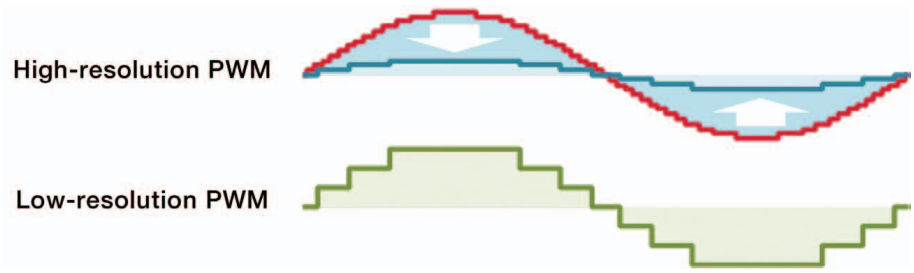

Figure 5. In contrast to the lower resolution output shown on the bottom, the high-resolution capability from the eTPU2 (on top) allows the generation of a smooth waveform at low voltages to achieve smooth torque control in this operating region.

VertiCal calibration systems use production silicon in a chip-scale package (CSP) to ensure full hardware and software compatibility between production and calibration systems, support for simplified use of overlay memory, Nexus-based debug tool support, support for full-feature calibration tools via availability of comprehensive set of device signals, flexibility to support new debug and calibration features such as high-speed serial communications, and allows system calibration without impacting standard MCU I/O resources.

Higher Performance within Low Power Constraints

Getting higher performance within low power constraints required in modern vehicles dictates a change in design philosophy that suppliers of microprocessors for personal computers have embraced for several years. The change results from the limitations of further improvements in performance at the expense of increased power consumption.

Pollack's rule states that the increase in performance is roughly proportional to the square root of the increase in complexity. In other words, in order to get twice the performance from a single core, its complexity must increase fourfold. In general, the increased complexity essentially equals the increase in power consumption. As shown in Figure 7, the lowest power consumption increase results from using two CPUs running at the same frequency. Other options of increasing the logic gates or increasing the frequency all result in higher power consumption.

Software Tasks and Shared Data Management

When applying the techniques described in this paper to the dual-core architecture of the MPC5676R, it is most likely necessary to coordinate software tasks and accesses to shared resources such as ADC result tables, program variables and hardware I/O accesses.

The MPC5676R provides enhanced features to support task synchronization and shared data management through the use of hardware cache coherency mechanisms and semaphores. Cache coherency provides a method of sharing fast access cached data between the cores as well as data updated by the DMA controllers. Semaphores implemented either with the memory mapped hardware semaphore block or with the software implemented reservation mechanism provide the means for sharing resources and synchronizing tasks between the cores. Programmers can take advantage of these powerful techniques to increase the performance, reliability and flexibility of their application software and hardware.

Software Tools and Enablement

Freescale has the tools and software for a comprehensive ecosystem to support dual-core MCUs. As part of the industry-standard Power Architecture family heritage, the newest dual-core MCUs benefit from a comprehensive selection of development tools from Freescale as well as third parties that have multi-core support with VertiCal calibration solutions. As the performance requirements increase, the transition is quite simple. There is a wide selection of development tools supported by several companies for software tools, compilers and debuggers.

The extensive use of Power Architecture technology in automotive has attracted many third-party tool developers. This simplifies system designers' efforts, even though they are addressing far more complex problems than they have in the past. Designers familiar with the Power Architecture toolset will feel comfortable using it for dual-core processors. Full software compatibility allows for reduced development time and quicker time to market. The dual-core MCU offers an extremely easy migration path for other Power Architecture family members and it is drop-in compatible with the single-core MPC5674F. As a result, investments that have been made in these toolsets apply to the next generation of processors. Additionally, the 6 MB of non-volatile flash memory of the MPC5676R supports computationally intensive modeling environments and auto-code generation software tools such as AUTOSAR, without the cost and complexity of adding off-chip memory. In addition, Freescale now offers a complete, integrated development environment to design, test and debug eTPU software with 100 percent cycle accuracy.

A History of Powertrain Enablement

Freescale has been an integral part of automotive powertrain since the earliest MCU applications in the 1970s, when pioneering technology was required to meet clean air regulations. The introduction of 32-bit Power Architecture technology in 1998 initiated a new era in powertrain performance that has resulted in the industry's most successful family of 32-bit powertrain microcontrollers.

Now, as carmakers and their tier-1 suppliers cope with solving new emissions and fuel economy problems for every region of the world, a flexible dual-core MCU based on the Power Architecture technology provides them the performance and design tools to turn extremely complex problems into a solvable situation.

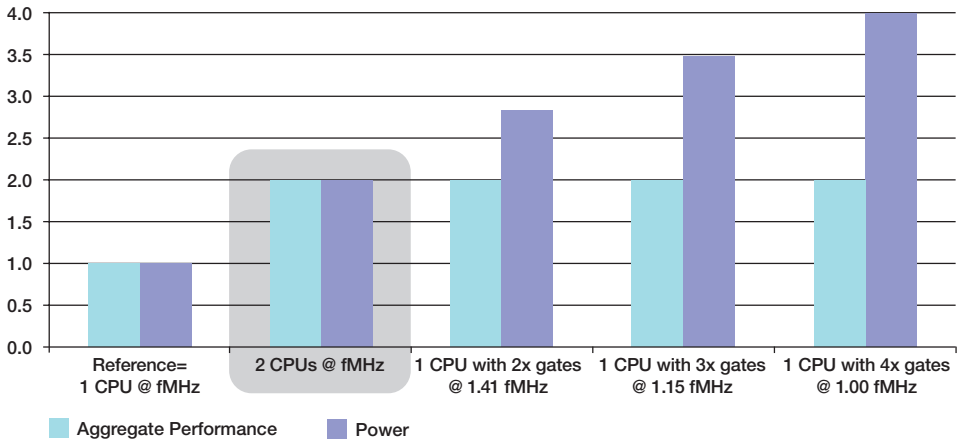

Figure 7. Doubling the CPUs is the most power efficient method to achieving twice the performance.

How to Reach Us:

Home Page:
freescale.com

Automotive Information:
freescale.com/automotive

e-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
1-800-521-6274
480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447
303-675-2140
Fax: 303-675 2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright license granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

freescale™

For more information, visit freescale.com/automotive

Freescale and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off.
All other product or service names are the property of their respective owners. © 2011 Freescale Semiconductor, Inc.

Document Number: PWRTRN1WP REV 0