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Advance Information

PowerPC 603e™ RISC Microprocessor Family: PID7v-603e Hardware Specifications

The PowerPC 603e microprocessor is an implementation of the PowerPC™ family of reduced instruction set computing (RISC) microprocessors. In this document, the term ‘603e’ is used as an abbreviation for ‘PowerPC 603e microprocessor’. The PowerPC 603e microprocessors are available from Motorola as MPC603e and from IBM as PPC603e.

Note that the 603e is implemented in both a 2.5-volt version (PID 0007v PowerPC 603e microprocessor, abbreviated as PID7v-603e) and a 3.3-volt version (PID 0006 PowerPC 603e microprocessor, abbreviated as PID6-603e). This document describes the pertinent physical characteristics of the PID7v-603e. For functional characteristics of the processor, refer to the *PowerPC 603e RISC Microprocessor User’s Manual*.

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1.1 Overview

This section describes the features of the 603e and describes briefly how those units interact.

The 603e is a low-power implementation of the PowerPC microprocessor family of reduced instruction set computing (RISC) microprocessors. The 603e implements the 32-bit portion of the PowerPC architecture specification, which provides 32-bit effective addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits. For 64-bit PowerPC microprocessors, the PowerPC architecture provides 64-bit integer data types, 64-bit addressing, and other features required to complete the 64-bit architecture.

The 603e provides four software controllable power-saving modes. Three of the modes (the nap, doze, and sleep modes) are static in nature, and progressively reduce the amount of power dissipated by the processor. The fourth is a dynamic power management mode that causes the functional units in the 603e to automatically enter a low-power mode when the functional units are idle without affecting operational performance, software execution, or any external hardware.

The 603e is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can execute out of order for increased performance; however, the 603e makes completion appear sequential.

The 603e integrates five execution units—an integer unit (IU), a floating-point unit (FPU), a branch processing unit (BPU), a load/store unit (LSU), and a system register unit (SRU). The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for 603e-based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single-precision multiply-add instruction can be issued every clock cycle.

The 603e provides independent on-chip, 16-Kbyte, four-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs). The MMUs contain 64-entry, two-way set-associative, data and instruction translation lookaside buffers (DTLB and ITLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation. The TLBs and caches use a least-recently used (LRU) replacement algorithm. The 603e also supports block address translation through the use of two independent instruction and data block address translation (IBAT and DBAT) arrays of four entries each. Effective addresses are compared simultaneously with all four entries in the BAT array during block translation. In accordance with the PowerPC architecture, if an effective address hits in both the TLB and BAT array, the BAT translation takes priority.

The 603e has a selectable 32- or 64-bit data bus and a 32-bit address bus. The 603e interface protocol allows multiple masters to compete for system resources through a central external arbiter. The 603e provides a three-state coherency protocol that supports the exclusive, modified, and invalid cache states. This protocol is a compatible subset of the MESI (modified/exclusive/shared/invalid) four-state protocol and operates coherently in systems that contain four-state caches. The 603e supports single-beat and burst data transfers for memory accesses, and supports memory-mapped I/O.

The 603e uses an advanced, 2.5/3.3-V CMOS process technology and maintains full interface compatibility with TTL devices.

1.2 Features

This section summarizes features of the 603e's implementation of the PowerPC architecture. Major features of the 603e are as follows:

- High-performance, superscalar microprocessor
  - As many as three instructions issued and retired per clock
  - As many as five instructions in execution per clock
  - Single-cycle execution for most instructions
  - Pipelined FPU for all single-precision and most double-precision operations
- Five independent execution units and two register files
  - BPU featuring static branch prediction
  - A 32-bit IU
  - Fully IEEE 754-compliant FPU for both single- and double-precision operations
  - LSU for data transfer between data cache and GPRs and FPRs
  - SRU that executes condition register (CR), special-purpose register (SPR) instructions, and integer add/compare instructions
  - Thirty-two GPRs for integer operands
  - Thirty-two FPRs for single- or double-precision operands
- High instruction and data throughput
  - Zero-cycle branch capability (branch folding)
  - Programmable static branch prediction on unresolved conditional branches
  - Instruction fetch unit capable of fetching two instructions per clock from the instruction cache
  - A six-entry instruction queue that provides lookahead capability
  - Independent pipelines with feed-forwarding that reduces data dependencies in hardware
  - 16-Kbyte data cache—four-way set-associative, physically addressed; LRU replacement algorithm
  - 16-Kbyte instruction cache—four-way set-associative, physically addressed; LRU replacement algorithm
  - Cache write-back or write-through operation programmable on a per page or per block basis
  - BPU that performs CR lookahead operations
  - Address translation facilities for 4-Kbyte page size, variable block size, and 256-Mbyte segment size
  - A 64-entry, two-way set-associative ITLB
  - A 64-entry, two-way set-associative DTLB
  - Four-entry data and instruction BAT arrays providing 128-Kbyte to 256-Mbyte blocks
  - Software table search operations and updates supported through fast trap mechanism
  - 52-bit virtual address; 32-bit physical address
- Facilities for enhanced system performance
  - A 32- or 64-bit split-transaction external data bus with burst transfers
  - Support for one-level address pipelining and out-of-order bus transactions

- Integrated power management
  - — Low-power 2.5/3.3-volt design
  - — Internal processor/bus clock multiplier that provides 2/1, 2.5/1, 3/1, 3.5/1, 4/1, 4.5/1, 5/1, 5.5/1, and 6/1 ratios
  - — Three power saving modes: doze, nap, and sleep
  - — Automatic dynamic power reduction when internal functional units are idle
- In-system testability and debugging features through JTAG boundary-scan capability

1.3 General Parameters

The following list provides a summary of the general parameters of the PID7v-603e:

Technology	0.35 μm CMOS, five-layer metal
Die size	10.5 mm x 7.5 mm (79 mm^2)
Transistor count	2.6 million
Logic design	Fully-static
Package	Surface mount 240-pin ceramic quad flat pack (CQFP) or 255 ceramic ball grid array (BGA)
Core power supply	2.5 ± 5% V dc
I/O power supply	3.3 ± 5% V dc

1.4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the PID7v-603e.

1.4.1 DC Electrical Characteristics

The tables in this section describe the PID7v-603e DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 2 provides the recommended operating conditions for the PID7v-603e.

Table 1. Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Core supply voltage	Vdd	–0.3 to 2.75	V
PLL supply voltage	AVdd	–0.3 to 2.75	V
I/O supply voltage	OVdd	–0.3 to 3.6	V
Input voltage	V_{in}	–0.3 to 5.5	V
Storage temperature range	T_{stg}	–55 to 150	°C

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: V_{in} must not exceed OVdd by more than 2.5 V at any time, including during power-on reset.
3. **Caution**: OVdd must not exceed Vdd/AVdd by more than 1.2 V at any time, including during power-on reset.
4. **Caution**: Vdd/AVdd must not exceed OVdd by more than 0.4 V at any time, including during power-on reset.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit
Core supply voltage	Vdd	2.375 to 2.625	V
PLL supply voltage	AVdd	2.375 to 2.625	V
I/O supply voltage	OVdd	3.135 to 3.465	V
Input voltage	V_{in}	GND to 5.5	V
Junction temperature	Tj	0 to 105	°C

Note: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3 provides the package thermal characteristics for the PID7v-603e.

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Rating
Motorola wire-bond CQFP package thermal resistance, junction-to-case (typical)	θ_{JC}	2.2	°C/W
IBM C4-CQFP package thermal resistance, junction-to-case	θ_{JC}	3.6	°C/W
BGA package thermal resistance, junction-to-top-of-die	θ_{JC}	0.03	°C/W

Note: Refer to Section 1.8, “System Design Information,” for more details about thermal management.

Table 4 provides the DC electrical characteristics for the PID7v-603e.

Table 4. DC Electrical Specifications

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ Tj ≤ 105 °C

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	V_{IH}	2.0	5.5	V	
Input low voltage (all inputs except SYSCLK)	V_{IL}	GND	0.8	V	
SYSCLK input high voltage	CV_{IH}	2.4	5.5	V	
SYSCLK input low voltage	CV_{IL}	GND	0.4	V	
Input leakage current, V_{in} = 3.465 V	I_{in}	—	30	µA	1,2
V_{in} = 5.5 V	I_{in}	—	300	µA	1,2
Hi-Z (off-state) leakage current, V_{in} = 3.465 V	I_{TSI}	—	30	µA	1,2
V_{in} = 5.5 V	I_{TSI}	—	300	µA	1,2
Output high voltage, I_{OH} = –7 mA	V_{OH}	2.4	—	V	
Output low voltage, I_{OL} = 7 mA	V_{OL}	—	0.4	V	
Capacitance, V_{in} = 0 V, f = 1 MHz (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C_{in}	—	10.0	pF	3
Capacitance, V_{in} = 0 V, f = 1 MHz (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C_{in}	—	15.0	pF	3

Notes:

1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and JTAG signals).
2. The leakage is measured for nominal OVdd and Vdd or both OVdd and Vdd must vary in the same direction (for example, both OVdd and Vdd vary by either +5% or -5%).
3. Capacitance is periodically sampled rather than 100% tested.

Table 5 provides the power consumption for the PID7v-603e.

Table 5. Power Consumption

	Processor (CPU) Frequency						Unit
	160 MHz	166 MHz	180 MHz	200 MHz	220, 225 MHz	233, 240 MHz	
Full-On Mode (DPM Enabled)							
Typical	2.9	3.0	3.5	4.0	4.4	4.8	W
Maximum	3.8	4.0	4.5	5.0	5.5	6.0	W
Doze Mode							
Typical	1.2	1.2	1.4	1.5	1.7	1.8	W
Nap Mode							
Typical	75	80	100	120	132	140	mW
Sleep Mode							
Typical	65	70	80	100	110	120	mW
Sleep Mode—PLL Disabled							
Typical	60	60	60	60	60	60	mW
Sleep Mode—PLL and SYSCLK Disabled							
Maximum	60	60	60	60	60	60	mW

Notes:

1. These values apply for all valid PLL_CFG[0–3] settings and do not include output driver power (OVdd) or analog supply power (AVdd). OVdd power is system dependent but is typically ≤ 10% of Vdd. Worst-case AVdd = 15 mW.
2. Typical power is an average value measured at Vdd = AVdd = 2.5 V, OVdd = 3.3V, in a system executing typical applications and benchmark sequences.
3. Maximum power is measured at 2.625 V using a worst-case instruction mix.

1.4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the PID7v-603e. These specifications are for 160, 166, 180, 200, 225, 233, and 240 MHz processor core frequencies. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0–3] signals. All timings are specified respective to the rising edge of SYSCLK. PLL_CFG signals should be set prior to power up and not altered afterwards.

1.4.2.1 Clock AC Specifications

Table 6 provides the clock AC timing specifications as defined in Figure 1. After fabrication, parts are sorted by maxium processor core frequency as shown in Section 1.4.2.1, “Clock AC Specifications” and tested for conformance to the AC specifications for that frequency. Parts are sold by maximum processor core frequency; see Section 1.9, “Ordering Information.”

Table 6. Clock AC Timing Specifications

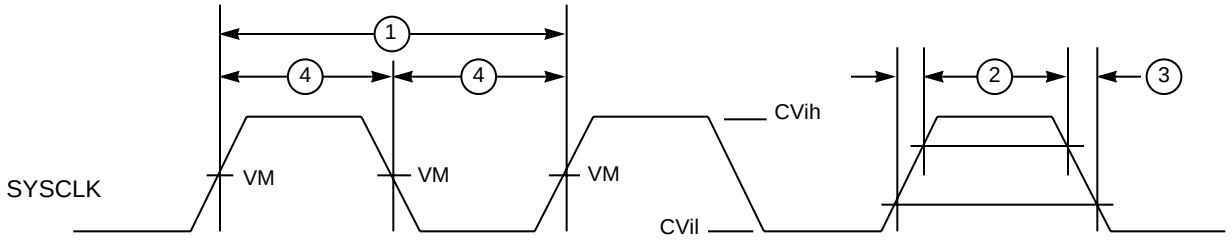
Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ Tj ≤ 105 °C

Num	Characteristic	160 MHz		166 MHz		180 MHz		200 MHz		220, 225 MHz		233, 240 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
	Processor frequency	125	160	125	167	125	180	125	200	125	220, 225	125	233, 240	MHz	1
	VCO frequency	250	320	250	333	250	360	250	400	250	440, 450	250	466, 480	MHz	1
	SYSCLK frequency	25	66.67	25	66.67	25	66.67	25	66.67	25	75	25	75	MHz	1
1	SYSCLK cycle time	15	40.0	15	40.0	15	40.0	15	40.0	13.3	40.0	13.3	40.0	ns	
2,3	SYSCLK rise and fall time	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	ns	2
4	SYSCLK duty cycle measured at 1.4 V	40.0	60.0	40.0	60.0	40.0	60.0	40.0	60.0	40.0	60.0	40.0	60.0	%	3
	SYSCLK jitter	—	±150	—	±150	—	±150	—	±150	—	±150	—	±150	ps	4
	603e internal PLL-relock time	—	100	—	100	—	100	—	100	—	100	—	100	µs	3,5

Notes:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0–3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0–3] signal description in Section 1.8, “System Design Information,” for valid PLL_CFG[0–3] settings.
2. Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4 V.
3. Timing is guaranteed by design and characterization, and is not tested.
4. Cycle-to-cycle jitter, and is guaranteed by design. The total input jitter (short term and long term combined) must be under ±150 ps.
5. Relock timing is guaranteed by design and characterization, and is not tested. PLL-relock time is the maximum time required for PLL lock after a stable Vdd, OVdd, AVdd, and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time (100 µs) during the power-on reset sequence.

Figure 1 provides the SYSCLK input timing diagram.



VM = Midpoint Voltage (1.4 V)

Figure 1. SYSCLK Input Timing Diagram

1.4.2.2 Input AC Specifications

Table 7 provides the input AC timing specifications for the PID7v-603e as defined in Figure 2 and Figure 3.

Table 7. Input AC Timing Specifications[1]

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ Tj ≤ 105° C

Num	Characteristic	160, 166, 180, 200 MHz		220, 225, 233, 240 MHz		Unit	Notes
		Min	Max	Min	Max		
10a	Address/data/transfer attribute inputs valid to SYSCLK (input setup)	2.5	—	2.5	—	ns	2
10b	All other inputs valid to SYSCLK (input setup)	4.0	—	3.5	—	ns	3
10c	Mode select inputs valid to $\overline{\text{HRESET}}$ (input setup) (for $\overline{\text{DRTRY}}$, $\overline{\text{QACK}}$ and $\overline{\text{TLBISYNC}}$)	8	—	8	—	t_{sysclk}	4, 5, 6, 7
11a	SYSCLK to address/data/transfer attribute inputs invalid (input hold)	1.0	—	1.0	—	ns	2

Table 7. Input AC Timing Specifications[1] (Continued)

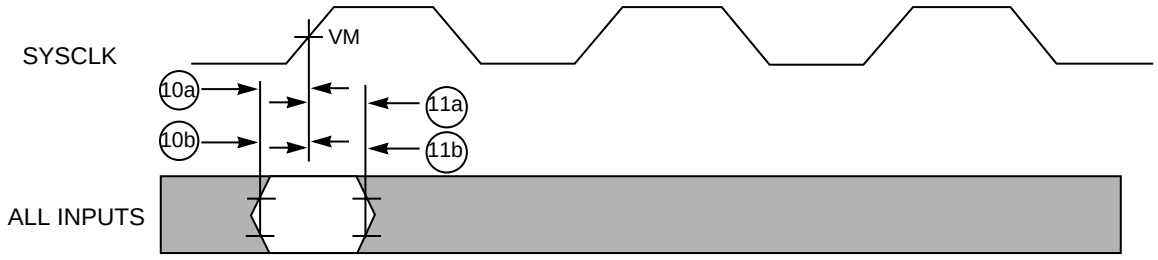
Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ Tj ≤ 105° C

Num	Characteristic	160, 166, 180, 200 MHz		220, 225, 233, 240 MHz		Unit	Notes
		Min	Max	Min	Max		
11b	SYSCLK to all other inputs invalid (input hold)	1.0	—	1.0	—	ns	3
11c	$\overline{\text{HRESET}}$ to mode select inputs invalid (input hold) (for $\overline{\text{DRTRY}}$, $\overline{\text{QACK}}$, and $\overline{\text{TLBISYNC}}$)	0	—	0	—	ns	4, 6, 7

Notes:

1. Input specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V of the rising edge of the input SYSCLK. Input and output timings are measured at the pin.
2. Address/data/transfer attribute input signals are composed of the following—A[0–31], AP[0–3], TT[0–4], TC[0–1], $\overline{\text{TBST}}$, TSIZ[0-2], $\overline{\text{GBL}}$, DH[0–31], DL[0–31], DP[0–7].
3. All other input signals are composed of the following—$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{AACK}}$, $\overline{\text{DBG}}$, $\overline{\text{DBWO}}$, $\overline{\text{TA}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TEA}}$, $\overline{\text{DBDIS}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{INT}}$, $\overline{\text{SMI}}$, $\overline{\text{MCP}}$, TBEN, $\overline{\text{QACK}}$, $\overline{\text{TLBISYNC}}$.
4. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 3).
5. t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. These values are guaranteed by design, and are not tested.
7. This specification is for configuration mode only. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 2 provides the input timing diagram for the PID7v-603e.



VM = Midpoint Voltage (1.4 V)

Figure 2. Input Timing Diagram

Figure 3 provides the mode select input timing diagram for the PID7v-603e.

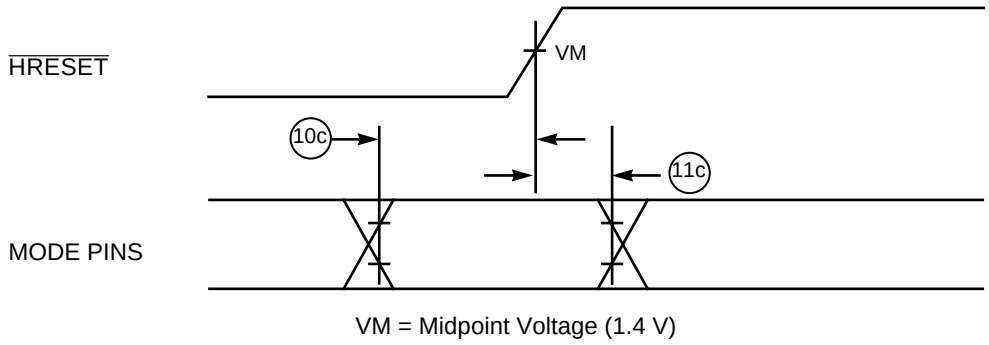


Figure 3. Mode Select Input Timing Diagram

1.4.2.3 Output AC Specifications

Table 8 provides the output AC timing specifications for the PID7v-603e as defined in Figure 4.

Table 8. Output AC Timing Specifications[1]

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5%, GND = 0 V dc, 0 ≤ Tj ≤ 105 °C, C_L = 50 pF (unless otherwise noted)

Num	Characteristic	160, 166, 180, 200 MHz		220, 225, 233, 240 MHz		Unit	Notes
		Min	Max	Min	Max		
12	SYSCLK to output driven (output enable time)	1.0	—	1.0	—	ns	
13a	SYSCLK to output valid (5.5 V to 0.8 V—$\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	9.0	—	9.0	ns	3
13b	SYSCLK to output valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	8.0	—	8.0	ns	5
14a	SYSCLK to output valid (5.5 V to 0.8 V—all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	11.0	—	11.0	ns	3
14b	SYSCLK to output valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	9.0	—	9.0	ns	5
15	SYSCLK to output invalid (output hold)	1.0	—	1.0	—	ns	2
16	SYSCLK to output high impedance (all except $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$)	—	8.5	—	8.0	ns	
17	SYSCLK to $\overline{ABB}$, $\overline{DBB}$, high impedance after precharge	—	1.0	—	1.0	t_{sysclk}	4, 6
18	SYSCLK to $\overline{ARTRY}$ high impedance before precharge	—	8.0	—	7.5	ns	

Table 8. Output AC Timing Specifications[1] (Continued)

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5%, GND = 0 V dc, 0 ≤ Tj ≤ 105 °C, C_L = 50 pF (unless otherwise noted)

Num	Characteristic	160, 166, 180, 200 MHz		220, 225, 233, 240 MHz		Unit	Notes
		Min	Max	Min	Max		
19	SYSCLK to $\overline{\text{ARTRY}}$ precharge enable	0.2 * t_{sysclk} + 1.0	—	0.2 * t_{sysclk} + 1.0	—	ns	2, 4, 7
20	Maximum delay to $\overline{\text{ARTRY}}$ precharge	—	1.0	—	1.0	t_{sysclk}	4, 7
21	SYSCLK to $\overline{\text{ARTRY}}$ high impedance after precharge	—	2.0	—	2.0	t_{sysclk}	5,7

Notes:

1. All output specifications are measured from the 1.4 V of the rising edge of SYSCLK to the TTL level (0.8 V or 2.0 V) of the signal in question. Both input and output timings are measured at the pin (see Figure 4).
2. This minimum parameter assumes C_L = 0 pF.
3. SYSCLK to output valid (5.5 V to 0.8 V) includes the extra delay associated with discharging the external voltage from 5.5 V to 0.8 V instead of from Vdd to 0.8 V (5-V CMOS levels instead of 3.3-V CMOS levels).
4. t_{sysclk} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
5. Output signal transitions from GND to 2.0 V or Vdd to 0.8 V.
6. Nominal precharge width for $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ is 0.5 t_{sysclk}.
7. Nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{sysclk}.

Figure 4 provides the output timing diagram for the PID7v-603e.

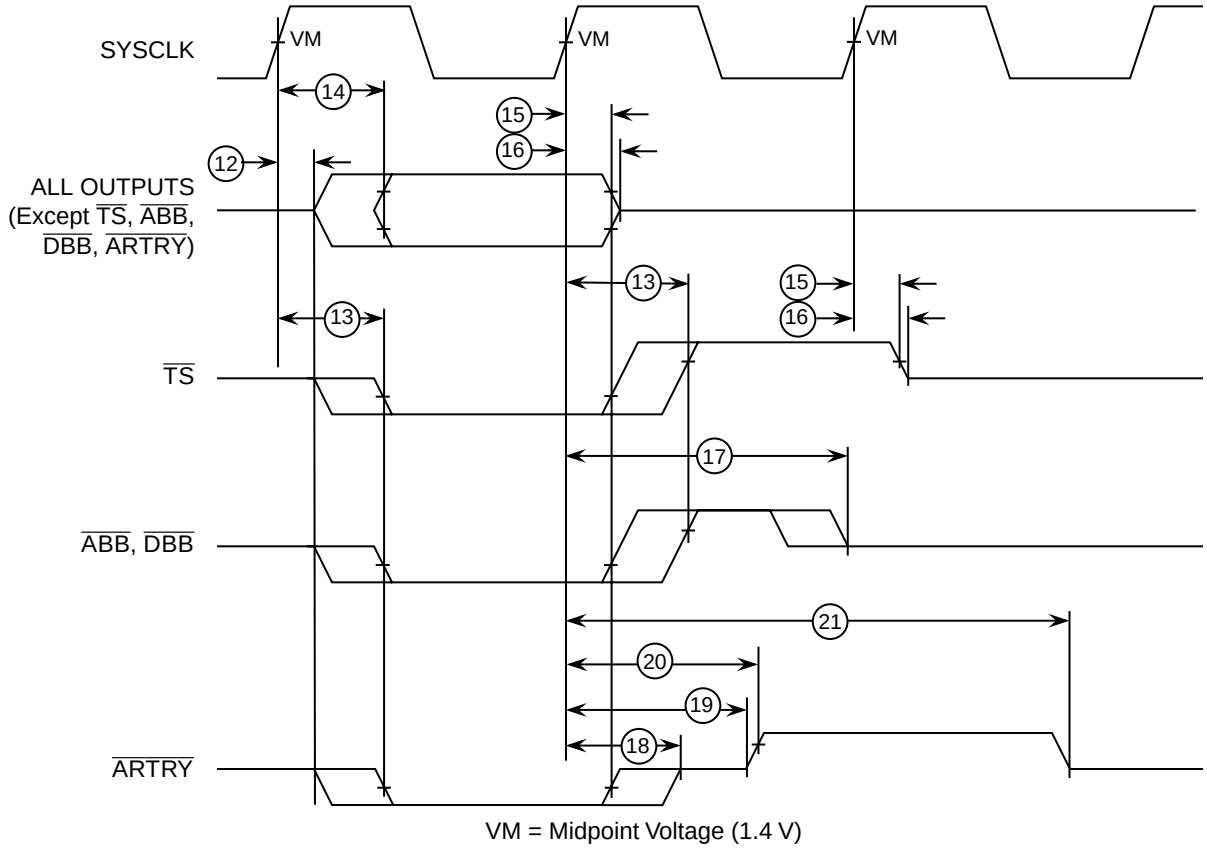


Figure 4. Output Timing Diagram

1.4.3 JTAG AC Timing Specifications

Table 9 provides the JTAG AC timing specifications as defined in Figure 5, Figure 6, Figure 7 and Figure 8.

Table 9. JTAG AC Timing Specifications

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5%, GND = 0 V dc, 0 ≤ Tj ≤ 105° C, C_L = 50 pF

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	16	MHz	
1	TCK cycle time	62.5	—	ns	
2	TCK clock pulse width measured at 1.4 V	25	—	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{\text{TRST}}$ setup time to TCK rising edge	13	—	ns	1
5	$\overline{\text{TRST}}$ assert time	40	—	ns	
6	Boundary scan input data setup time	6	—	ns	2
7	Boundary scan input data hold time	27	—	ns	2
8	TCK to output data valid	4	25	ns	3
9	TCK to output high impedance	3	24	ns	3
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	25	—	ns	
12	TCK to TDO data valid	4	24	ns	
13	TCK to TDO high impedance	3	15	ns	

Notes:

1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Non-test signal input timing with respect to TCK.
3. Non-test signal output timing with respect to TCK.

Figure 5 provides the JTAG clock input timing diagram.

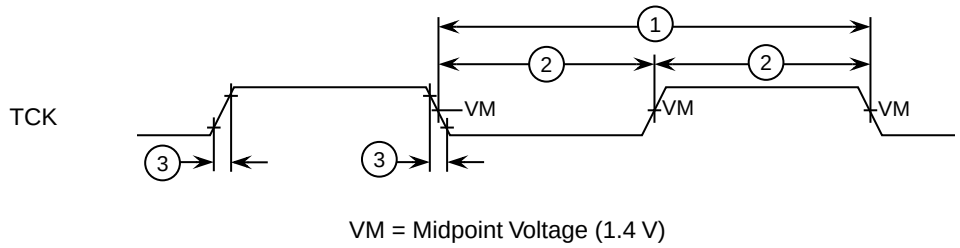


Figure 5. JTAG Clock Input Timing Diagram

Figure 6 provides the $\overline{\text{TRST}}$ timing diagram.

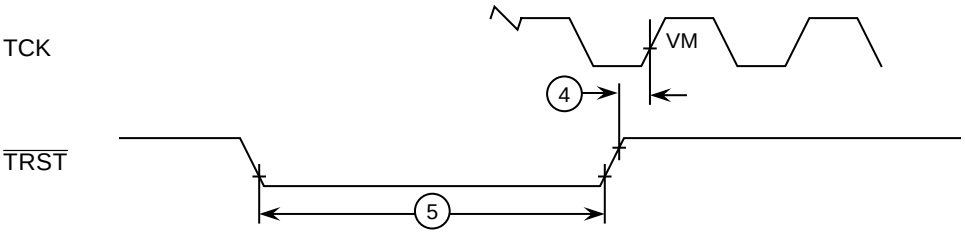


Figure 6. $\overline{\text{TRST}}$ Timing Diagram

Figure 7 provides the boundary-scan timing diagram.

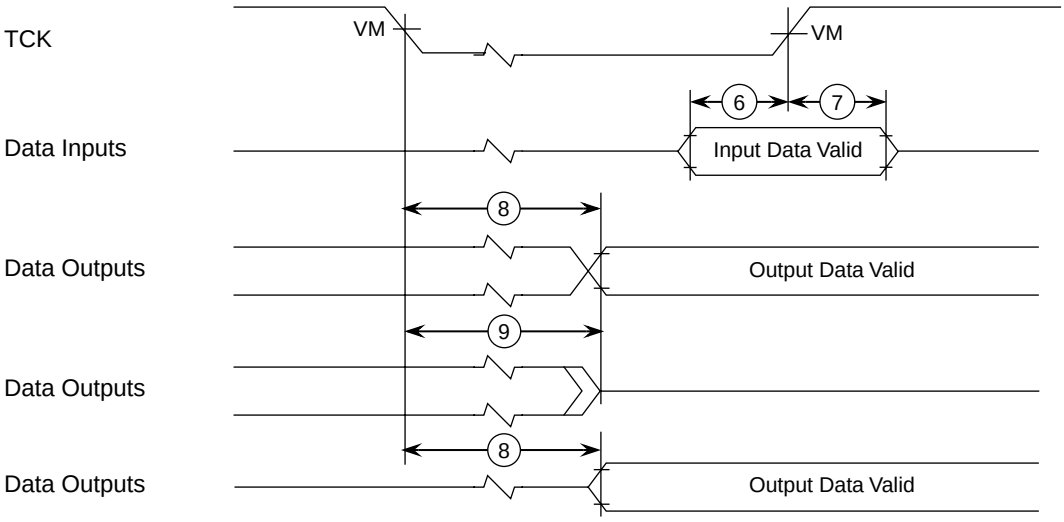


Figure 7. Boundary-Scan Timing Diagram

Figure 8 provides the test access port timing diagram.

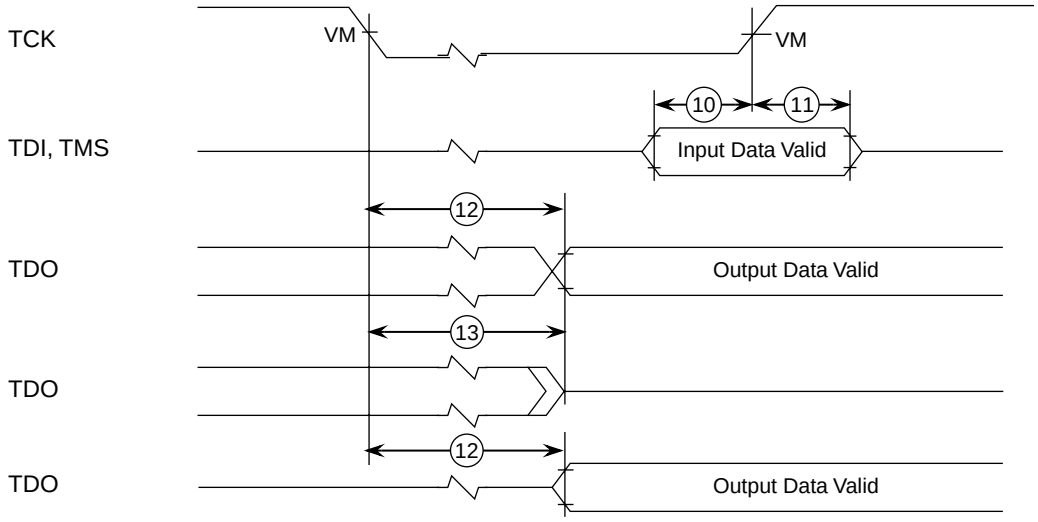


Figure 8. Test Access Port Timing Diagram

1.5 PowerPC 603e Microprocessor Pin Assignments

The following sections contain the pinout diagrams for the 603e. Note that the 603e is offered in both ceramic quad flat pack (CQFP) and ceramic ball grid array (BGA) packages.

1.5.1 Pinout Diagram for the CQFP Package

Figure 9 contains the CQFP pin assignments for the 603e.

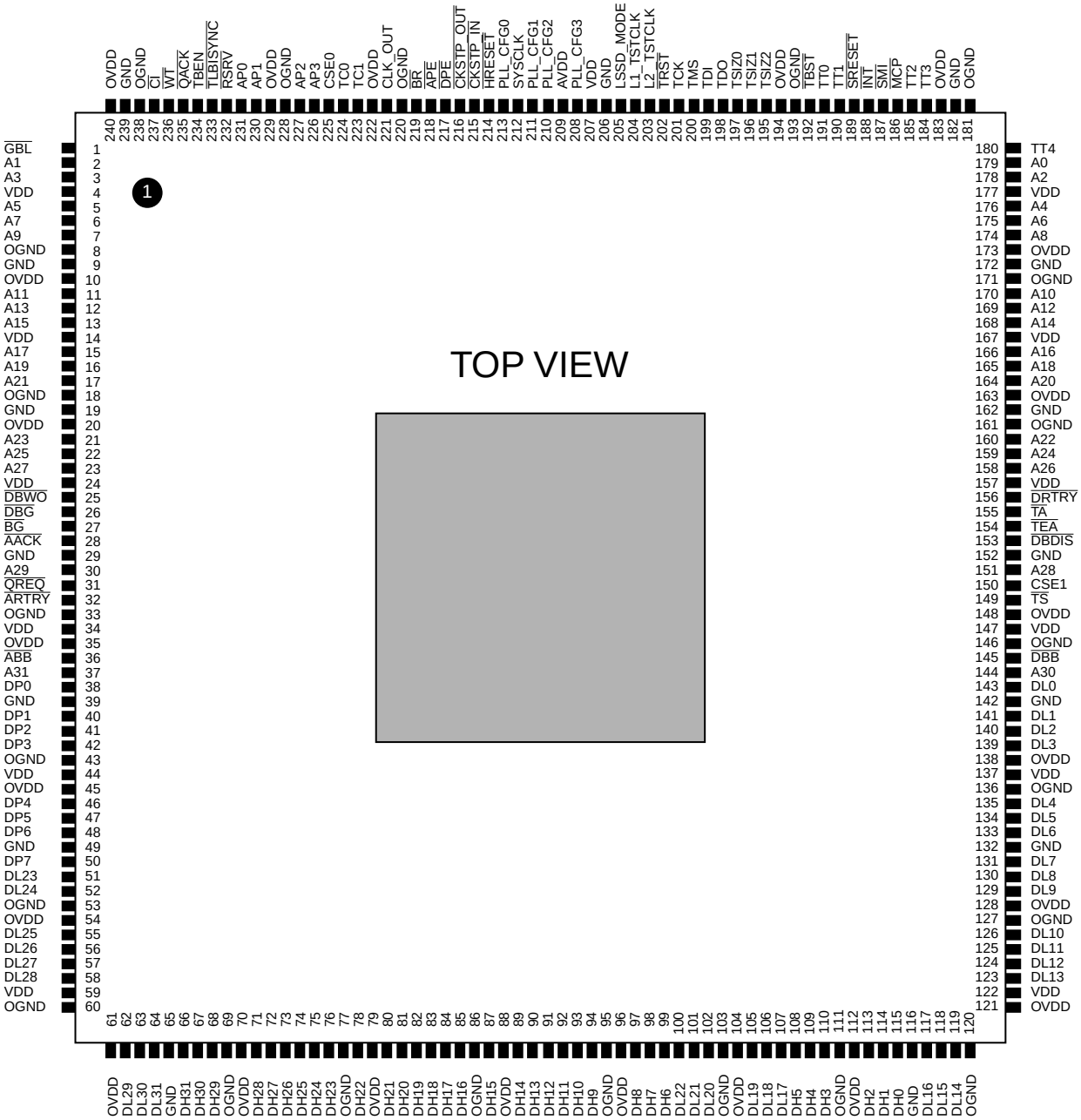
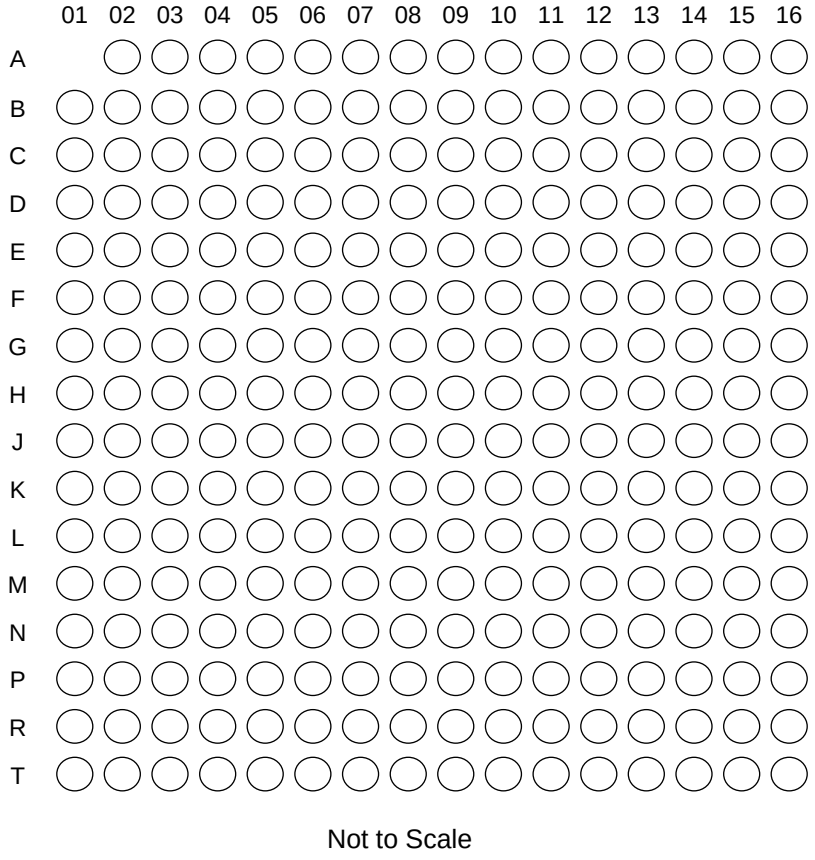


Figure 9. Pinout of the CQFP Package

1.5.2 Pinout Diagram for the BGA Package

Figure 10 (in part A) shows the pinout of the BGA package as viewed from the top surface. Part B shows the side profile of the BGA package to indicate the direction of the top surface view.

Part A



Part B

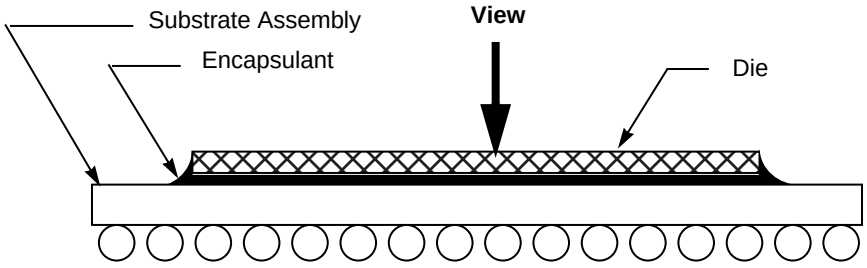


Figure 10. Pinout of the BGA Package as Viewed from the Top Surface

1.6 PowerPC 603e Microprocessor Pinout Listings

The following sections provide the pinout listings for the 603e CQFP and BGA packages.

1.6.1 Pinout Listing for the CQFP Package

Table 10 provides the pinout listing for the 603e CQFP package.

Table 10. Pinout Listing for the 240-pin CQFP Package

Signal Name	Pin Number	Active	I/O
A[0–31]	179, 2, 178, 3, 176, 5, 175, 6, 174, 7, 170, 11, 169, 12, 168, 13, 166, 15, 165, 16, 164, 17, 160, 21, 159, 22, 158, 23, 151, 30, 144, 37	High	I/O
$\overline{\text{AACK}}$	28	Low	Input
$\overline{\text{ABB}}$	36	Low	I/O
AP[0–3]	231, 230, 227, 226	High	I/O
$\overline{\text{APE}}$	218	Low	Output
$\overline{\text{ARTRY}}$	32	Low	I/O
AVDD	209	High	Input
$\overline{\text{BG}}$	27	Low	Input
$\overline{\text{BR}}$	219	Low	Output
$\overline{\text{CI}}$	237	Low	Output
CLK_OUT	221	—	Output
$\overline{\text{CKSTP\_IN}}$	215	Low	Input
$\overline{\text{CKSTP\_OUT}}$	216	Low	Output
CSE[0–1][1]	225, 150	High	Output
$\overline{\text{DBB}}$	145	Low	I/O
$\overline{\text{DBDIS}}$	153	Low	Input
$\overline{\text{DBG}}$	26	Low	Input
$\overline{\text{DBWO}}$	25	Low	Input
DH[0–31]	115, 114, 113, 110, 109, 108, 99, 98, 97, 94, 93, 92, 91, 90, 89, 87, 85, 84, 83, 82, 81, 80, 78, 76, 75, 74, 73, 72, 71, 68, 67, 66	High	I/O
DL[0–31]	143, 141, 140, 139, 135, 134, 133, 131, 130, 129, 126, 125, 124, 123, 119, 118, 117, 107, 106, 105, 102, 101, 100, 51, 52, 55, 56, 57, 58, 62, 63, 64	High	I/O
DP[0–7]	38, 40, 41, 42, 46, 47, 48, 50	High	I/O
$\overline{\text{DPE}}$	217	Low	Output
$\overline{\text{DRTRY}}$	156	Low	Input

Table 10. Pinout Listing for the 240-pin CQFP Package (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{\text{GBL}}$	1	Low	I/O
GND	9, 19, 29, 39, 49, 65, 116, 132, 142, 152, 162, 172, 182, 206, 239	Low	Input
$\overline{\text{HRESET}}$	214	Low	Input
$\overline{\text{INT}}$	188	Low	Input
LSSD_MODE[2]	205	Low	Input
L1_TSTCLK[2]	204	—	Input
L2_TSTCLK[2]	203	—	Input
$\overline{\text{MCP}}$	186	Low	Input
OGND	8, 18, 33, 43, 53, 60, 69, 77, 86, 95, 103, 111, 120, 127, 136, 146, 161, 171, 181, 193, 220, 228, 238	Low	Input
OVDD[3]	10, 20, 35, 45, 54, 61, 70, 79, 88, 96, 104, 112, 121, 128, 138, 148, 163, 173, 183, 194, 222, 229, 240	High	Input
PLL_CFG[0–3]	213, 211, 210, 208	High	Input
$\overline{\text{QACK}}$	235	Low	Input
$\overline{\text{QREQ}}$	31	Low	Output
$\overline{\text{RSRV}}$	232	Low	Output
$\overline{\text{SMI}}$	187	Low	Input
$\overline{\text{SRESET}}$	189	Low	Input
SYSCLK	212	—	Input
$\overline{\text{TA}}$	155	Low	Input
TBEN	234	High	Input
$\overline{\text{TBST}}$	192	Low	I/O
TC[0–1]	224, 223	High	Output
TCK	201	—	Input
TDI	199	High	Input
TDO	198	High	Output
$\overline{\text{TEA}}$	154	Low	Input
$\overline{\text{TLBISYNC}}$	233	Low	Input
TMS	200	High	Input
$\overline{\text{TRST}}$	202	Low	Input

Table 10. Pinout Listing for the 240-pin CQFP Package (Continued)

Signal Name	Pin Number	Active	I/O
TSIZ[0–2]	197, 196, 195	High	Output
$\overline{TS}$	149	Low	I/O
TT[0–4]	191, 190, 185, 184, 180	High	I/O
VDD[3]	4, 14, 24, 34, 44, 59, 122, 137, 147, 157, 167, 177, 207	High	Input
$\overline{WT}$	236	Low	Output

Notes:

1. There are two CSE signals in the 603e—CSE0 and CSE1. The $\overline{XATS}$ signal in the PowerPC 603™ microprocessor is replaced by the CSE1 signal in both the PID6-603e and the PID7v-603e.
2. These are test signals for factory use only and must be pulled up to OVdd for normal machine operation.
3. OVdd inputs supply power to the I/O drivers and Vdd inputs supply power to the processor core.

1.6.2 Pinout Listing for the BGA Package

Table 11 provides the pinout listing for the 603e BGA package.

Table 11. Pinout Listing for the 255 BGA Package

Signal Name	Pin Number	Active	I/O
A[0–31]	C16, E04, D13, F02, D14, G01, D15, E02, D16, D04, E13, GO2, E15, H01, E16, H02, F13, J01, F14, J02, F15, H03, F16, F04, G13, K01, G15, K02, H16, M01, J15, P01	High	I/O
$\overline{AACK}$	L02	Low	Input
$\overline{ABB}$	K04	Low	I/O
AP[0–3]	C01, B04, B03, B02	High	I/O
$\overline{APE}$	A04	Low	Output
$\overline{ARTRY}$	J04	Low	I/O
AVDD	A10	—	—
$\overline{BG}$	L01	Low	Input
$\overline{BR}$	B06	Low	Output
$\overline{CI}$	E01	Low	Output
$\overline{CKSTP\_IN}$	D08	Low	Input
$\overline{CKSTP\_OUT}$	A06	Low	Output
CLK_OUT	D07	—	Output
CSE[0–1]	B01, B05	High	Output
$\overline{DBB}$	J14	Low	I/O
$\overline{DBG}$	N01	Low	Input
$\overline{DBDIS}$	H15	Low	Input

Table 11. Pinout Listing for the 255 BGA Package (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{\text{DBWO}}$	G04	Low	Input
DH[0–31]	P14, T16, R15, T15, R13, R12, P11, N11, R11,T12, T11, R10, P09, N09, T10, R09, T09, P08, N08, R08, T08, N07, R07, T07, P06, N06, R06, T06, R05, N05, T05, T04	High	I/O
DL[0–31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P03, N03, N04, R03, T01, T02, P04, T03, R04	High	I/O
DP[0–7]	M02, L03, N02, L04, R01, P02, M04, R02	High	I/O
$\overline{\text{DPE}}$	A05	Low	Output
$\overline{\text{DRTRY}}$	G16	Low	Input
$\overline{\text{GBL}}$	F01	Low	I/O
GND	C05, C12, E03, E06, E08, E09, E11, E14, F05, F07, F10, F12, G06, G08, G09, G11, H05, H07, H10, H12, J05, J07, J10, J12, K06, K08, K09, K11, L05, L07, L10, L12, M03, M06, M08, M09, M11, M14, P05, P12	—	—
$\overline{\text{HRESET}}$	A07	Low	Input
$\overline{\text{INT}}$	B15	Low	Input
L1_TSTCLK [1]	D11	—	Input
L2_TSTCLK [1]	D12	—	Input
LSSD_MODE [1]	B10	Low	Input
$\overline{\text{MCP}}$	C13	Low	Input
NC (No-Connect)	B07, B08, C03, C06, C08, D05, D06, H04, J16	—	—
OVDD	C07, E05, E07, E10, E12, G03, G05, G12, G14, K03, K05, K12, K14, M05, M07, M10, M12, P07, P10	—	—
PLL_CFG[0–3]	A08, B09, A09, D09	High	Input
$\overline{\text{QACK}}$	D03	Low	Input
$\overline{\text{QREQ}}$	J03	Low	Output
RSRV	D01	Low	Output
$\overline{\text{SMI}}$	A16	Low	Input
$\overline{\text{SRESET}}$	B14	Low	Input
SYSCLK	C09	—	Input
$\overline{\text{TA}}$	H14	Low	Input
TBEN	C02	High	Input
$\overline{\text{TBST}}$	A14	Low	I/O
TC[0–1]	A02, A03	High	Output

Table 11. Pinout Listing for the 255 BGA Package (Continued)

Signal Name	Pin Number	Active	I/O
TCK	C11	—	Input
TDI	A11	High	Input
TDO	A12	High	Output
$\overline{\text{TEA}}$	H13	Low	Input
$\overline{\text{TLBISYNC}}$	C04	Low	Input
TMS	B11	High	Input
$\overline{\text{TRST}}$	C10	Low	Input
$\overline{\text{TS}}$	J13	Low	I/O
TSIZ[0–2]	A13, D10, B12	High	Output
TT[0–4]	B13, A15, B16, C14, C15	High	I/O
$\overline{\text{WT}}$	D02	Low	Output
VDD[2]	F06, F08, F09, F11, G07, G10, H06, H08, H09, H11, J06, J08, J09, J11, K07, K10, L06, L08, L09, L11	—	—
VOLTDETGND[3]	F03	Low	Output

Notes:

1. These are test signals for factory use only and must be pulled up to OVdd for normal machine operation.
2. OVdd inputs supply power to the I/O drivers and Vdd inputs supply power to the processor core.
3. NC (no-connect) in the PID6-603e; internally tied to GND in the PID7v-603e BGA package to indicate to the power supply that a low-voltage processor is present.

1.7 PowerPC 603e Microprocessor Package Descriptions

The following sections provide the package parameters and the mechanical dimensions for the 603e. Note that the 603e is currently offered in two types of CQFP packages—the Motorola wire-bond CQFP and the IBM C4-CQFP, as well as a common ceramic ball grid array (BGA) package.

1.7.1 Motorola Wire-Bond CQFP Package Description

The following sections provide the package parameters and mechanical dimensions for the Motorola wire-bond CQFP package.

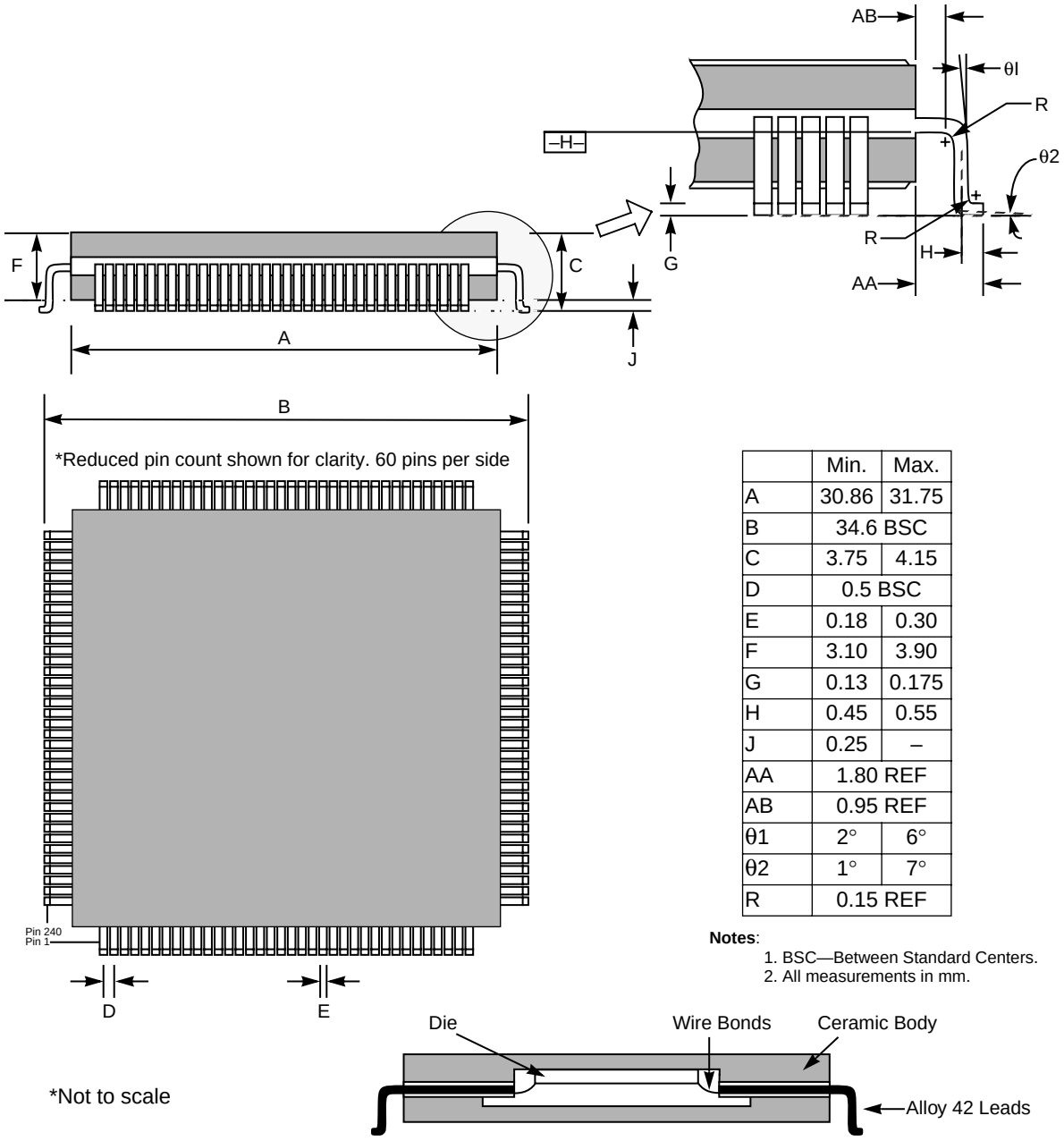
1.7.1.1 Package Parameters

The package parameters are as provided in the following list. The package type is 32 mm x 32 mm, 240-pin ceramic quad flat pack.

Package outline	32 mm x 32 mm
Interconnects	240
Pitch	0.5 mm (20 mil)

1.7.1.2 Mechanical Dimensions of the Motorola Wire-Bond CQFP Package

Figure 11 shows the mechanical dimensions for the wire-bond CQFP package.



	Min.	Max.
A	30.86	31.75
B	34.6 BSC	
C	3.75	4.15
D	0.5 BSC	
E	0.18	0.30
F	3.10	3.90
G	0.13	0.175
H	0.45	0.55
J	0.25	–
AA	1.80 REF	
AB	0.95 REF	
θ1	2°	6°
θ2	1°	7°
R	0.15 REF	

Notes:
1. BSC—Between Standard Centers.
2. All measurements in mm.

Figure 11. Mechanical Dimensions of the Motorola Wire-Bond CQFP Package

1.7.2 IBM C4-CQFP Package Description

The following sections provide the package parameters and mechanical dimensions for the IBM C4-CQFP package.

1.7.2.1 Package Parameters

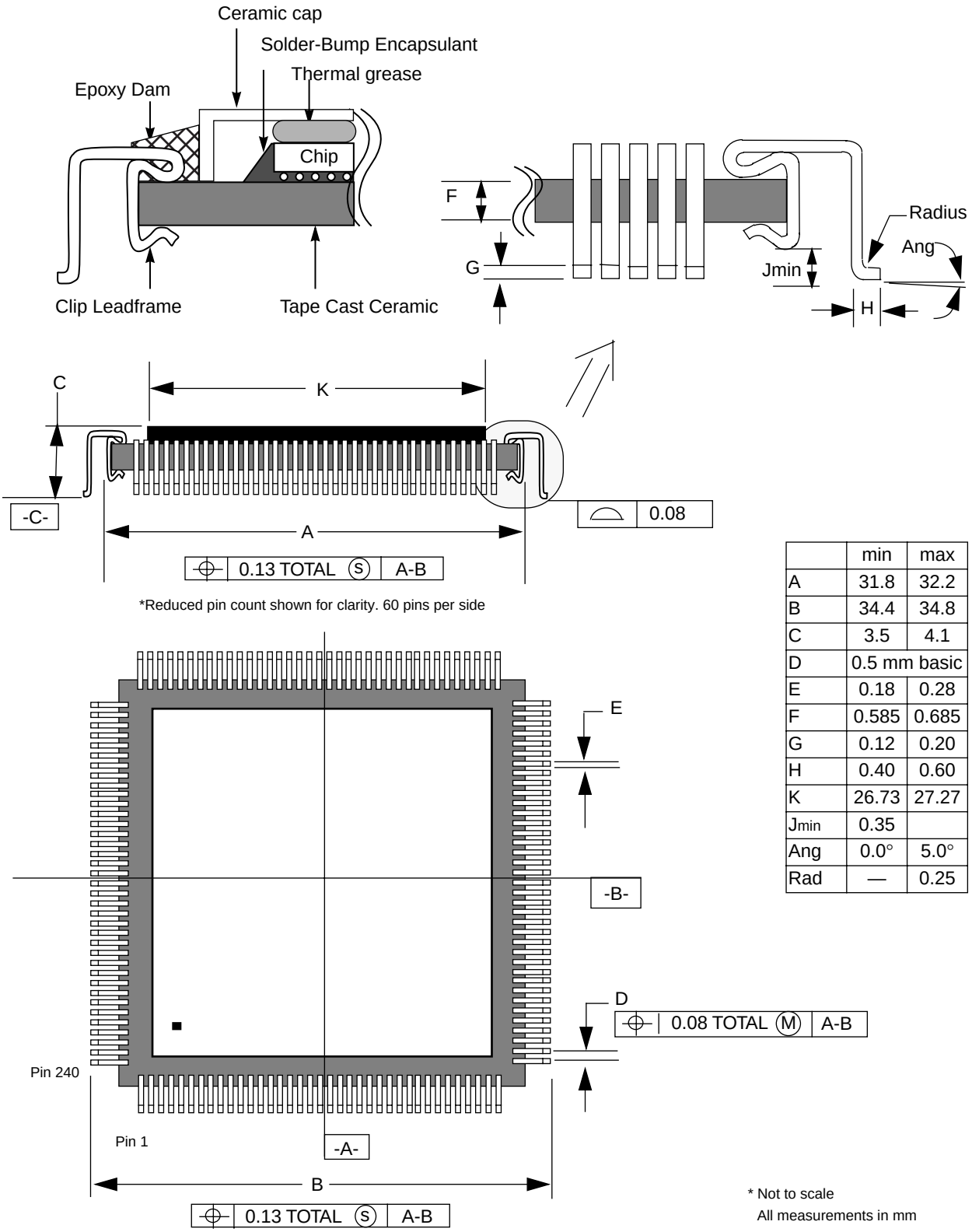
The package parameters are as provided in the following list. The package type is 32 mm x 32 mm, 240-pin ceramic quad flat pack.

Package outline	32 mm x 32 mm
Interconnects	240
Pitch	0.5 mm
Lead plating material	Ni Au
Lead plating thickness	Ni = 50 ± 25 μ-inch Au = 13 ± 5 μ-inch
Solder joint	Sn/PB (10/90)
Lead encapsulation	Epoxy
Solder-bump encapsulation	Epoxy
Maximum module height	4.1 mm
Co-planarity specification	0.08 mm

Note: No solvent can be used with the C4-CQFP package. See Appendix A, “General Handling Recommendations for the C4-CQFP Package,” for details.

1.7.2.2 Mechanical Dimensions of the IBM C4-CQFP Package

Figure 12 shows the mechanical dimensions for the C4-CQFP package.



	min	max
A	31.8	32.2
B	34.4	34.8
C	3.5	4.1
D	0.5 mm basic	
E	0.18	0.28
F	0.585	0.685
G	0.12	0.20
H	0.40	0.60
K	26.73	27.27
Jmin	0.35	
Ang	0.0°	5.0°
Rad	—	0.25

Figure 12. Mechanical Dimensions of the IBM Solder-Bump CQFP Package

1.7.3 BGA Package Description

The following sections provide the package parameters and mechanical dimensions for the Motorola and IBM BGA packages.

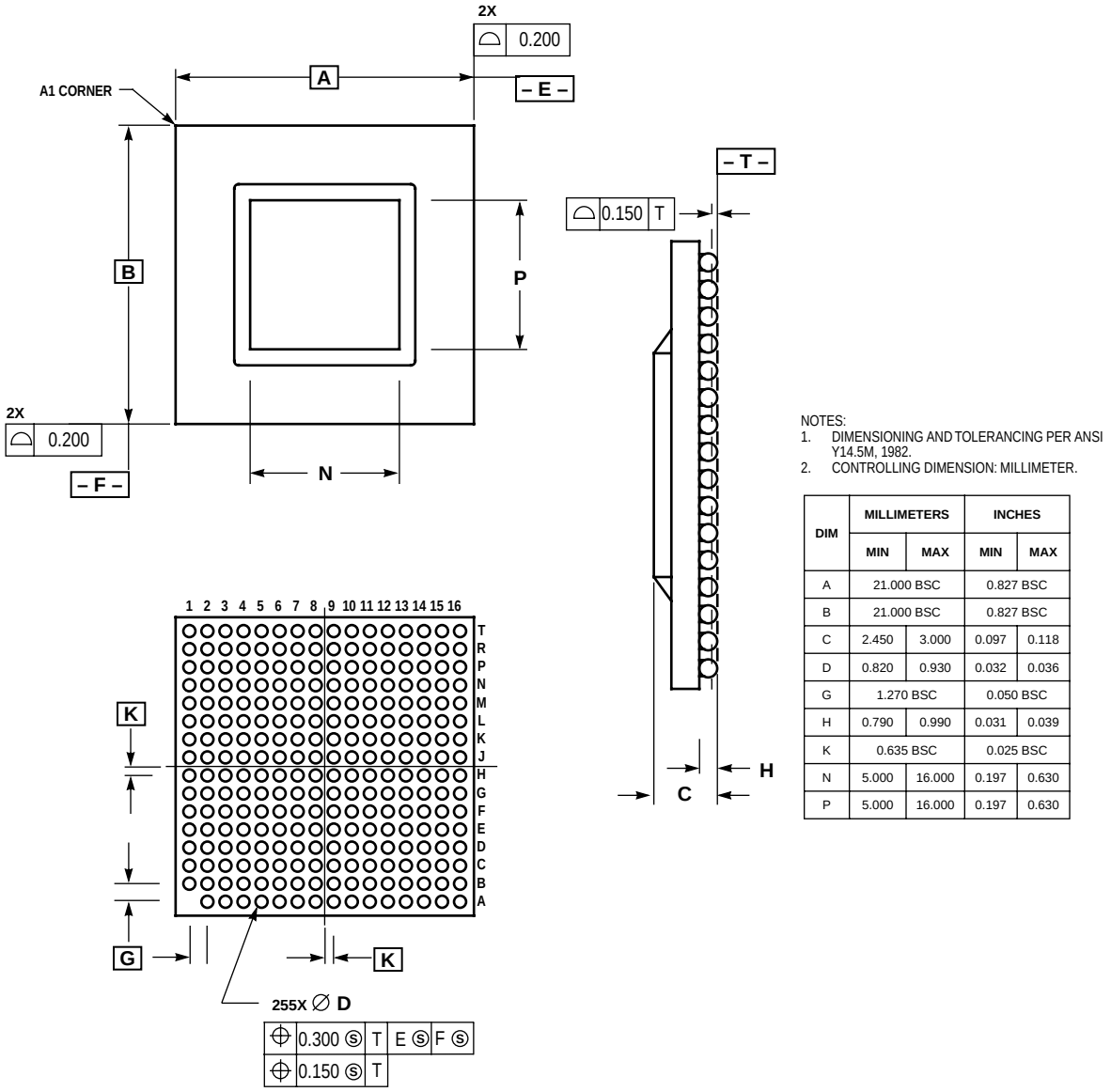
1.7.3.1 Package Parameters

The package parameters are as provided in the following list. The package type is 21 mm x 21 mm, 255-lead ceramic ball grid array (BGA).

Package outline	21 mm x 21 mm
Interconnects	255
Pitch	1.27 mm (50 mil)
Package height	Minimum: 2.45 mm Maximum: 3.00 mm
Ball diameter	0.89 mm (35 mil)
Maximum heat sink force	10 lbs

1.7.3.2 Mechanical Dimensions of the BGA Package

Figure 13 provides the mechanical dimensions and bottom surface nomenclature of the Motorola and IBM BGA package.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	21.000 BSC		0.827 BSC	
B	21.000 BSC		0.827 BSC	
C	2.450	3.000	0.097	0.118
D	0.820	0.930	0.032	0.036
G	1.270 BSC		0.050 BSC	
H	0.790	0.990	0.031	0.039
K	0.635 BSC		0.025 BSC	
N	5.000	16.000	0.197	0.630
P	5.000	16.000	0.197	0.630

Figure 13. Mechanical Dimensions and Bottom Surface Nomenclature of the BGA Package

1.8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the 603e.

1.8.1 PLL Configuration

The 603e PLL is configured by the PLL_CFG[0–3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the PID7v-603e is shown in Table 12 for nominal frequencies.

Table 12. PowerPC PID7v-603e Microprocessor PLL Configuration

PLL_CFG[0–3]	CPU Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	**Core-to VCO Multiplier**	**Bus 25 MHz**	**Bus 33.33 MHz**	**Bus 40 MHz**	**Bus 50 MHz**	**Bus 60 MHz**	**Bus 66.67 MHz**	**Bus 75 MHz**
0100	2x	2x	—	—	—	—	—	133 (266)	150 (300)
0101	2x	4x	—	—	—	—	—	—	—
0110	2.5x	2x	—	—	—	125 (250)	150 (300)	166 (333)	187 (375)
1000	3x	2x	—	—	120 (240)	150 (300)	180 (360)	200 (400)	225 (450)
1110	3.5x	2x	—	—	140 (280)	175 (350)	210 (420)	233 (466)	
1010	4x	2x	—	133 (266)	160 (320)	200 (400)	240 (480)		
0111	4.5x	2x	—	150 (300)	180 (360)	225 (450)	—	—	—
1011	5x	2x	125 (250)	166 (333)	200 (400)	—	—	—	—
1001	5.5x	2x	137 (275)	183 (366)	220 (440)	—	—	—	—
1101	6x	2x	150 (300)	200 (400)	240 (480)	—	—	—	—
0011	PLL bypass								
1111	Clock off								

Notes:

1. Some PLL configurations may select bus, CPU, or VCO frequencies which are not supported; see Section 1.4.2.1, “Clock AC Specifications,” for valid SYSCLK and VCO frequencies.
2. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
3. In clock-off mode, no clocking occurs inside the 603e regardless of the SYSCLK input.

1.8.2 PLL Power Supply Filtering

The AVdd power signal is provided on the 603e to provide power to the clock generation phase-locked loop. To ensure stability of the internal clock, the power supplied to the AVdd input signal should be filtered using a circuit similar to the one shown in Figure 14. The circuit should be placed as close as possible to the AVdd pin to ensure it filters out as much noise as possible. The 0.1 μF capacitor should be closest to the AVdd pin, followed by the 10 μF capacitor, and finally the 10 Ω resistor to Vdd. These traces should be kept short and direct.

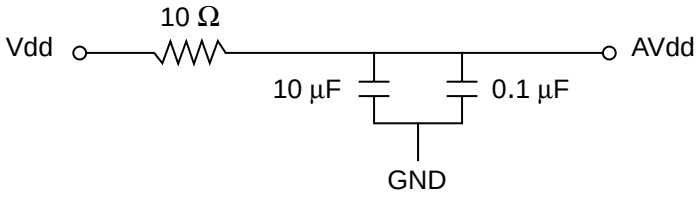


Figure 14. PLL Power Supply Filter Circuit

1.8.3 Decoupling Recommendations

Due to the 603e's dynamic power management feature, large address and data buses, and high operating frequencies, the 603e can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the 603e system, and the 603e itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each Vdd and OVdd pin of the 603e. It is also recommended that these decoupling capacitors receive their power from separate Vdd, OVdd, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should vary in value from 220 pF to 10 μF to provide both high- and low-frequency filtering, and should be placed as close as possible to their associated Vdd or OVdd pin. Suggested values for the Vdd pins—220 pF (ceramic), 0.01 μF (ceramic), and 0.1 μF (ceramic). Suggested values for the OVdd pins—0.01 μF (ceramic), 0.1 μF (ceramic), and 10 μF (tantalum). Only SMT (surface mount technology) capacitors should be used to minimize lead inductance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the Vdd and OVdd planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should also have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100 μF (AVX TPS tantalum) or 330 μF (AVX TPS tantalum).

1.8.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to Vdd. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external Vdd, OVdd, and GND pins of the 603e.

1.8.5 Pull-up Resistor Requirements

The 603e requires high-resistive (weak: 10 KΩ) pull-up resistors on several control signals of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the 603e or other bus master. These signals are—$\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$.

In addition, the 603e has three open-drain style outputs that require pull-up resistors (weak or stronger: 4.7 KΩ–10 KΩ) if they are used by the system. These signals are—$\overline{\text{APE}}$, $\overline{\text{DPE}}$, and $\overline{\text{CKSTP\_OUT}}$.

During inactive periods on the bus, the address and transfer attributes on the bus are not driven by any master and may float in the high-impedance state for relatively long periods of time. Since the 603e must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the 603e. It is recommended that these signals be pulled up through weak (10 KΩ) pull-up resistors or restored in some manner by the system. The snooped address and transfer attribute inputs are—A[0–31], AP[0–3], TT[0–4], $\overline{\text{TBST}}$, and $\overline{\text{GBL}}$.

The data bus input receivers are normally turned off when no read operation is in progress and do not require pull-up resistors on the data bus.

1.8.6 Thermal Management Information

This section provides thermal management data for the 603e; the information found in the first sub-sections (Section 1.8.6.1.1, “Thermal Characteristics,” through Section 1.8.6.2.2, “Thermal Management Example”) is based on a typical desktop configuration using a 240 lead, 32 mm x 32 mm, Motorola wire-bond CQFP package and an IBM C4-CQFP package. The heat sink used for this data is a pinfin configuration from Thermalloy, part number 2338. The IBM C4-CQFP also uses a flat aluminum plate with dimensions of 24 x 24 mm and 1.5 mm thickness. The data found in the subsequent sub-sections concerns 603e’s packaged in the 255-lead 21 mm multi-layer ceramic (MLC), ceramic BGA package. Data is shown for two cases, the exposed-die case (no heat sink) and using the Thermalloy 2338-pin fin heat sink.

1.8.6.1 Motorola Wire-Bond CQFP Package

This section provides thermal management data for the 603e; this information is based on a typical desktop configuration using a 240 lead, 32 mm x 32 mm, Motorola wire-bond CQFP package. The heat sink used for this data is a pinfin configuration from Thermalloy, part number 2338.

1.8.6.1.1 Thermal Characteristics

The thermal characteristics for a wire-bond CQFP package are as follows:

Thermal resistance (junction-to-case) = $R_{\theta jc}$ or θ_{jc} = 2.2° C/Watt (junction-to-case)

1.8.6.1.2 Thermal Management Example

The following example is based on a typical desktop configuration using a Motorola wire-bond CQFP package. The heat sink used for this data is a pinfin heat sink #2338 attached to the wire-bond CQFP package with thermal grease.

Figure 15 provides a thermal management example for the Motorola CQFP package.

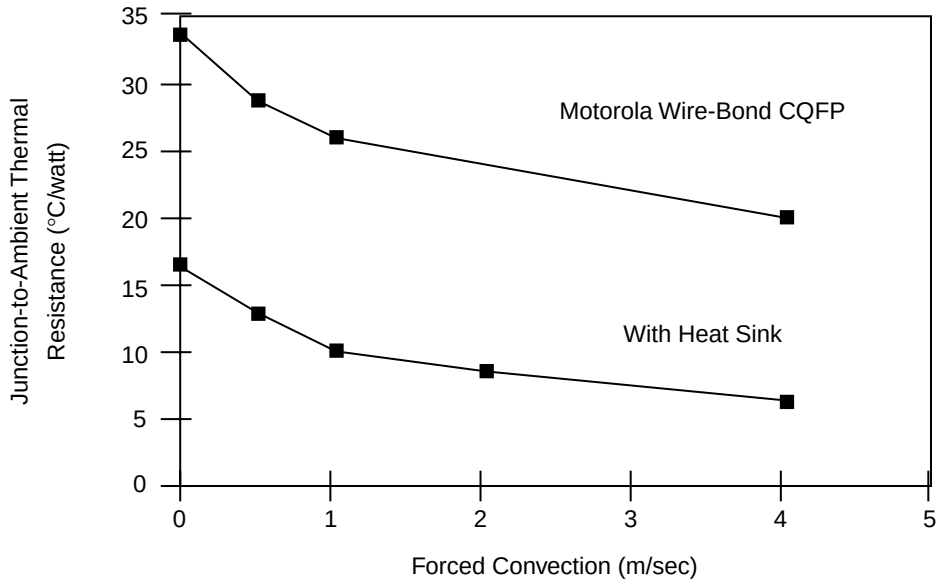


Figure 15. Motorola CQFP Thermal Management Example

The junction temperature can be calculated from the junction-to-ambient thermal resistance, as follows:

Junction temperature: $T_j = T_a + R_{\theta ja} * P$

or

$T_j = T_a + (R_{\theta jc} + R_{cs} + R_{sa}) * P$

Where:

T_a is the ambient temperature in the vicinity of the device

$R_{\theta ja}$ is the junction-to-ambient thermal resistance

$R_{\theta jc}$ is the junction-to-case thermal resistance of the device

R_{cs} is the case-to-heat sink thermal resistance of the interface material

R_{sa} is the heat sink-to-ambient thermal resistance

P is the power dissipated by the device

In this environment, it can be assumed that all the heat is dissipated to the ambient through the heat sink, so the junction-to-ambient thermal resistance is the sum of the resistances from the junction to the case, from the case to the heat sink, and from the heat sink to the ambient.

Note that verification of external thermal resistance and case temperature should be performed for each application. Thermal resistance can vary considerably due to many factors including degree of air turbulence.

For a power dissipation of 2.5 Watts in an ambient temperature of 40 °C at 1 m/sec with the heat sink measured above, the junction temperature of the device would be as follows:

$T_j = T_a + R_{\theta ja} * P$

$T_j = 40\ °C + (10\ °C/Watt * 2.5\ Watts) = 65\ °C$

which is well within the reliability limits of the device.

Notes:

1. Junction-to-ambient thermal resistance is based on measurements on single-sided printed circuit boards per SEMI (Semiconductor Equipment and Materials International) G38-87 in natural convection.
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88 with the exception that the cold plate temperature is used for the case temperature.

The vendors who supply heat sinks are Aavid Engineering, IERC, Thermalloy, and Wakefield Engineering. Contact information for these vendors follows:

Thermalloy 214-243-4321
2021 W. Valley View Lane
P.O. Box 810839
Dallas, TX 75731

International Electronic Research Corporation (IERC) 818-842-7277
135 W. Magnolia Blvd.
Burbank, CA 91502

Aavid Engineering 603-528-3400
One Kool Path
Laconic, NH 03247-0440

Wakefield Engineering 617-245-5900
60 Audubon Rd.
Wakefield, MA 01880

Any of these vendors can supply heat sinks with sufficient thermal performance.

1.8.6.2 IBM C4-CQFP Package

This section provides thermal management data for the 603e; this information is based on a typical desktop configuration using a 240 lead, 32 mm x 32 mm, IBM C4-CQFP package. The heat sink used for this data is a pinfin configuration from Thermalloy, part number 2338 and a flat aluminum plate with dimensions of 24 x 24 mm and 1.5 mm thickness.

1.8.6.2.1 Thermal Characteristics

The thermal characteristics for a C4-CQFP package are as follows:

Thermal resistance (junction-to-heat sink) = $R_{\theta js}$ or θ_{js} = 0.03° C/Watt (junction-to-heat sink)

1.8.6.2.2 Thermal Management Example

The following example is based on a typical desktop configuration using an IBM C4-CQFP package. The heat sink used for this data is a pinfin heat sink #2338 attached to the C4-CQFP package with 2-stage epoxy.

The junction temperature can be calculated from the junction-to-ambient thermal resistance, as follows:

Junction temperature: $T_j = T_a + R_{\theta ja} * P$

or

$T_j = T_a + (R_{\theta jS} + R_{sa}) * P$

Where:

T_a is the ambient temperature in the vicinity of the device

$R_{\theta ja}$ is the junction-to-ambient thermal resistance

$R_{\theta jS}$ is the junction-to-heat sink thermal resistance (includes thermal grease or thermal adhesive)

R_{sa} is the heat sink-to-ambient thermal resistance

P is the power dissipated by the device

Note: $R_{\theta js}$ includes the resistance of a typical layer of thermal compound. If a lower conductivity material is used, its thermal resistance must be included.

In this environment, it can be assumed that all the heat is dissipated to the ambient through the heat sink, so the junction-to-ambient thermal resistance is the sum of the resistances from the junction to the heat sink and from the heat sink to the ambient.

Note that verification of external thermal resistance and case temperature should be performed for each application. Thermal resistance can vary considerably due to many factors including degree of air turbulence.

Figure 16 provides a thermal management example for the IBM C4-CQFP package.

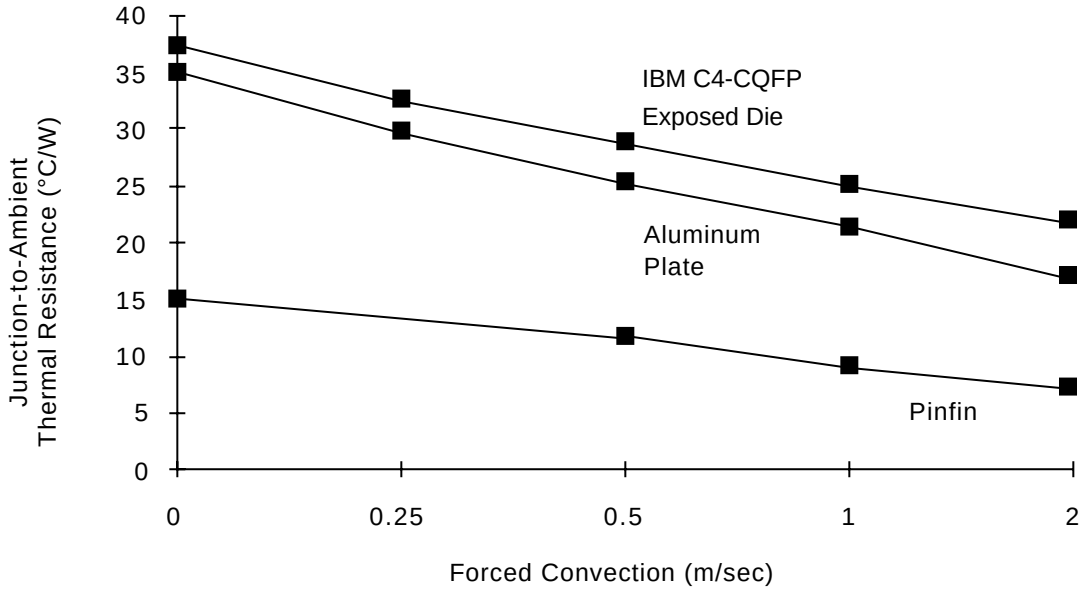


Figure 16. IBM C4-CQFP Thermal Management Example

For a power dissipation of 2.5 Watts in an ambient temperature of 40 °C at 1 m/sec with the pinfin heat sink measured above, the junction temperature of the device is as follows:

$T_j = T_a + R_{\theta ja} * P$

$T_j = 40\ °C + (9.1\ °C/Watt * 2.5\ Watts) = 63\ °C$

which is well within the reliability limits of the device.

Notes:

1. Junction-to-ambient thermal resistance is based on modeling.
2. Junction-to-heat sink thermal resistance is based on measurements and model using thermal test chip and thermal couple which is placed on the base of the heat sink.
3. θ_{ja} is not measured for 0.25 m/sec convection for the pinfin.

The vendors who supply heat sinks are Aavid Engineering, Thermalloy, and Wakefield Engineering. Any of these vendors can supply heat sinks with sufficient thermal performance. Refer to Section 1.8.6.1.2, "Thermal Management Example," for contact information.

1.8.6.3 Motorola and IBM CBGA Package

The data found in this section concerns 603e's packaged in the 255-lead 21 mm multi-layer ceramic (MLC), ceramic BGA package. Data is shown for two cases, the exposed-die case (no heat sink) and using the Thermalloy 2338-pin fin heat sink.

1.8.6.3.1 Thermal Characteristics

The internal thermal resistance for this package is negligible due to the exposed die design. A heat sink is attached directly to the silicon die surface only when external thermal enhancement is necessary.

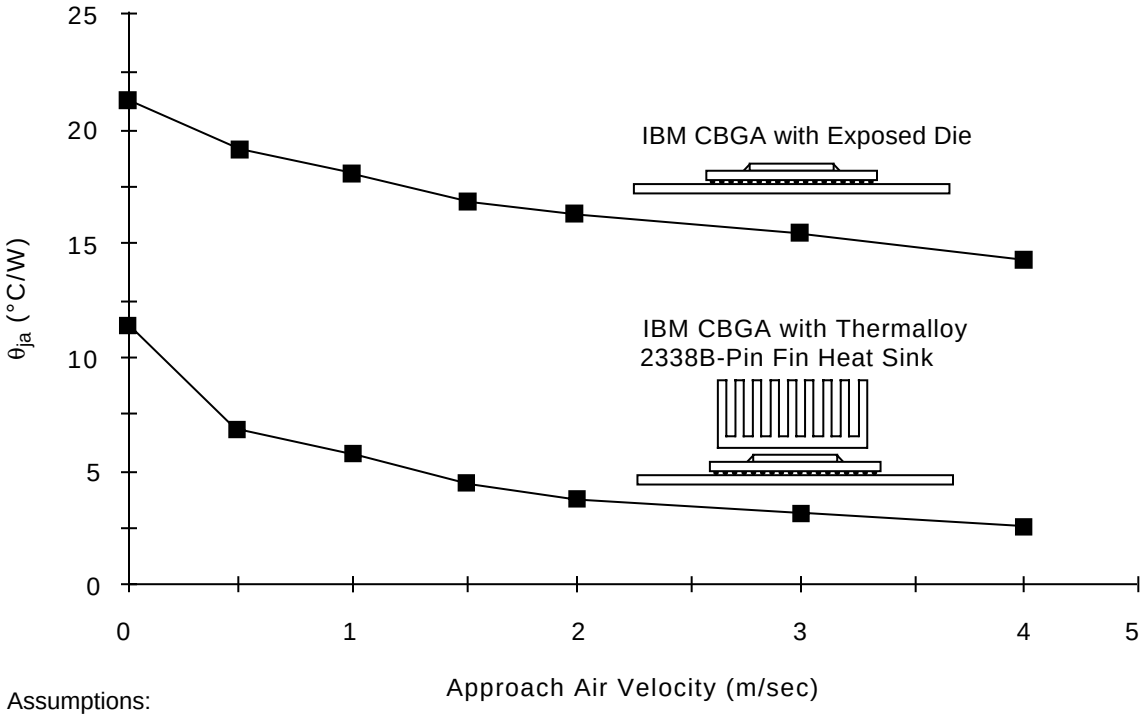
Additionally, the CBGA package offers an exceptional thermal connection to the card and power planes. Heat generated at the chip is dissipated through the package, the heat sink (when used) and the card. The parallel heat flow paths result in the lowest overall thermal resistance as well as offer significantly better power dissipation capability when a heat sink is not used.

1.8.6.3.2 Thermal Management Example

The following example is based on a typical desktop configuration using a solder-bump 21 mm CBGA package. The heat sink shown is the Thermalloy pinfin heat sink #2338 attached directly to the exposed die with a two-stage thermally conductive epoxy.

The calculations are performed exactly as shown in the previous section.

Figure 17 shows typical thermal performance data for the 21 mm CBGA package mounted to a test card.



Assumptions:

1. 2P card with 1 OZ Cu planes
2. 63 mm x 76 mm card
3. Air flow on both sides of card
4. Vertical orientation
5. 2-stage epoxy heat sink attach

Figure 17. CBGA Thermal Management Example

Temperature calculations are also performed identically to those in the previous section. For a power dissipation of 2.5 Watts in an ambient of 40° C at 1.0 m/sec, the associated overall thermal resistance and junction temperature, found in Table 13, will result.

Table 13. Thermal Resistance and Junction Temperature

Configuration	θ_{ja} (°C/W)	Tj (°C)
Exposed die (no heat sink)	18.4	86
With 2338 heat sink	5.3	53

Vendors such as Aavid Engineering Inc., Thermalloy, and Wakefield Engineering can supply heat sinks with a wide range of thermal performance. Refer to Section 1.8.6.1.2, “Thermal Management Example,” for contact information.

1.9 Ordering Information

This section provides the part numbering nomenclature for the PID7v-603e. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Motorola or IBM sales office.

1.9.1 Motorola Part Number Key

Figure 18 provides the Motorola part numbering nomenclature for the PID7v-603e. In addition to the processor frequency, the part numbering scheme also consists of a part modifier and application modifier. The part modifier indicates any enhancement(s) in the part from the original production design. The bus divider may specify special bus frequencies or application conditions. Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

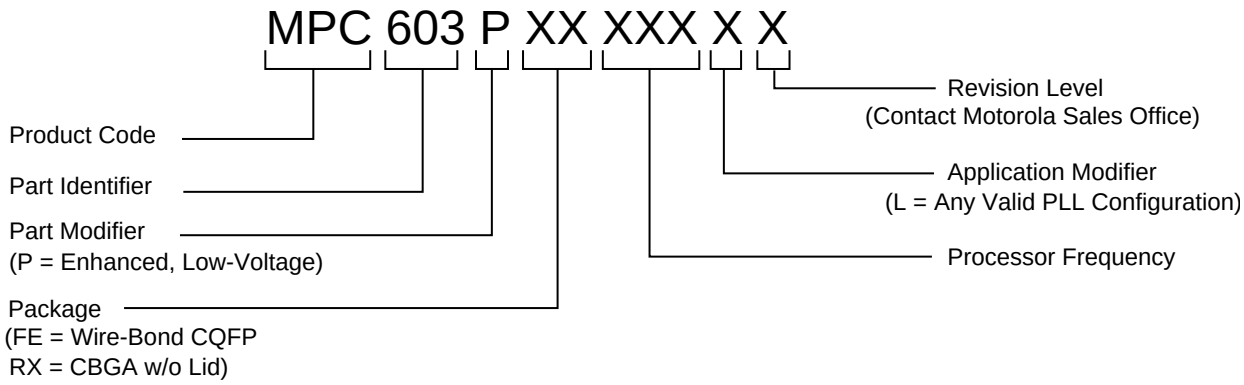


Figure 18. Motorola Part Number Key

1.9.2 IBM Part Number Key

Figure 19 provides a description of the IBM part number for the PID7v-603e.

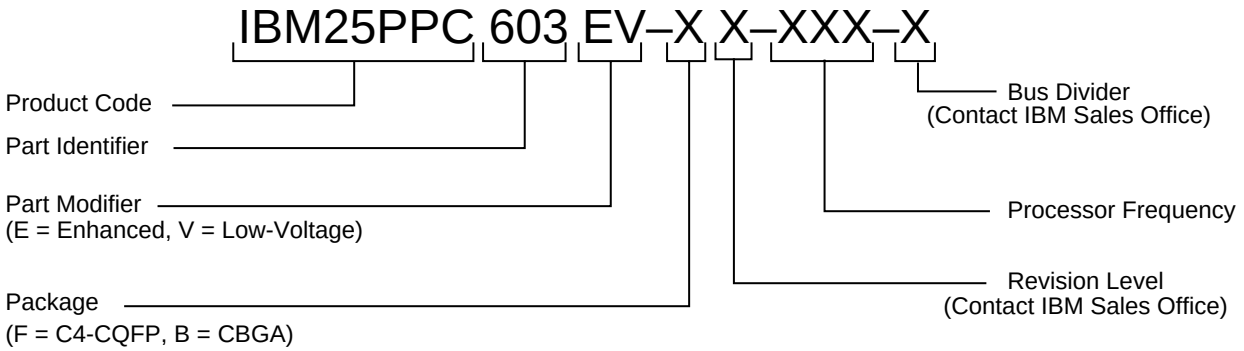


Figure 19. IBM Part Number Key

Appendix A
General Handling Recommendations for the C4-CQFP Package

The following list provides a few guidelines for package handling:

- Handle the electrostatic discharge sensitive (ESD) package with care before, during, and after processing.
- Do not apply any load to exceed 3 Kg after assembly.
- Components should not be hot-dip tinned.
- The package encapsulation is an acrylated urethane. Use adequate ventilation (local exhaust) for all elevated temperature processes.

The package parameters are as follows:

Heat sink adhesive	AIEG-7655
IBM reference drawing	99F4869
Test socket	Yamaichi QFP-PO 0.5-240P
Signal	165
Power/ground	75
Total	240

A.1 Package Environmental, Operation, Shipment, and Storage Requirements

The environmental, operation, shipment, and storage requirements are as follows:

- Make sure that the package is suitable for continuous operation under business office environments.
  - — Operating environment: 10° C to 40° C, 8% to 80% relative humidity
  - — Storage environment: 1° C to 60° C, up to 80% relative humidity
  - — Shipping environment: 40° C to 60° C, 5% to 100% relative humidity
- This component is qualified to meet JEDEC moisture Class 2.

  After expiration of shelf life, packages may be baked at 120° C (+10/–5° C) for 4 hours minimum and then be used or repackaged. Shelf life is as specified by JEDEC for moisture Class 2 components.

A.2 Card Assembly Recommendations

This section provides recommendations for card assembly process. Follow these guidelines for card assembly.

- This component is supported for aqueous, IR, convection reflow, and vapor phase card assembly processes.
- The temperature of packages should not exceed 220° C for longer than 5 minutes.
- The package entering a cleaning cycle must not be exposed to temperature greater than that occurring during solder reflow or hot air exposure.
- It is not recommended to re-attach a package that is removed after card assembly.

During the card assembly process, no solvent can be used with the C4FP, and no more than 3 Kg of force must be applied normal to the top of the package prior to, during, or after card assembly. Other details of the card assembly process follow:

Solder paste	Either water soluble (for example, Alpha 1208) or no clean
Solder stencil thickness	0.152 mm
Solder stencil aperature	Width reduced to 0.03 mm from the board pad width
Placement tool	Panasonic MPA3 or equivalent
Solder reflow	Infrared, convection, or vapor phase
Solder reflow profile	Infrared and/or convection • Average ramp-up—0.48 to 1.8° C/second • Time above 183° C—45 to 145 seconds • Minimum lead temperature—200° C • Maximum lead temperature—240° C • Maximum C4FP temperature—245° C Vapor phase • Preheat (board)—60° C to 150° C • Time above 183° C—60 to 145 seconds • Minimum lead temperature—200° C • Maximum C4FP temperature—220° C • Egress temperature—below 150° C
Clean after reflow	De-ionized (D.I.) water if water-soluble paste is used • Cleaner requirements—conveyorized, in-line • Minimum of four washing chambers — Pre-clean chamber: top and bottom sprays, minimum top-side pressure of 25 psig, water temperature of 70° C minimum, dwell time of 24 seconds minimum, water is not re-used, water flow rate of 30 liters/minute. — Wash chamber #1: top and bottom sprays, minimum top-side pressure of 48 psig, minimum bottom-side pressure of 44 psig, water temperature of 62.5° C (±2.5° C), dwell time of 48 seconds minimum, water flow rate of 350 liters/minute. — Wash chamber #2: top and bottom sprays, minimum top-side pressure of 32 psig, minimum bottom-side pressure of 28 psig, water temperature of 72.5° C (±2.5° C), dwell time of 48 seconds minimum, water flow rate of 325 liters/minute. — Final rinse chamber: top and bottom sprays, minimum top-side pressure of 25 psig, water temperature of 72.5° C minimum, dwell time of 24 seconds minimum, water flow rate of 30 liters/minute. • No cleaning required if “no clean solder paste” is used
Touch-up and repair	Water soluble (for example, Kester 450) or No Clean Flux
C4FP removal	Hot air rework
C4FP replace	Hand solder

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