Advance Information

MPC7457RXNXPNS/D
Rev. 0, 2/2003

MPC7457 Part Number Specification for the MPC74x7RXnnnnNx Series

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Motorola Part Numbers Affected:

XPC7457RX1000NB
XPC7447RX1000NB

This document describes part-number-specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC7457 RISC Microprocessor Hardware Specifications* (Order No. MPC7457EC/D).

Specifications provided in this document supersede those in the *MPC7457 RISC Microprocessor Hardware Specifications*, Rev. 0 or later, for the part numbers listed in Table A only. Specifications not addressed herein are unchanged. Because this document is frequently updated, refer to http://www.motorola.com/semiconductors or to your Motorola sales office for the latest version.

Note that headings and table numbers in this document are not consecutively numbered. They are intended to correspond to the heading or table affected in the general hardware specification.

Part numbers addressed in this document are listed in Table A.

Table A. Part Numbers Addressed by this Data Sheet

Motorola Part Number	Operating Conditions			Significant Differences from Hardware Specification
	CPU Frequency (MHz)	V_{DD}	T_j (°C)	
XPC7457RX1000NB	1000	1.1 V ± 50 mV	0 to 105	Modified core frequency and voltage to reduce power consumption, modified processor bus clock frequency and AC timing.
XPC7447RX1000NB				

Note: The X prefix in a Motorola part number designates a “Pilot Production Prototype” as defined by Motorola SOP 3-13. These are from a limited production volume of prototypes manufactured, tested, and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

1.1 Features

This section summarizes changes to the features of the MPC7457 described in the *MPC7457 RISC Microprocessor Hardware Specifications*.

- Power management
  - — 1.1-V processor core

1.3 General Parameters

- Core power supply: 1.1 V ± 50 mV DC nominal

1.5.1 DC Electrical Characteristics

Table 4 provides the recommended operating conditions for the MPC7457 part numbers described herein.

Table 4. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit
Core supply voltage	V_{DD}	1.1 V ± 50 mV	V
PLL supply voltage	AV_{DD}	1.1 V ± 50 mV	V

Note: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 7 provides the power consumption for the MPC7457 part numbers described herein.

Table 7. Power Consumption for MPC7457

	Processor (CPU) Frequency	Unit	Notes
	1000 MHz		
Full-Power Mode			
Typical	7.5	W	1, 3
Maximum	12.5	W	1, 2
Doze Mode			
Typical	—	W	4
Nap Mode			
Typical	TBD	W	1, 2
Sleep Mode			
Typical	TBD	W	1, 2
Deep Sleep Mode (PLL Disabled)			
Typical	2.0	W	1, 3

Notes:
1. These values apply for all valid processor bus and L3 bus ratios. The values do not include I/O supply power (OV_{DD} and GV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} and GV_{DD} power is system dependent, but is typically <5% of V_{DD} power. Worst case power consumption for AV_{DD} < 3 mW.
2. Maximum power is the maximum measured at nominal V_{DD} and maximum operating junction temperature (see Table 4) while running an entirely cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.
3. Typical power is an average value measured at the nominal recommended V_{DD} (see Table 4) and 65°C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz.
4. Doze mode is not a user-definable state; it is an intermediate state between Full-Power and either Nap or Sleep mode. As a result, power consumption for this mode is not tested.

Table 8 provides the clock AC timing specifications for the MPC7457 part numbers described herein.

Table 8. Clock AC Timing Specifications

At recommended operating conditions. See Table 4.

Characteristic	Symbol	Maximum Processor Core Frequency		Unit	Notes
		1000 MHz			
		Min	Max		
Processor frequency	f_{core}	500	1000	MHz	1
VCO frequency	f_{VCO}	1000	2000	MHz	1
SYSCLK frequency	f_{SYSCLK}	33	133	MHz	
SYSCLK cycle time	t_{SYSCLK}	7.5	30	ns	

Note:

1. **Caution**: The SYSCLK frequency, PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies (see Table 4 in the *MPC7457 RISC Microprocessor Hardware Specifications*). Refer to the PLL_CFG[0:4] signal description in Section 1.9.1, “PLL Configuration,” for valid PLL_CFG[0:4] settings.

1.5.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC7457 as defined in Figure 4 and Figure 5. Timing specifications for the L3 bus are provided in Section 1.5.2.3, “L3 Clock AC Specifications.”

Table 1-9. Processor Bus AC Timing Specifications [1]

At recommended operating conditions. See Table 4.

Parameter	Symbol [2]	All Speed Grades		Unit	Notes
		Min	Max		
Mode select input setup to $\overline{\text{HRESET}}$	t_{MVRH}	8	—	t_{SYSCLK}	3, 4, 5, 6
$\overline{\text{HRESET}}$ to mode select input hold	t_{MXRH}	0	—	ns	3, 6
Input setup times: A[0:35], AP[0:4] D[0:63], DP[0:7] $\overline{\text{AACK}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{CKSTP\_IN}}$, $\overline{\text{DBG}}$, DTI[0:3], $\overline{\text{GBL}}$, $\overline{\text{TBST}}$, TSIZ[0:2], TT[0:3], $\overline{\text{QACK}}$, $\overline{\text{TA}}$,TBEN, $\overline{\text{TEA}}$, $\overline{\text{TS}}$, EXT_QUAL, $\overline{\text{PMON\_IN}}$, $\overline{\text{SHD}}$[0:1]	 t_{AVKH} t_{DVKH} t_{IVKH}	 2.0 2.0 2.0	 — — —	ns	
Input hold times: A[0:35], AP[0:4] D[0:63], DP[0:7] $\overline{\text{AACK}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{CKSTP\_IN}}$, $\overline{\text{DBG}}$, DTI[0:3], $\overline{\text{GBL}}$, $\overline{\text{TBST}}$, TSIZ[0:2], TT[0:3], $\overline{\text{QACK}}$, $\overline{\text{TA}}$,TBEN, $\overline{\text{TEA}}$, $\overline{\text{TS}}$, EXT_QUAL, $\overline{\text{PMON\_IN}}$, $\overline{\text{SHD}}$[0:1]	 t_{AXKH} t_{DXKH} t_{IXKH}	 0 0 0	 — — —	ns	
Output valid times: A[0:35], AP[0:4] D[0:63], DP[0:7] $\overline{\text{AACK}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{CKSTP\_IN}}$, $\overline{\text{DBG}}$, DTI[0:3], $\overline{\text{GBL}}$, $\overline{\text{TBST}}$, TSIZ[0:2], TT[0:3], $\overline{\text{QACK}}$, $\overline{\text{TA}}$,TBEN, $\overline{\text{TEA}}$, $\overline{\text{TS}}$, EXT_QUAL, $\overline{\text{PMON\_IN}}$, $\overline{\text{SHD}}$[0:1]	 t_{KHAV} t_{KHDV} t_{KHOV}	 — — —	 2.5 2.5 2.5	ns	
Output hold times: A[0:35], AP[0:4] D[0:63], DP[0:7] $\overline{\text{AACK}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{CKSTP\_IN}}$, $\overline{\text{DBG}}$, DTI[0:3], $\overline{\text{GBL}}$, $\overline{\text{TBST}}$, TSIZ[0:2], TT[0:3], $\overline{\text{QACK}}$, $\overline{\text{TA}}$,TBEN, $\overline{\text{TEA}}$, $\overline{\text{TS}}$, EXT_QUAL, $\overline{\text{PMON\_IN}}$, $\overline{\text{SHD}}$[0:1]	 t_{KHAX} t_{KHDX} t_{KHOX}	 0.5 0.5 0.5	 — — —	ns	
SYSCLK to output enable	t_{KHOE}	0.5	—	ns	
SYSCLK to output high impedance (all except $\overline{\text{TS}}$, $\overline{\text{ARTRY}}$, $\overline{\text{SHD0}}$, $\overline{\text{SHD1}}$)	t_{KHOZ}	—	3.5	ns	
SYSCLK to $\overline{\text{TS}}$ high impedance after precharge	t_{KHTSPZ}	—	1	t_{SYSCLK}	5, 7, 10
Maximum delay to $\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$ precharge	t_{KHARP}	—	1	t_{SYSCLK}	5, 8, 9, 10

Table 1-9. Processor Bus AC Timing Specifications [1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol [2]	All Speed Grades		Unit	Notes
		Min	Max		
SYSCLK to ARTRY/SHD0/SHD1 high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	5, 8, 9, 10

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. The setup and hold time is with respect to the rising edge of HRESET (see Figure 5).
4. This specification is for configuration mode select only.
5. t_{SYSCLK} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
6. Mode select signals are: BVSEL, L3VSEL, PLL_CFG[0:4], BMODE[0:1].
7. According to the bus protocol, TS is driven only by the currently active bus master. It is asserted low then precharged high before returning to high impedance as shown in Figure 6. The nominal precharge width for TS is $0.5 \times t_{SYSCLK}$, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting TS on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
8. According to the bus protocol, ARTRY can be driven by multiple bus masters through the clock period immediately following AACK. Bus contention is not an issue because any master asserting ARTRY will be driving it low. Any master asserting it low in the first clock following AACK will then go to high impedance for one clock before precharging it high during the second cycle after the assertion of AACK. The nominal precharge width for ARTRY is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 6 before the first opportunity for another master to assert ARTRY. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
9. According to the MPX bus protocol, SHD0 and SHD1 can be driven by multiple bus masters beginning the cycle of TS. Timing is the same as ARTRY, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for SHD0 and SHD1 is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
10. Guaranteed by design and not tested.

1.5.2.3 L3 Clock AC Specifications

Table 10 provides the potential range of L3_CLK output AC timing specifications for the MPC7457 part numbers described herein.

Table 1-10. L3_CLK Output AC Timing Specifications

At recommended operating conditions. See Table 4.

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
L3 clock frequency	f_{L3_CLK}	TBD	TBD	MHz	1
L3 clock cycle time	t_{L3_CLK}	TBD	TBD	ns	
L3 clock duty cycle	t_{CHCL}/t_{L3_CLK}	50		%	2
L3 clock output-to-output skew (L1_CLK0 to L1_CLK1)	$t_{L3CSKW1}$	—	TBD	ps	3
L3 clock output-to-output skew (L1_CLK[0:1] to L1_ECHO_CLK[2:3])	$t_{L3CSKW2}$	—	TBD	ps	4
L3 clock jitter		—	TBD	ps	5

Notes:

1. The maximum L3 clock frequency will be system dependent. See Section 1.5.2.3, “L3 Clock AC Specifications,” for an explanation that this maximum frequency is not functionally tested at speed by Motorola.
2. The nominal duty cycle of the L3 output clocks is 50% measured at midpoint voltage.
3. Maximum possible skew between L3_CLK0 and L3_CLK1. This parameter is critical to the address and control signals which are common to both SRAM chips in the L3.
4. Maximum possible skew between L3_CLK0 and L3_ECHO_CLK1 or between L3_CLK1 and L3_ECHO_CLK3 for PB2 or late write SRAM. This parameter is critical to the write data signals which are separately latched onto each SRAM part by these pairs of signals.
5. Guaranteed by design and not tested. The input jitter on SYSCLK affects L3 output clocks and the L3 address/data/control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L3 timing analysis. The clock-to-clock jitter shown here is uncertainty in the internal clock period caused by supply voltage noise or thermal effects. This must be accounted for, along with clock skew, in any L3 timing analysis.

1.5.2.4.1 L3 Bus AC Specifications for DDR MSUG2 SRAMs

Table 12 provides the L3 bus interface AC timing specifications for MSUG2 for the MPC7457 part numbers described herein.

Table 12. L3 Bus Interface AC Timing Specifications for MSUG2

At recommended operating conditions. See Table 4.

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
L3_CLK rise and fall time	t_{L3CR}, t_{L3CF}	—	TBD	ns	1
Setup times: Data and parity	t_{L3DVEH}, t_{L3DVEL}	TBD	—	ns	2, 3, 4
Input hold times: Data and parity	t_{L3DXEH}, t_{L3DXEL}	TBD	—	ns	2, 4
Valid times: Data and parity	t_{L3CHDV}, t_{L3CLDV}	—	TBD	ns	5, 6, 7
Valid times: All other outputs	t_{L3CHOV}	—	TBD	ns	5, 7
Output hold times: Data and parity	t_{L3CHDX}, $t_{L3CLDX,}$	TBD	—	ns	5, 6, 7
Output hold times: All other outputs	t_{L3CHOX}	TBD	—	ns	5, 7
L3_CLK to high impedance: Data and parity	t_{L3CLDZ}	—	TBD	ns	
L3_CLK to high impedance: All other outputs	t_{L3CHOZ}	—	TBD	ns	

Notes:
1. Rise and fall times for the L3_CLK output are measured from 20% to 80% of GV_{DD}.
2. For DDR, all input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising or falling edge of the input L3_ECHO_CLK*n* (see Figure 10 in the *MPC7457 RISC Microprocessor Hardware Specifications*). Input timings are measured at the pins.
3. For DDR, the input data will typically follow the edge of L3_ECHO_CLK*n* as shown in Figure 10 in the *MPC7457 RISC Microprocessor Hardware Specifications*. For consistency with other input setup time specifications, this will be treated as negative input setup time.
4. $t_{L3\_ECHO\_CLK}/4$ is one-fourth the period of L3_ECHO_CLK*n*. This parameter indicates that the MPC7457 can latch an input signal that is valid for only a short time before and a short time after the midpoint between the rising and falling (or falling and rising) edges of L3_ECHO_CLK*n* at any frequency.
5. All output specifications are measured from the midpoint voltage of the rising (or for DDR write data, also the falling) edge of L3_CLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 8 in the *MPC7457 RISC Microprocessor Hardware Specifications*).
6. For DDR, the output data will typically lead the edge of L3_CLK*n* as shown in Figure 10 in the *MPC7457 RISC Microprocessor Hardware Specifications*. For consistency with other output valid time specifications, this will be treated as negative output valid time.
7. $t_{L3\_CLK}/4$ is one-fourth the period of L3_CLK*n*. This parameter indicates that the specified output signal is actually launched by an internal clock delayed in phase by 90°. Therefore, there is a frequency component to the output valid and output hold times such that the specified output signal will be valid for approximately one L3_CLK period starting three-fourths of a clock prior to the edge on which the SRAM will sample it and ending one-fourth of a clock period after the edge it will be sampled.
8. These configuration bits allow the AC timing of the L3 interface to be altered via software. They must be both set or both cleared; other configurations will increase $t_{L3CSKW1}$, which may cause unreliable L3 operation.

1.5.2.4.2 L3 Bus AC Specifications for PB2 and Late Write SRAMs

Table 13 provides the L3 bus AC timing specifications for PB2 and Late Write SRAMs for the MPC7457 part numbers described herein.

Table 13. L3 Bus Interface AC Timing Specifications for PB2 and Late Write SRAMs

At recommended operating conditions. See Table 4.

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
L3_CLK rise and fall time	t_{L3CR}, t_{L3CF}	—	TBD	ns	1, 5
Setup times: Data and parity	t_{L3DVEH}	TBD	—	ns	2, 5
Input hold times: Data and parity	t_{L3DXEH}	—	TBD	ns	2, 5
Valid times: Data and parity	t_{L3CHDV}	—	TBD	ns	3, 4, 5
Valid times: All other outputs	t_{L3CHOV}	—	TBD	ns	4
Output hold times: Data and parity	t_{L3CHDX}	TBD	—	ns	3, 4, 5
Output hold times: All other outputs	t_{L3CHOX}	TBD	—	ns	4, 5
L3_CLK to high impedance: Data and parity	t_{L3CHDZ}	—	TBD	ns	5
L3_CLK to high impedance: All other outputs	t_{L3CHOZ}	—	TBD	ns	5

Notes:
1. Rise and fall times for the L3_CLK output are measured from 20% to 80% of GV_{DD}.
2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L3_ECHO_CLK*n* (see Figure 10 in the *MPC7457 RISC Microprocessor Hardware Specifications*). Input timings are measured at the pins.
3. All output specifications are measured from the midpoint voltage of the rising edge of L3_CLK*n* to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 10 in the *MPC7457 RISC Microprocessor Hardware Specifications*).
4. $t_{L3\_CLK}/4$ is one-fourth the period of L3_CLK*n*. This parameter indicates that the specified output signal is actually launched by an internal clock delayed in phase by 90°. Therefore, there is a frequency component to the output valid and output hold times such that the specified output signal will be valid for approximately one L3_CLK period starting three-fourths of a clock prior to the edge on which the SRAM will sample it and ending one-fourth of a clock period after the edge it will be sampled.
5. Timing behavior and characterization are currently being evaluated.
6. These configuration bits allow the AC timing of the L3 interface to be altered via software. They must be both set or both cleared; other configurations will increase $t_{L3CSKW1}$ and $t_{L3CSKW2}$, which may cause unreliable L3 operation.

1.11 Ordering Information

1.11.1 Part Numbers Addressed by This Specification

Table 21 provides the ordering information for the MPC7457 parts described in this document.

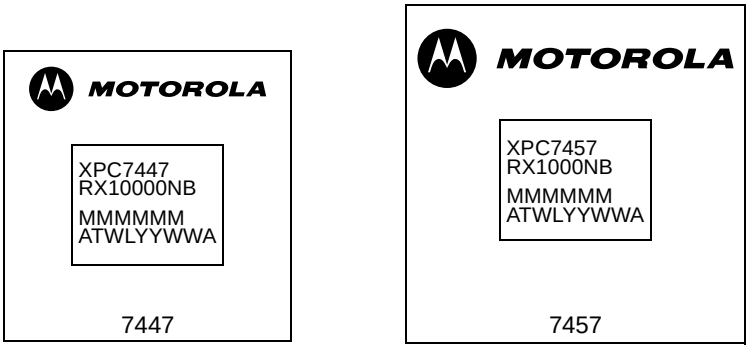
Table 21. Part Marking Nomenclature

XPC	74*x*7	RX	*nnn*	*x*	*x*
Product Code	**Part Identifier**	**Package**	**Processor Frequency [1]**	**Application Modifier**	**Revision Level**
XPC [2]	7457 7447	RX = CBGA	1000	N: 1.1 V ± 50 mV 0 to 105°C	B: 1.1; PVR = 8001 0201

Notes:
1. Processor core frequencies supported by parts addressed by this specification only. Parts addressed by other specifications may support other maximum core frequencies.
2. The X prefix in a Motorola part number designates a “Pilot Production Prototype” as defined by Motorola SOP 3-13. These are from a limited production volume of prototypes manufactured, tested, and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

1.11.3 Part Marking

Parts are marked as the example shown in Figure 29.



Notes:
MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 29. Motorola Part Marking for BGA Devices

Document Revision History

Table B provides a revision history for this part number specification.

Table B. Document Revision History

Rev. No.	Substantive Change(s)
0	Initial release.

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