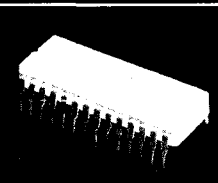
BURR-BROWN®

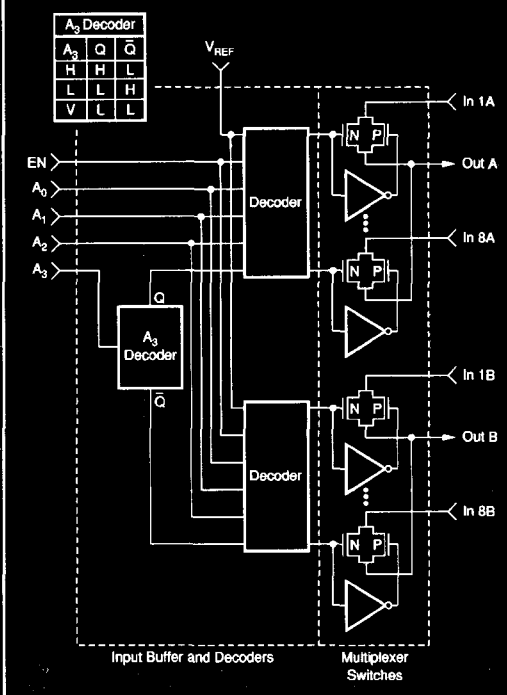


MPC800

High Speed CMOS ANALOG MULTIPLEXER

FEATURES

- HIGH SPEED
  100ns Access Time
  800ns Settling to 0.01%
  250ns Settling to 0.1%
- USER-PROGRAMMABLE
  16-Channel Single-Ended or
  8-Channel Differential
- SELECTABLE TTL OR CMOS COMPATIBILITY
- WILL NOT SHORT SIGNAL SOURCES — Break-Before-Make Switching
- SELF-CONTAINED WITH INTERNAL CHANNEL ADDRESS DECODER
- 28-PIN HERMETIC DUAL-IN-LINE PACKAGE



DESCRIPTION

The MPC800 is a high speed multiplexer that is user-programmable for 16-channel single-ended operation or 8-channel differential operation and for TTL or CMOS compatibility.

The MPC800 features a self-contained binary address decoder. It also has an enable line which allows the user to inhibit the entire multiplexer thereby facilitating channel expansion by adding additional multiplexers.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, low ON resistance, high OFF resistance, low feedthrough capacitance, and fast settling time.

Two models are available, the MPC800KG for operation from 0°C to +75°C and the MPC800SG for operation from –55°C to +125°C.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 15V, unless otherwise noted.

PARAMETER	MPC800KG, MPC800SG MIN	TYP	MAX	UNITS
ANALOG INPUTS				
Voltage Range	–15		+15	V
Maximum Overvoltage	$-V_{CC}$ –2		$+V_{CC}$ +2	V
Number of Input Channels				
Differential	8			
Single-Ended	16			
Reference Voltage Range[1]	6		10	V
ON Characteristics[2]				
ON Resistance (R_{ON}) at +25°C		620	750	Ω
Over Temperature Range		700	1000	Ω
R_{ON} Drift vs Temperature		See Typical Performance Curves		
R_{ON} Mismatch		< 10		Ω
ON Channel Leakage		0.04		nA
Over Temperature Range		0.6	100	nA
ON Channel Leakage Drift		See Typical Performance Curves		
OFF Characteristics				
OFF Isolation		90		dB
OFF Channel Input Leakage		0.01		nA
Over Temperature Range		0.38	50	nA
OFF Channel Input Leakage Drift		See Typical Performance Curves		
OFF Channel Output Leakage		0.035		nA
Over Temperature Range		0.48	100	nA
OFF Channel Output Leakage Drift		See Typical Performance Curves		
Output Leakage (All channels disabled)[3]		0.02		nA
Output Leakage with Overvoltage				
+16V Input		< 0.35		mA
–16V Input		< 0.65		mA
DIGITAL INPUTS				
Over Temperature Range				
TTL[4]				
Logic "0" (V_{AL})			0.8	V
Logic "1" (V_{AH})	2.4			V
I_{AH}		0.05	1	µA
I_{AL}		4	25	µA
TTL Input Overvoltage	–6		6	V
CMOS				
Logic "0" (V_{AL})			$0.3V_{REF}$	V
Logic "1" (V_{AH})	$0.7V_{REF}$			V
CMOS Input Overvoltage	–2		$+V_{CC}$ +2	V
Address A_3 Overvoltage	$-V_{CC}$ –2		$+V_{CC}$ +2	V
Digital Input Capacitance		5		pF
Channel Select[5]				
Single-Ended		4-bit Binary Code One of 16		
Differential		3-bit Binary Code One of 8		
Enable		Logic "0" Inhibits All Channels		
POWER REQUIREMENTS				
Over Temperature Range				
Rated Supply Voltage		±15		V
Maximum Voltage Between Supply Pins			33	V
Total Power Dissipation		525		mW
Allowable Total Power Dissipation[6]			1200	mW
Supply Drain (+25°C)				
At 1MHz Switching Speed		+35, –39		mA
At 100kHz Switching Speed		+25, –29		mA

SPECIFICATIONS (CONT)

ELECTRICAL

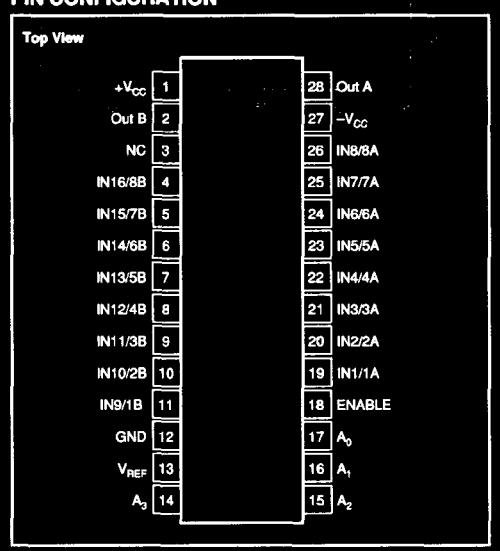
At T_A = +25°C and $\pm V_{CC}$ = 15V, unless otherwise noted.

PARAMETER	MPC800KG, MPC800SG MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS				
Gain Error		< 0.0003		%
Cross Talk(7)		See Typical Performance Curves		
T_{OPEN} (Break-before-make delay)		20		ns
Access Time at +25°C		100	150	ns
Over Temperature Range		120	200	ns
Settling Time(8)				
to 0.1% (20mV)		250		ns
to 0.01% (2mV)		800		ns
Common-Mode Rejection (Differential)				
DC		> 125		dB
60Hz		> 75		dB
OFF Channel Input Capacitance, C_S		2.5		pF
OFF Channel Output Capacitance, C_O		18		pF
OFF Input to Output Capacitance, C_{DS}		0.02		pF
TEMPERATURE				
MPC800KG				
Specification	0		+75	°C
Storage	–65		+150	°C
MPC800SG				
Specification	–55		+125	°C
Storage	–65		+150	°C

NOTES: (1) Reference voltage controls noise immunity, normally left open for TTL compatibility and connected to V_{DD} for CMOS compatibility. (2) V_{IN} = ±10V, I_{OUT} = 100µA. (3) Single-ended mode. (4) Logic levels specified for V_{REF} (pin 13) open. (5) For single-ended operation, connect output A (pin 28) to output B (pin 2) and use A_3 (pin 14) as an address line. For differential operation connect A_3 to $-V_{CC}$. (6) Derate 8mW/°C above T_A = +75°C. (7) 10Vp-p sine wave on all unused channels. See Typical Performan Curves. (8) For 20V step input to ON channel, into 1kΩ load.

PIN CONFIGURATION

Top View



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
MPC800KG	Single-Wide Cerdip	–0°C to +75°C
MPC800SG	Single-Wide Cerdip	–55°C to +125°C

PACKAGE INFORMATION(1)

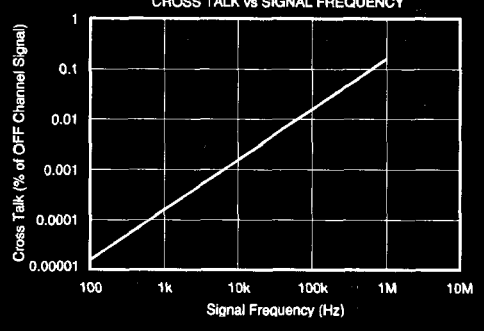
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
MPC800KG	28-Pin Single-Wide Cerdip	228
MPC800SG	28-Pin Single-Wide Cerdip	228

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

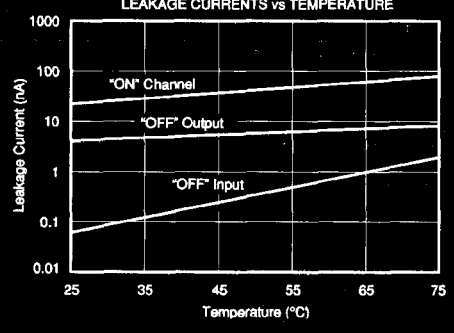
TYPICAL PERFORMANCE CURVES

At T_A = +25°C and $\pm V_{CC}$ = 15V, unless otherwise noted.

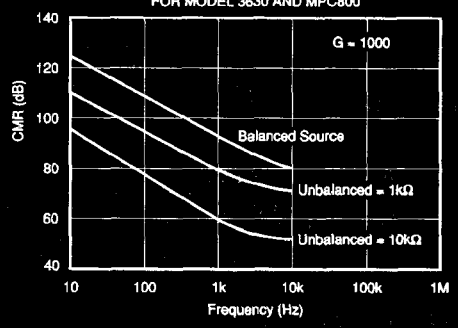
CROSS TALK vs SIGNAL FREQUENCY



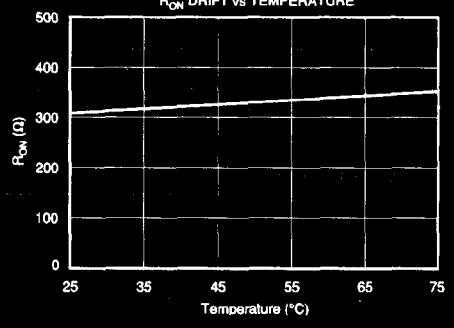
LEAKAGE CURRENTS vs TEMPERATURE



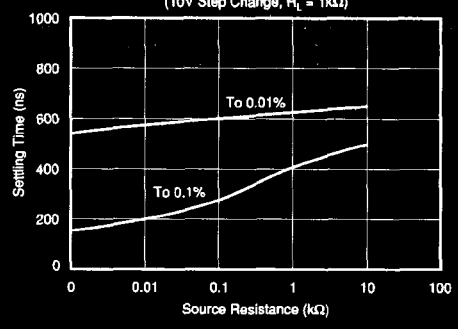
COMBINED CMR vs FREQUENCY
FOR MODEL 3630 AND MPC800



R_{ON} DRIFT vs TEMPERATURE



SETTLING TIME vs SOURCE RESISTANCE
(10V Step Change, R_L = 1kΩ)



DISCUSSION OF PERFORMANCE

STATIC TRANSFER ACCURACY

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current, and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the ON resistance loading errors. To minimize these errors:

- *Keep loading impedance as high as possible.* This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedance of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- *Use sources with impedances as low as possible.* A 1000Ω source resistance will present less than 0.002% loading error and $10k\Omega$ source resistance will increase source loading error 0.02% with a $10^8\Omega$ load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1):

Source and Multiplexer Resistive Loading Error

$$\epsilon(R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where, $R_S = R_{SOURCE}$
R_L = Load resistance
R_{OS} = Multiplexer ON resistance

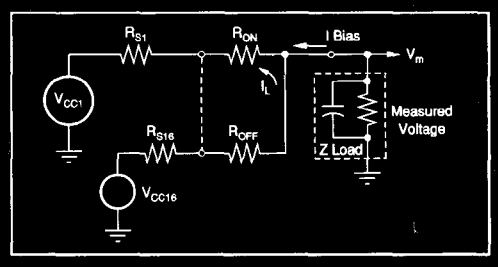


FIGURE 1. MPC800 Static Accuracy Equavalent Circuit (Single-ended Operation).

Input Offset Voltage

Bias and leakage currents generate an input offset voltage as a result of the I_R drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA, a leakage current of 1nA, and an ON resistance of 700Ω will generate an offset voltage of $19\mu V$ if a 1000Ω source is used, and $118\mu V$ if a $10k\Omega$ source is used. In general, for the MPC800 the offset voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_{SOURCE})$$

where:

I_B = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{SOURCE} = Source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low level signals with full scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications.

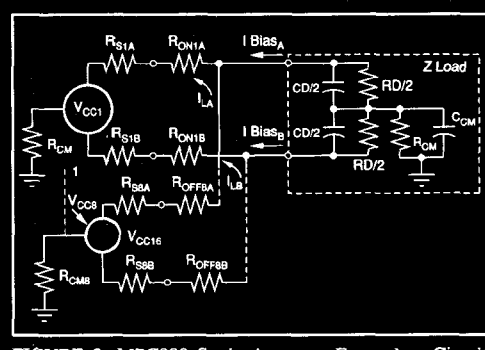


FIGURE 2. MPC800 Static Accuracy Equavalent Circuit (Differential Operation).

Load (Output Device) Characteristics

- *Use devices with very low bias current.* Generally FET input amplifiers should be used for low level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine input offset.

- *The system DC common-mode rejection* (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- *Load impedances, differential and common-mode* should be $10^{10}\Omega$ or higher.

Source Characteristics

- *The source impedance unbalance* will produce offset, common-mode, and channel-to-channel gain scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- *Keep source impedances as low as possible* to minimize resistive loading errors.
- *Minimize ground loops.* If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC800 is used for multiplexing high level signals of 1V to 10V full scale ranges, the foregoing precautions should be taken, but the parameters are not as critical as for low level signal applications.

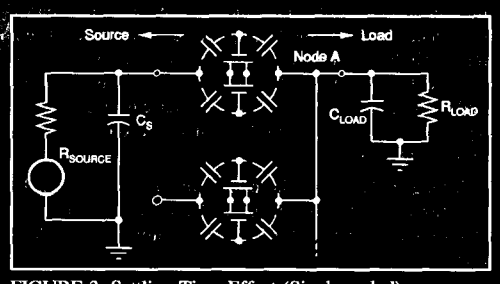


FIGURE 3. Settling Time Effect (Single-ended).

SETTLING TIME

Settling time is the time required for the multiplexer to reach and maintain an output within a specified error band of its final value in response to a step input. The settling time of the MPC800 is primarily due to the channel capacitance and a combination of resistances which include the source and load resistances.

If the parallel combination of the source and load resistance times the total channel capacitance is kept small, then the settling time is primarily affected by internal RCs. For the MPC800, the internal capacitance is approximately 20pF differential or 40pF single-ended. With external capacitance neglected, the time constant of source resistance in parallel with load resistance and the internal capacitance should be kept less than 40ns. This means the source resistance should be kept to less than $2k\Omega$ (assume high load resistance) to maintain fast settling times.

ACCESS TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the 7 differential or 15 signal-ended OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance, and junction capacitances in series with the R_{ON} and R_{SOURCE} impedance of the ON channel. Crosstalk is measured with a

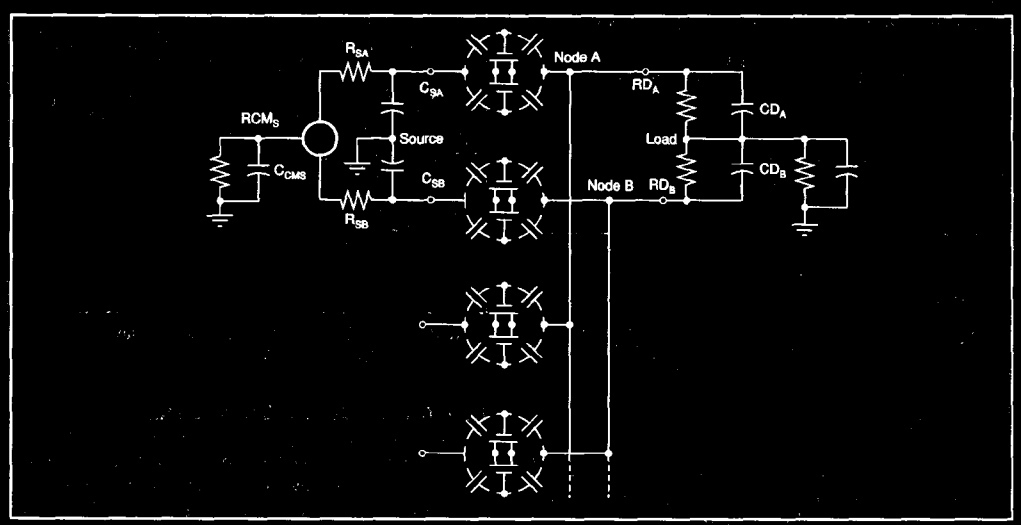


FIGURE 4. Settling and Common-Mode Effects (Differential).

20Vp-p, 1000Hz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

COMMON-MODE REJECTION (Differential Mode Only)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. Protection is provided for common-mode signals of ±2V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC800 and Burr-Brown's model 3630 instrumentation amplifier is 120dB at DC to 10Hz with a 6dB/octave rolloff to 80dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model 3630 instrumentation amplifier connected for a signal of 1000 and with source unbalance of 10kΩ. 1kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch.
- Load impedance mismatch.
- Multiplexer impedance and leakage current mismatch.
- Load and source common-mode impedance.

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

INSTALLATION AND OPERATING INSTRUCTIONS

The ENABLE input, pin 18, is included for expansion of the number of channels on a single-node as illustrated in Figure 5. With the ENABLE line at a logic 1, the channel is selected by the Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to logic 1.

For the best settling time, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pullup resistors are recommended.

To preserve common-mode rejection of the MPC800 use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

LOGIC LEVELS

The logic level is user-programmable as either TTL-compatible by leaving the V_{REF} (pin 13) open or CMOS-compatible by connecting the V_{REF} to V_{DD} (CMOS supply voltage).

16-CHANNEL SINGLE-ENDED OPERATION

To use the MPC800 as a 16-channel single-ended multiplexer, output A (pin 28) is connected to output B (pin 2) to form a single output, then all four address lines (A_0, A_1, A_2 and A_3) are used to address the correct channel.

The MPC800 can also be used as a dual 8-channel single-ended multiplexer by not connecting output A and B, but then only one channel in one of the multiplexers can be addressed at a time.

8-CHANNEL DIFFERENTIAL OPERATION

To use the MPC800 as an 8-channel differential multiplexer, connect address line A_3 to $-V_{CC}$, then use the remaining three address lines (A_0, A_1, and A_2) to address the correct channel. The differential inputs are the pairs of A_1 and B_1, A_2 and B_2, etc.

TRUTH TABLES

MPC800 used as 16-channel single-ended multiplexer or 8-channel dual multiplexer.

USE A_3 AS DIGITAL ADDRESS INPUT					"ON" CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	None	None
H	L	L	L	L	1A	None
H	L	L	L	H	2A	None
H	L	L	H	L	3A	None
H	L	L	H	H	4A	None
H	L	H	L	L	5A	None
H	L	H	L	H	6A	None
H	L	H	H	L	7A	None
H	L	H	H	H	8A	None
H	H	L	L	L	None	1B
H	H	L	L	H	None	2B
H	H	L	H	L	None	3B
H	H	L	H	H	None	4B
H	H	H	L	L	None	5B
H	H	H	L	H	None	6B
H	H	H	H	L	None	7B
H	H	H	H	H	None	8B

For 16-channel single-ended function, tie "out A" to "out B", for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

MPC800 used as 8-channel differential multiplexer.

A_3 CONNECT TO $-V_{CC}$				"ON" CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	None	None
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

CHANNEL EXPANSION

Single-Tier Expansion

Up to four MPC800s can be connected to a single node to form a 64-channel single-ended multiplexer or up to eight MPC800s can be connected to two nodes to form a 64-channel differential multiplexer. Programming is accomplished with a 6-bit address and a 1-of-4 decoder for 64-channel single-ended expansion (see Figure 5), and an 8-bit address and a 1-of-8 decoder for 64-channel differential expansion. The decoder drives the enable inputs of the MPC800, turning on only one multiplexer at a time.

Two-Tier Expansion

Up to seventeen MPC800s can be connected in a two-tier structure to form a 256-channel single-ended multiplexer (see Figure 6) or up to nine MPC800s can be connected in a two-tier structure to form a 64-channel differential multiplexer. Programming is accomplished with an 8-bit address.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced offset), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one-channel group is failed (8 or 16) in the multitiered configuration.

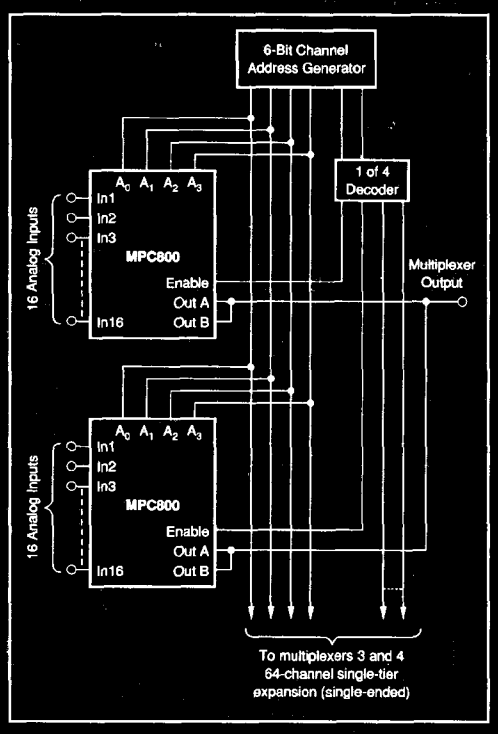


FIGURE 5. 32- to 64-Channel, Single-tier Expansion.

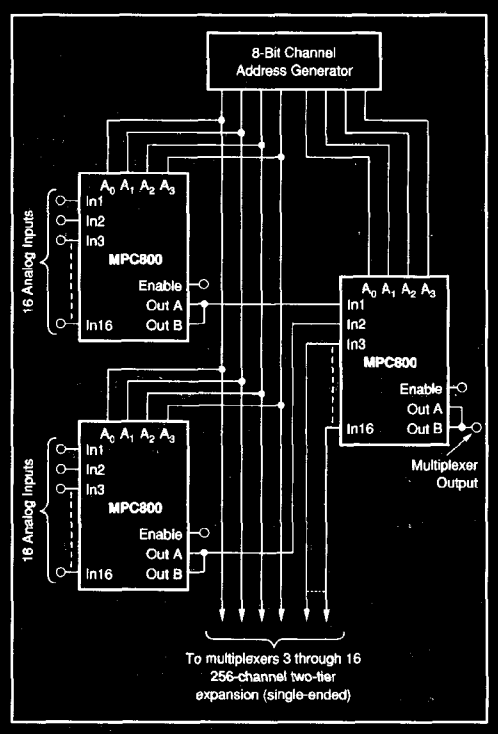


FIGURE 6. Channel Expansion up to 256 Channels Using 16 X 16 Two-tiered Expansion.