# Low Voltage PLL Clock Driver

**MPC9351**

**LOW VOLTAGE 2.5V AND 3.3V PLL CLOCK GENERATOR**

The MPC9351 is a 2.5V and 3.3V compatible, PLL based clock generator targeted for high performance clock distribution systems. With output frequencies of up to 200 MHz and a maximum output skew of 150 ps the MPC9351 is an ideal solution for the most demanding clock tree designs. The device offers 9 low skew clock outputs, each is configurable to support the clocking needs of the various high-performance microprocessors including the PowerQuicc II integrated communication microprocessor. The extended temperature range of the MPC9351 supports telecommunication and networking requirements.The devices employs a fully differential PLL design to minimize cycle-to-cycle and long-term jitter.

**FA SUFFIX**
LQFP PACKAGE
CASE 873A–02

**Features**

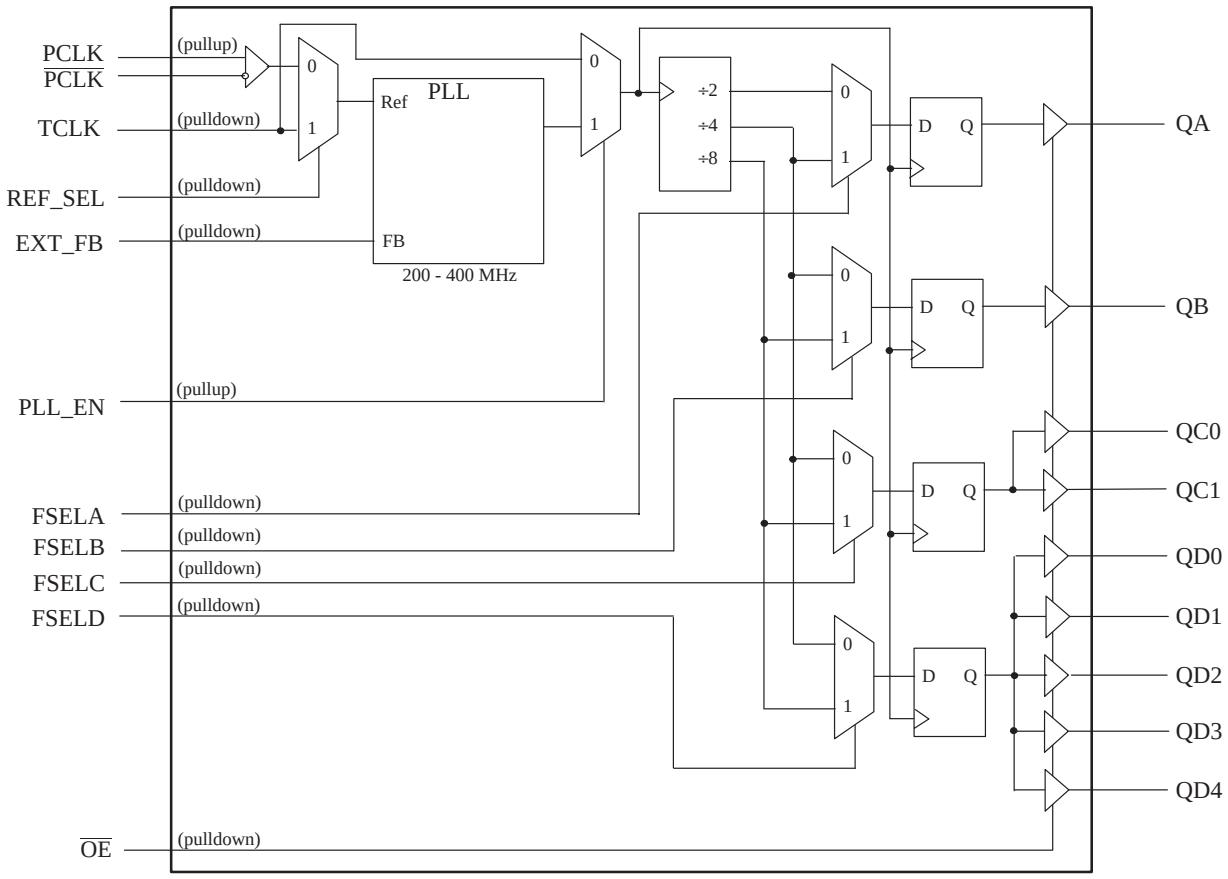
- 9 outputs LVCMOS PLL clock generator
- 25 - 200 MHz output frequency range
- Fully integrated PLL
- 2.5V and 3.3V compatible
- Compatible to various microprocessors such as PowerQuicc II
- Supports networking, telecommunications and computer applications
- Configurable outputs: divide-by-2, 4 and 8 of VCO frequency
- LVPECL and LVCMOS compatible inputs
- External feedback enables zero-delay configurations
- Output enable/disable and static test mode (PLL enable/disable)
- Low skew characteristics: maximum 150 ps output-to-output
- Cycle-to-cycle jitter max. 22 ps RMS
- 32 lead LQFP package
- Ambient Temperature Range –40°C to +85°C

**Functional Description**

The MPC9351 utilizes PLL technology to frequency and phase lock its outputs onto an input reference clock. Normal operation of the MPC9351 requires a connection of one of the device outputs to the EXT_FB input to close the PLL feedback path. The reference clock frequency and the output divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. With available output dividers of divide-by-2, divide-by-4 and divide-by-8 the internal VCO of the MPC9351 is running at either 2x, 4x or 8x of the reference clock frequency. The frequency of the QA, QB, QC and QD outputs is either the one half, one fourth or one eighth of the selected VCO frequency and can be configured for each output bank using the FSELA, FSELB, FSELC and FSELD pins, respectively. The available output to input frequency ratios are 4:1, 2:1, 1:1, 1:2 and 1:4. The REF_SEL pin selects the differential LVPECL (PCLK and PCLK) or the LVCMOS compatible reference input (TCLK). The MPC9351 also provides a static test mode when the PLL enable pin (PLL_EN) is pulled to logic low state. In test mode, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The test mode is intended for system diagnostics, test and debug purpose. This test mode is fully static and the minimum clock frequency specification does not apply. The outputs can be disabled by deasserting the OE pin (logic high state). In PLL mode, deasserting OE causes the PLL to loose lock due to no feedback signal presence at EXT_FB. Asserting OE will enable the outputs and close the phase locked loop, also enabling the PLL to recover to normal operation. The MPC9351 is fully 2.5V and 3.3V compatible and requires no external loop filter components. All inputs except PCLK and PCLK accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9351 outputs can drive one or two traces giving the devices an effective fanout of 1:18. The device is packaged in a 7x7 $mm^2$ 32-lead LQFP package.

**Application Information**

The fully integrated PLL of the MPC9351 allows the low skew outputs to lock onto a clock input and distribute it with essentially zero propagation delay to multiple components on the board. In zero-delay buffer mode, the PLL minimizes phase offset between the outputs and the reference signal.




The MPC9351 requires an external RC filter for the analog power supply pin VCCA. Please see application section for details.

**Figure 1. MPC9351 Logic Diagram**

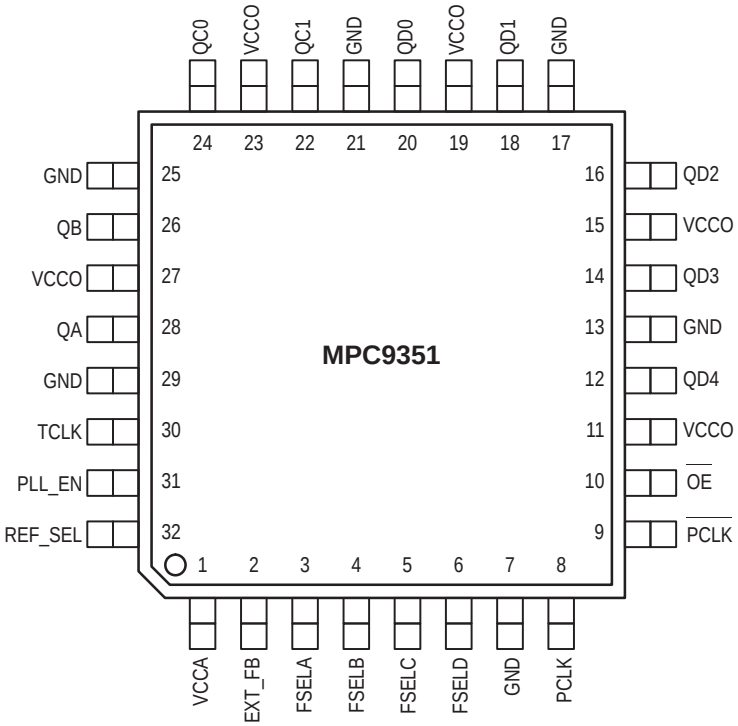



**Figure 2. Pinout: 32–Lead Package Pinout** (Top View)

## PIN CONFIGURATION

| Pin | I/O | Type | Function |
|---|---|---|---|
| PCLK, PCLK | Input | LVPECL | Differential clock reference<br>Low voltage positive ECL input |
| TCLK | Input | LVCMOS | Single ended reference clock signal or test clock |
| EXT_FB | Input | LVCMOS | Feedback signal input, connect to a QA, QB, QC, QD output |
| REF_SEL | Input | LVCMOS | Selects input reference clock |
| FSELA | Input | LVCMOS | Output A divider selection |
| FSELB | Input | LVCMOS | Output B divider selection |
| FSELC | Input | LVCMOS | Outputs C divider selection |
| FSELD | Input | LVCMOS | Outputs D divider selection |
| $\overline{OE}$ | Input | LVCMOS | Output enable/disable |
| QA | Output | LVCMOS | Bank A clock output |
| QB | Output | LVCMOS | Bank B clock output |
| QC0, QC1 | Output | LVCMOS | Bank C clock outputs |
| QD0 - QD4 | Output | LVCMOS | Bank D clock outputs |
| VCCA | Supply | VCC | Positive power supply for the PLL |
| VCC | Supply | VCC | Positive power supply for I/O and core |
| GND | Supply | Ground | Negative power supply |

## FUNCTION TABLE

| Control | Default | 0 | 1 |
|---|---|---|---|
| REF_SEL | 0 | Selects PCLK as reference clock | Selects TCLK as reference clock |
| PLL_EN | 1 | Test mode with PLL disabled. The input clock is directly routed to the output dividers | PLL enabled. The VCO output is routed to the output dividers |
| $\overline{OE}$ | 0 | Outputs enabled | Outputs disabled, PLL loop is open<br>VCO is forced to its minimum frequency |
| FSELA | 0 | QA = VCO ÷ 2 | QA = VCO ÷ 4 |
| FSELB | 0 | QB = VCO ÷ 4 | QB = VCO ÷ 8 |
| FSELC | 0 | QC = VCO ÷ 4 | QC = VCO ÷ 8 |
| FSELD | 0 | QD = VCO ÷ 4 | QD = VCO ÷ 8 |

## ABSOLUTE MAXIMUM RATINGS[a]

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 4.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage Temperature | -55 | 150 | °C | |

a. Absolute maximum continuos ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

## GENERAL SPECIFICATIONS

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output Termination Voltage | | $V_{CC}$ ÷ 2 | | V | |
| MM | ESD (Machine Model) | 200 | | | V | |
| HBM | ESD (Human Body Model) | 2000 | | | V | |
| LU | Latch–Up | 200 | | | mA | |
| $C_{PD}$ | Power Dissipation Capacitance | | 10 | | pF | Per output |
| $C_{IN}$ | | | 4.0 | | pF | Inputs |

**DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | V | LVCMOS |
| $V_{PP}$ | Peak-to-Peak Input Voltage PCLK, $\overline{PCLK}$ | 250 | | | mV | LVPECL |
| $V_{CMR}$[a] | Common Mode Range PCLK, $\overline{PCLK}$ | 1.0 | | $V_{CC}$-0.6 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$=-24 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24 mA<br>$I_{OL}$= 12 mA |
| $Z_{OUT}$ | Output Impedance | | 14 - 17 | | Ω | |
| $I_{IN}$ | Input Leakage Current | | | ±150 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CCA}$ | Maximum PLL Supply Current | | 3.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification.

b. The MPC9351 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

**AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency ÷ 2 feedback<br>÷ 4 feedback<br>÷ 8 feedback<br>Static test mode | 100<br>50<br>25<br>0 | | 200<br>100<br>50<br>300 | MHz<br>MHz<br>MHz<br>MHz | PLL_EN = 1<br>PLL_EN = 1<br>PLL_EN = 1<br>PLL_EN = 0 |
| $f_{VCO}$ | VCO Frequency | 200 | | 400 | MHz | |
| $f_{MAX}$ | Maximum Output Frequency ÷ 2 output<br>÷ 4 output<br>÷ 8 output | 100<br>50<br>25 | | 200<br>100<br>50 | MHz<br>MHz<br>MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | | 75 | % | |
| $V_{PP}$ | Peak-to-Peak Input Voltage PCLK, $\overline{PCLK}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[b] | Common Mode Range PCLK, $\overline{PCLK}$ | 1.2 | | $V_{CC}$-0.9 | V | LVPECL |
| tr, tf | TCLK Input Rise/Fall Time | | | 1.0 | ns | 0.8 to 2.0V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset)<br>TCLK to EXT_FB<br>PCLK to EXT_FB | <br>–50<br>+25 | | <br>+150<br>+325 | <br>ps<br>ps | <br>PLL locked<br>PLL locked |
| $t_{sk(o)}$ | Output-to-Output Skew | | | 150 | ps | |
| DC | Output Duty Cycle 100 – 200 MHz<br>50 – 100 MHz<br>25 – 50 MHz | 45<br>47.5<br>48.75 | 50<br>50<br>50 | 55<br>52.5<br>51.75 | %<br>%<br>% | |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | 10 | ns | |
| $t_{PZL, ZH}$ | Output Enable Time | | | 10 | ns | |
| BW | PLL closed loop bandwidth ÷ 2 feedback<br>÷ 4 feedback<br>÷ 8 feedback | | 9.0 – 20.0<br>3.0 – 9.5<br>1.2 – 2.1 | | MHz<br>MHz<br>MHz | –3 db point of<br>PLL transfer<br>characteristic |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter ÷ 4 feedback<br>Single Output Frequency Configuration | | 10 | 22 | ps | RMS value |
| $t_{JIT(PER)}$ | Period Jitter ÷ 4 feedback<br>Single Output Frequency Configuration | | 8.0 | 15 | ps | RMS value |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | | 4.0 – 17 | | ps | RMS value |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 1.0 | ms | |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$

b. $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$.

**DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | | | 0.7 | V | LVCMOS |
| $V_{PP}$ | Peak-to-Peak Input Voltage PCLK, $\overline{PCLK}$ | 250 | | | mV | LVPECL |
| $V_{CMR}$[a] | Common Mode Range PCLK, $\overline{PCLK}$ | 1.0 | | $V_{CC}$-0.6 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$=-15 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$= 15 mA |
| $Z_{OUT}$ | Output Impedance | | 17 - 20 | | Ω | |
| $I_{IN}$ | Input Leakage Current | | | ±150 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | |
| $C_{PD}$ | Power Dissipation Capacitance | | 10 | | pF | Per Output |
| $I_{CCA}$ | Maximum PLL Supply Current | | 3.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification.

b. The MPC9351 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

**AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency ÷ 2 feedback<br>÷ 4 feedback<br>÷ 8 feedback | 100<br>50<br>25 | | 200<br>100<br>50 | MHz<br>MHz<br>MHz | |
| $f_{VCO}$ | VCO Frequency | 200 | | 400 | MHz | |
| $f_{MAX}$ | Maximum Output Frequency ÷ 2 output<br>÷ 4 output<br>÷ 8 output | 100<br>50<br>25 | | 200<br>100<br>50 | MHz<br>MHz<br>MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | | 75 | % | |
| $V_{PP}$ | Peak-to-Peak Input Voltage PCLK, $\overline{PCLK}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[b] | Common Mode Range PCLK, $\overline{PCLK}$ | 1.2 | | $V_{CC}$-0.6 | V | LVPECL |
| tr, tf | TCLK Input Rise/Fall Time | | | 1.0 | ns | 0.7 to 1.7V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset)<br>TCLK to EXT_FB<br>PCLK to EXT_FB | <br>–100<br>0 | | <br>+100<br>+300 | <br>ps<br>ps | <br>PLL locked<br>PLL locked |
| $t_{sk(o)}$ | Output-to-Output Skew | | | 150 | ps | |
| DC | Output Duty Cycle 100 – 200 MHz<br>50 – 100 MHz<br>25 – 50 MHz | 45<br>47.5<br>48.75 | 50<br>50<br>50 | 55<br>52.5<br>51.75 | %<br>%<br>% | |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | 12 | ns | |
| $t_{PZL, ZH}$ | Output Enable Time | | | 12 | ns | |
| BW | PLL closed loop bandwidth ÷ 2 feedback<br>÷ 4 feedback<br>÷ 8 feedback | | 4.0 – 15.0<br>2.0 – 7.0<br>0.7 – 2.0 | | MHz<br>MHz<br>MHz | –3dB point of PLL transfer characteristic |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter ÷ 4 feedback<br>Single Output Frequency Configuration | | 10 | 22 | ps | RMS value |
| $t_{JIT(PER)}$ | Period Jitter ÷ 4 feedback<br>Single Output Frequency Configuration | | 8.0 | 15 | ps | RMS value |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | | 6.0 – 25 | | ps | RMS value |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 1.0 | ms | |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$

b. $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$.

## APPLICATIONS INFORMATION

### Programming the MPC9351

The MPC9351 clock driver outputs can be configured into several divider modes, in addition the external feedback of the device allows for flexibility in establishing various input to output frequency relationships. The output divider of the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensure that the output duty cycle is always 50%. “Output Frequency Relationship for an Example Configuration” illustrates the various output configurations, the table describes the outputs using the input clock frequency CLK as a reference.

The output division settings establish the output relationship, in addition, it must be ensured that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL supports output frequencies from 25 MHz to 200 MHz while the VCO frequency range is specified from 200 MHz to 400 MHz and should not be exceeded for stable operation.

**Output Frequency Relationship[a] for an Example Configuration**

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| FSELA | FSELB | FSELC | FSELD | QA | QB | QC | QD |
| 0 | 0 | 0 | 0 | 2 * CLK | CLK | CLK | CLK |
| 0 | 0 | 0 | 1 | 2 * CLK | CLK | CLK | CLK ÷ 2 |
| 0 | 0 | 1 | 0 | 4 * CLK | 2 * CLK | CLK | 2* CLK |
| 0 | 0 | 1 | 1 | 4 * CLK | 2 * CLK | CLK | CLK |
| 0 | 1 | 0 | 0 | 2 * CLK | CLK ÷ 2 | CLK | CLK |
| 0 | 1 | 0 | 1 | 2 * CLK | CLK ÷ 2 | CLK | CLK ÷ 2 |
| 0 | 1 | 1 | 0 | 4 * CLK | CLK | CLK | 2 * CLK |
| 0 | 1 | 1 | 1 | 4 * CLK | CLK | CLK | CLK |
| 1 | 0 | 0 | 0 | CLK | CLK | CLK | CLK |
| 1 | 0 | 0 | 1 | CLK | CLK | CLK | CLK ÷ 2 |
| 1 | 0 | 1 | 0 | 2 * CLK | 2 * CLK | CLK | 2 * CLK |
| 1 | 0 | 1 | 1 | 2 * CLK | 2 * CLK | CLK | CLK |
| 1 | 1 | 0 | 0 | CLK | CLK ÷ 2 | CLK | CLK |
| 1 | 1 | 0 | 1 | CLK | CLK ÷ 2 | CLK | CLK ÷ 2 |
| 1 | 1 | 1 | 0 | 2 * CLK | CLK | CLK | 2 * CLK |
| 1 | 1 | 1 | 1 | 2 * CLK | CLK | CLK | CLK |

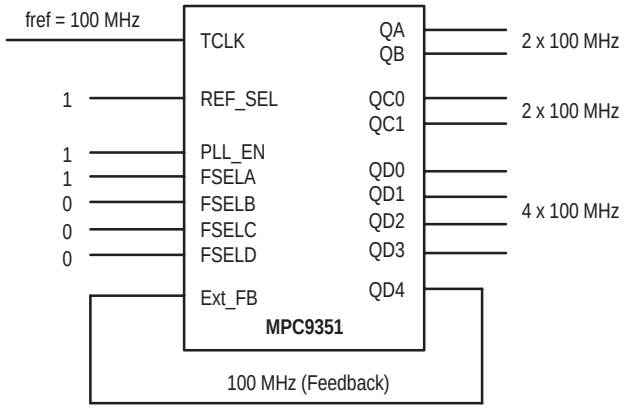
a. Output frequency relationship with respect to input reference frequency CLK. QC1 is connected to EXT_FB. More frequency ratios are available by the connection of QA to the feedback input (EXT_FB).

### Using the MPC9351 in zero–delay applications

Nested clock trees are typical applications for the MPC9351. For these applications the MPC9351 offers a differential LVPECL clock input pair as a PLL reference. This allows for the use of differential LVPECL primary clock distribution devices such as the Motorola MC100EP111 or MC10EP222, taking advantage of its superior low-skew performance. Clock trees using LVPECL for clock distribution and the MPC9351 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers.

The external feedback option of the MPC9351 PLL allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge and virtually eliminates the propagation delay through the device.

The remaining insertion delay (skew error) of the MPC9351 in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset (SPO or $t_{(\varnothing)}$), I/O jitter ($t_{JIT(\varnothing)}$, phase or long-term jitter), feedback path delay and the output-to-output skew ($t_{SK(O)}$ relative to the feedback output.




**MPC9351 zero–delay configuration (feedback of QD4)**

**Calculation of part-to-part skew**

The MPC9351 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs (TCLK or PCLK) of two or more MPC9351 are connected together, the maximum overall timing uncertainty from the common TCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

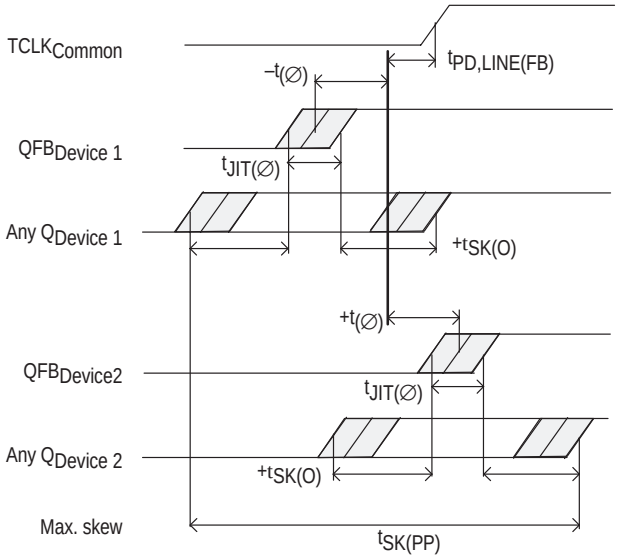



**Figure 3. MPC9351 max. device-to-device skew**

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

**Table 8: Confidence Facter CF**

| CF | Probability of clock edge within the distribution |
|---|---|
| ± 1σ | 0.68268948 |
| ± 2σ | 0.95449988 |
| ± 3σ | 0.99730007 |
| ± 4σ | 0.99993663 |
| ± 5σ | 0.99999943 |
| ± 6σ | 0.99999999 |

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -251 ps to 351 ps relative to TCLK ($V_{CC}$=3.3V and $f_{VCO}$ = 400 MHz):

$$t_{SK(PP)} = [–50ps...150ps] + [–150ps...150ps] + [(17ps \cdot –3)...(17ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [–251ps...351ps] + t_{PD,\ LINE(FB)}$$

Above equation uses the maximum I/O jitter number shown in the AC characteristic table for $V_{CC}$=3.3V (17 ps RMS). I/O jitter is frequency dependant with a maximum at the lowest VCO frequency (200 MHz for the MPC9351). Applications using a higher VCO frequency exhibit less I/O jitter than the AC characteristic limit. The I/O jitter characteristics in Figure 4. and Figure 5. can be used to derive a smaller I/O jitter number at the specific VCO frequency, resulting in tighter timing limits in zero-delay mode and for part-to-part skew $t_{SK(PP)}$.

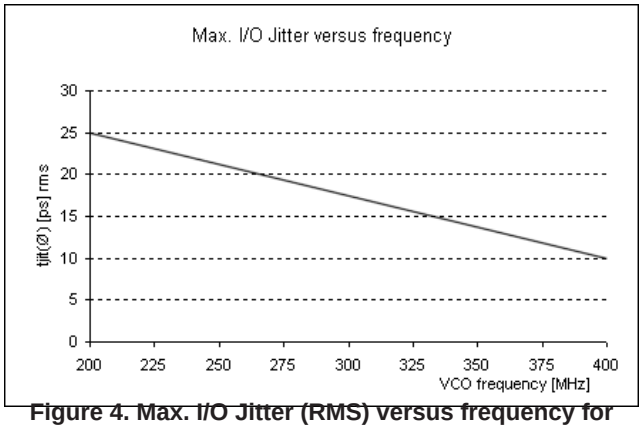



**Figure 4. Max. I/O Jitter (RMS) versus frequency for $V_{CC}$=2.5V**

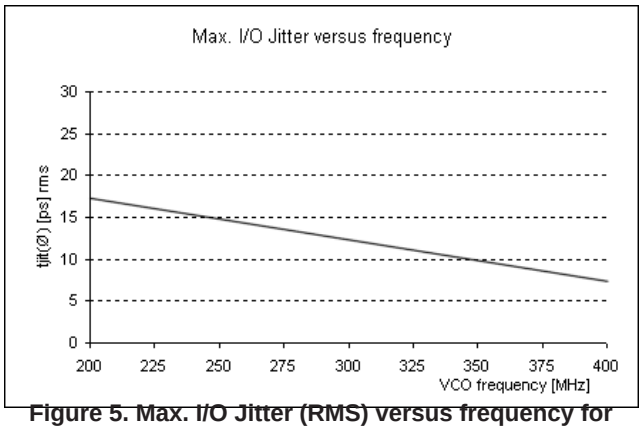



**Figure 5. Max. I/O Jitter (RMS) versus frequency for $V_{CC}$=3.3V**

**Power Supply Filtering**

The MPC9351 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Noise on the $V_{CCA}$ (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9351 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop ($V_{CCA}$) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the $V_{CCA}$ pin for the MPC9351. Figure 6. illustrates a typical power supply filter scheme. The MPC9351 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to

target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CCA}$ current (the current sourced through the $V_{CCA}$ pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}$=3.3V or $V_{CC}$=2.5V) must be maintained on the $V_{CCA}$ pin. The resistor $R_F$ shown in Figure 6. "$V_{CCA}$ Power Supply Filter" must have a resistance of 270Ω ($V_{CC}$=3.3V) or 9-10Ω ($V_{CC}$=2.5V) to meet the voltage drop criteria.

$R_F$ = 270Ω for $V_{CC}$ = 3.3V
$R_F$ = 9–10Ω for $V_{CC}$ = 2.5V
$C_F$ = 1 µF for $V_{CC}$ = 3.3V
$C_F$ = 22 µF for $V_{CC}$ = 2.5V

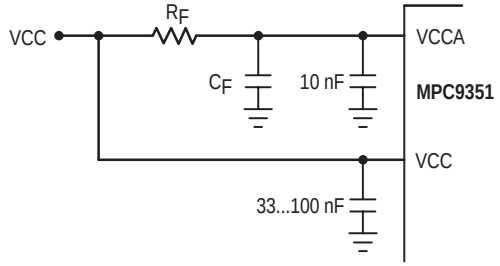



**Figure 6. $V_{CCA}$ Power Supply Filter**

The minimum values for $R_F$ and the and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 6. "$V_{CCA}$ Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9351 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

### Driving Transmission Lines

The MPC9351 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9351 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 7. "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9351 clock driver is effectively doubled due to its capability to drive multiple lines.

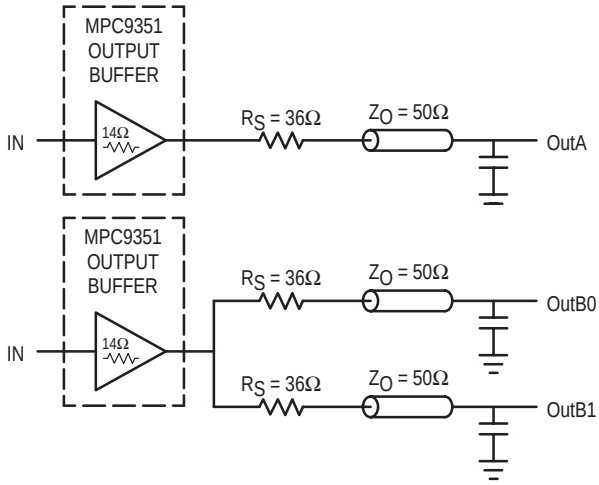



**Figure 7. Single versus Dual Transmission Lines**

The waveform plots in Figure 8. "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9351 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9351. The output waveform in Figure 8. "Single versus Dual Line Termination Waveforms" shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 ( 25 \div (18+17+25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

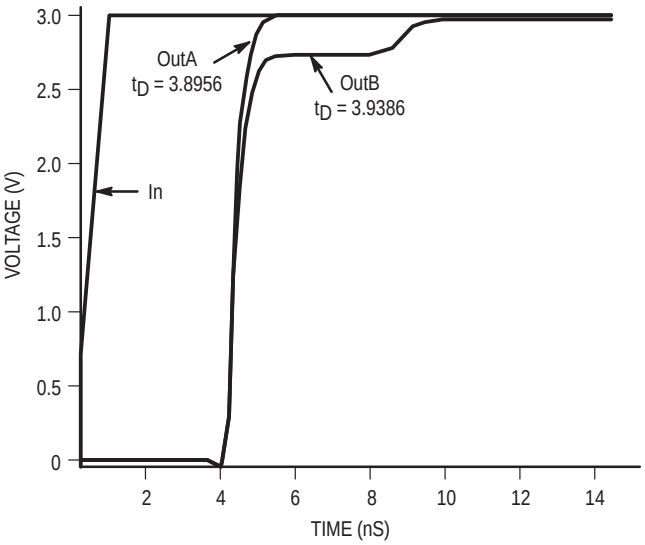
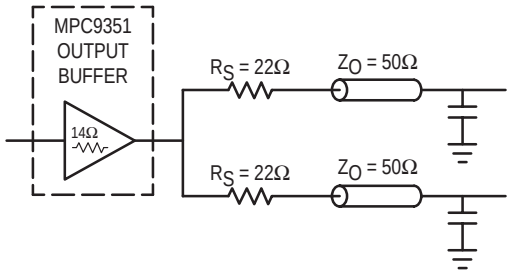



**Figure 8. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 9. "Optimized Dual Line Termination" should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 9. Optimized Dual Line Termination**

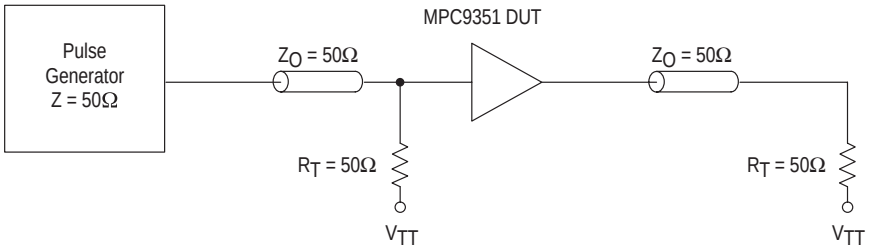



**Figure 10. TCLK MPC9351 AC test reference for $V_{CC}$ = 3.3V and $V_{CC}$ = 2.5V**

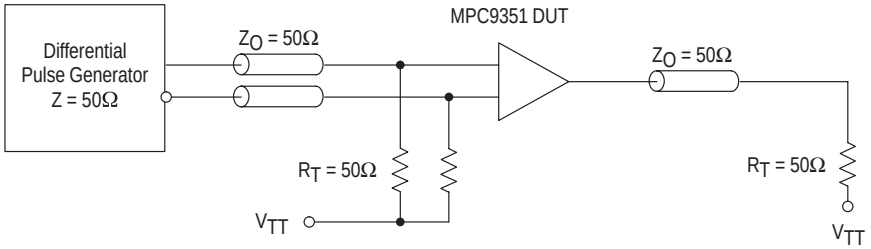



**Figure 11. PCLK MPC9351 AC test reference**

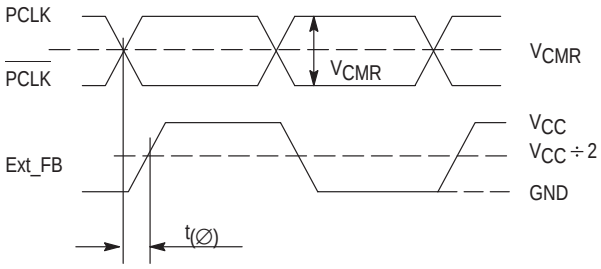



**Figure 12. Propagation delay ($t_{PD}$, static phase offset) test reference**

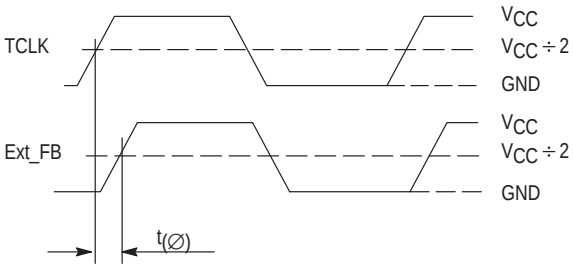
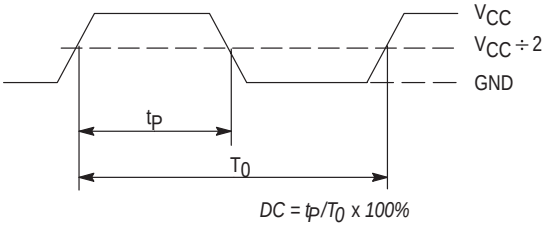
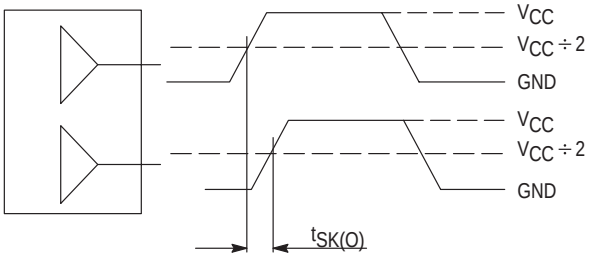



**Figure 13. Propagation delay ($t_{PD}$) test reference**



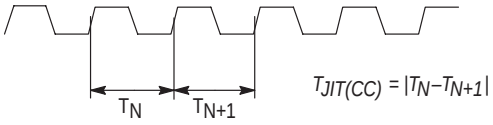

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 14. Output Duty Cycle (DC)**



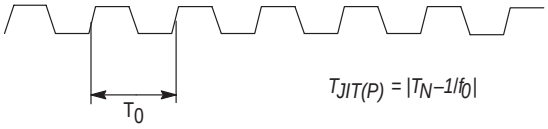

The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 15. Output–to–output Skew $t_{SK(O)}$**



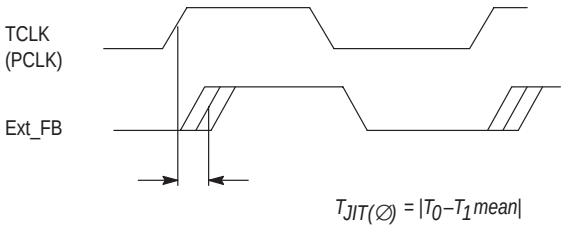

The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 16. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 17. Period Jitter**




The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**Figure 18. I/O Jitter**

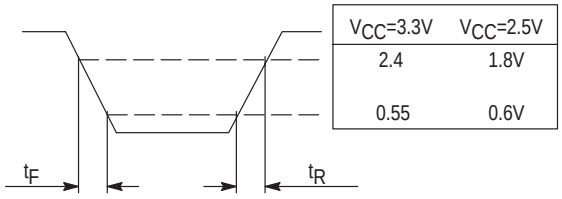
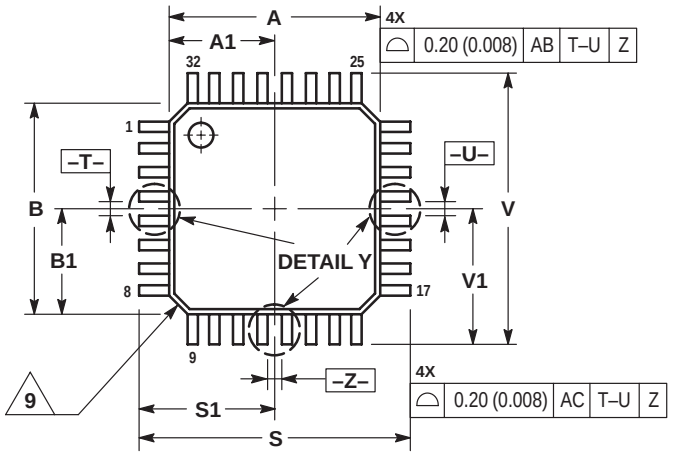
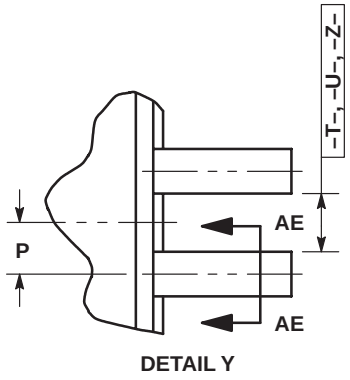



**Figure 19. Transition Time Test Reference**

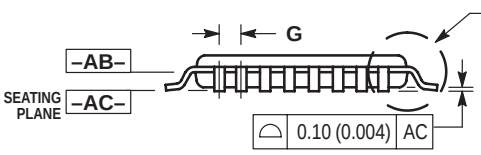
## OUTLINE DIMENSIONS

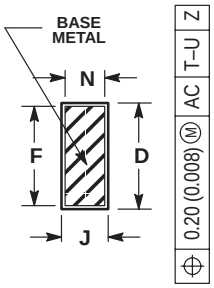
**FA SUFFIX**
LQFP PACKAGE
CASE 873A-02
ISSUE A



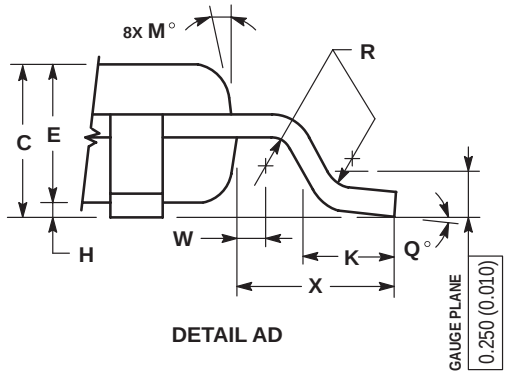




DETAIL Y




SECTION AE–AE




DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 7.000 BSC | | 0.276 BSC | |
| A1 | 3.500 BSC | | 0.138 BSC | |
| B | 7.000 BSC | | 0.276 BSC | |
| B1 | 3.500 BSC | | 0.138 BSC | |
| C | 1.400 | 1.600 | 0.055 | 0.063 |
| D | 0.300 | 0.450 | 0.012 | 0.018 |
| E | 1.350 | 1.450 | 0.053 | 0.057 |
| F | 0.300 | 0.400 | 0.012 | 0.016 |
| G | 0.800 BSC | | 0.031 BSC | |
| H | 0.050 | 0.150 | 0.002 | 0.006 |
| J | 0.090 | 0.200 | 0.004 | 0.008 |
| K | 0.500 | 0.700 | 0.020 | 0.028 |
| M | 12° REF | | 12° REF | |
| N | 0.090 | 0.160 | 0.004 | 0.006 |
| P | 0.400 BSC | | 0.016 BSC | |
| Q | 1° | 5° | 1° | 5° |
| R | 0.150 | 0.250 | 0.006 | 0.010 |
| S | 9.000 BSC | | 0.354 BSC | |
| S1 | 4.500 BSC | | 0.177 BSC | |
| V | 9.000 BSC | | 0.354 BSC | |
| V1 | 4.500 BSC | | 0.177 BSC | |
| W | 0.200 REF | | 0.008 REF | |
| X | 1.000 REF | | 0.039 REF | |

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