Low Voltage 1:18 Clock Distribution Chip

MPC940L

LOW VOLTAGE 1:18 CLOCK DISTRIBUTION CHIP

The MPC940L is a 1:18 low voltage clock distribution chip with 2.5V or 3.3V LVCMOS output capabilities. The device features the capability to select either a differential LVPECL or an LVCMOS compatible input. The 18 outputs are 2.5V or 3.3V LVCMOS compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output–to–output skews of 150ps, the MPC940L is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5V outputs also make the device ideal for supplying clocks for a high performance microprocessor based design. For a similar device at a lower price/performance point the reader is referred to the MPC9109.

- LVPECL or LVCMOS Clock Input
- 2.5V LVCMOS Outputs for Pentium II Microprocessor Support
- 150ps Maximum Output–to–Output Skew
- Maximum Output Frequency of 250MHz
- 32–Lead LQFP Packaging
- Dual or Single Supply Device:
  - Dual V_{CC} Supply Voltage, 3.3V Core and 2.5V Output
  - Single 3.3V V_{CC} Supply Voltage for 3.3V Outputs
  - Single 2.5V V_{CC} Supply Voltage for 2.5V I/O

FA SUFFIX
32–LEAD LQFP PACKAGE
CASE 873A–02

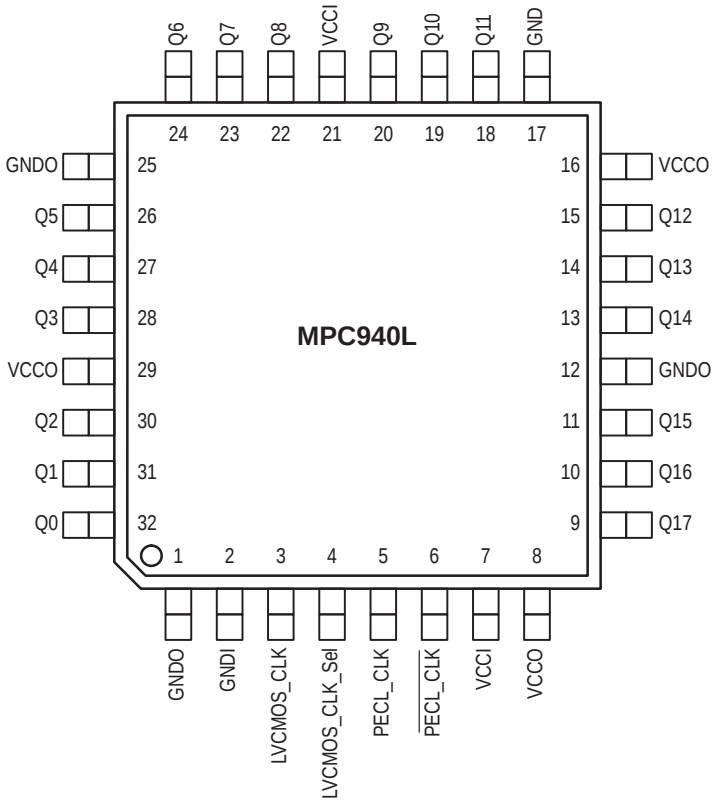
With a low output impedance (≈20Ω), in both the HIGH and LOW logic states, the output buffers of the MPC940L are ideal for driving series terminated transmission lines. With a 20Ω output impedance the 940L has the capability of driving two series terminated lines from each output. This gives the device an effective fanout of 1:36. If a lower output impedance is desired please see the MPC942 data sheet.

The differential LVPECL inputs of the MPC940L allow the device to interface directly with a LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS_CLK_Sel pin will select the LVCMOS level clock input. All inputs of the MPC940L have internal pullup/pulldown resistor so they can be left open if unused.

The MPC940L is a single or dual supply device. The device power supply offers a high degree of flexibility. The device can operate with a 3.3V core and 3.3V output, a 3.3V core and 2.5V outputs as well as a 2.5V core and 2.5V outputs. The 32–lead LQFP package was chosen to optimize performance, board space and cost of the device. The 32–lead LQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

LOGIC DIAGRAM

Pinout: 32–Lead TQFP (Top View)



FUNCTION TABLE

LVCMOS_CLK_Sel	Input
0	PECL_CLK
1	LVCMOS_CLK

POWER SUPPLY VOLTAGES

Supply Pin	Voltage Level
VCCI	2.5V or 3.3V ± 5%
VCCO	2.5V or 3.3V ± 5%

PIN CONFIGURATIONS

Pin	I/O	Type	Function
PECL_CLK PECL_CLK	Input	LVPECL	Reference Clock Input
LVCMOS_CLK	Input	LVCMOS	Alternative Reference Clock Input
LVCMOS_CLK_SEL	Input	LVCMOS	Selects Clock Source
Q0–Q17	Output	LVCMOS	Clock Outputs
VCCO		Supply	Output Positive Power Supply
VCCI		Supply	Core Positive Power Supply
GNDO		Supply	Output Negative Power Supply
GNDI		Supply	Core Negative Power Supply

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CCI} = 3.3V ±5%; V_{CCO} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	CMOS_CLK	2.4		V_{CCI}	V	
V_{IL}	Input LOW Voltage	CMOS_CLK			0.8	V	
V_{PP}	Peak–to–Peak Input Voltage	PECL_CLK	500		1000	mV	
V_{CMR}	Common Mode Range	PECL_CLK	V_{CC}–1.4		V_{CC}–0.6	V	
V_{OH}	Output HIGH Voltage		2.4			V	I_{OH} = –20mA
V_{OL}	Output LOW Voltage				0.5	V	I_{OH} = 20mA
I_{IN}	Input Current				±200	µA	
C_{IN}	Input Capacitance			4.0		pF	
C_{pd}	Power Dissipation Capacitance			10		pF	per output
Z_{OUT}	Output Impedance		18	23	28	Ω	
I_{CC}	Maximum Quiescent Supply Current			0.5	1.0	mA	

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CCI} = 3.3V ±5%; V_{CCO} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency				250	MHz	
t_{PLH}	Propagation Delay	PECL_CLK ≤ 150MHz CMOS_CLK ≤ 150MHz	2.0 1.8	2.7 2.5	3.4 3.0	ns	Note 1.
t_{PLH}	Propagation Delay	PECL_CLK > 150MHz CMOS_CLK > 150MHz	2.0 1.8	2.9 2.4	3.7 3.2	ns	
$t_{sk(o)}$	Output–to–Output Skew	PECL_CLK CMOS_CLK			150 150	ps	Note 1.
$t_{sk(pp)}$	Part–to–Part Skew	PECL_CLK < 150MHz CMOS_CLK < 150MHz			1.4 1.2	ns	Notes 1., 2.
$t_{sk(pp)}$	Part–to–Part Skew	PECL_CLK > 150MHz CMOS_CLK > 150MHz			1.7 1.4	ns	Notes 1., 2.
$t_{sk(pp)}$	Part–to–Part Skew	PECL_CLK CMOS_CLK			850 750	ps	Notes 1., 3.
DC	Output Duty Cycle	f_{CLK} < 134 MHz f_{CLK} ≤ 250 MHz	45 40	50 50	55 60	% %	Input DC = 50% Input DC = 50%
t_r, t_f	Output Rise/Fall Time		0.3		1.1	ns	0.5 – 2.4 V

1. Tested using standard input levels, Production tested @ 150MHz.
2. Across temperature and voltage ranges, Includes output skew.
3. For a specific temperature and voltage, Includes output skew.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CCI} = 3.3V ±5%; V_{CCO} = 2.5V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	CMOS_CLK	2.4		V_{CCI}	V	
V_{IL}	Input LOW Voltage	CMOS_CLK			0.8	V	
V_{PP}	Peak–to–Peak Input Voltage	PECL_CLK	500		1000	mV	
V_{CMR}	Common Mode Range	PECL_CLK	V_{CC}–1.4		V_{CC}–0.6	V	
V_{OH}	Output HIGH Voltage		1.8			V	I_{OH} = –20mA
V_{OL}	Output LOW Voltage				0.5	V	I_{OH} = 20mA
I_{IN}	Input Current				±200	µA	
C_{IN}	Input Capacitance			4.0		pF	
C_{pd}	Power Dissipation Capacitance			10		pF	per output
Z_{OUT}	Output Impedance			23		Ω	
I_{CC}	Maximum Quiescent Supply Current			0.5	1.0	mA	

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CCI} = 3.3V ±5%; V_{CCO} = 2.5V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency				250	MHz	
t_{PLH}	Propagation Delay	PECL_CLK ≤ 150MHz CMOS_CLK ≤ 150MHz	2.0 1.7	2.8 2.5	3.5 3.0	ns	Note 1.
t_{PLH}	Propagation Delay	PECL_CLK > 150MHz CMOS_CLK > 150MHz	2.0 1.8	2.9 2.5	3.8 3.3	ns	
$t_{sk(o)}$	Output–to–Output Skew	PECL_CLK CMOS_CLK			150 150	ps	Note 1.
$t_{sk(pp)}$	Part–to–Part Skew	PECL_CLK < 150MHz CMOS_CLK < 150MHz			1.5 1.3	ns	Notes 1., 2.
$t_{sk(pp)}$	Part–to–Part Skew	PECL_CLK > 150MHz CMOS_CLK > 150MHz			1.8 1.5	ns	Notes 1., 2.
$t_{sk(pp)}$	Part–to–Part Skew	PECL_CLK CMOS_CLK			850 750	ps	Notes 1., 3.
DC	Output Duty Cycle	f_{CLK} < 134 MHz f_{CLK} ≤ 250 MHz	45 40	50 50	55 60	% %	Input DC = 50% Input DC = 50%
t_r, t_f	Output Rise/Fall Time		0.3		1.2	ns	0.5 – 1.8 V

1. Tested using standard input levels, Production tested @ 150MHz.
2. Across temperature and voltage ranges, Includes output skew.
3. For a specific temperature and voltage, Includes output skew.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CCI} = 2.5V ±5%; V_{CCO} = 2.5V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	CMOS_CLK	2.0		V_{CCI}	V	
V_{IL}	Input LOW Voltage	CMOS_CLK			0.8	V	
V_{PP}	Peak–to–Peak Input Voltage	PECL_CLK	500		1000	mV	
V_{CMR}	Common Mode Range	PECL_CLK	V_{CC}–1.0		V_{CC}–0.6	V	
V_{OH}	Output HIGH Voltage		1.8			V	I_{OH} = –12mA
V_{OL}	Output LOW Voltage				0.5	V	I_{OH} = 12mA
I_{IN}	Input Current				±200	µA	
C_{IN}	Input Capacitance			4.0		pF	
C_{pd}	Power Dissipation Capacitance			10		pF	per output
Z_{OUT}	Output Impedance		18	23	28	Ω	
I_{CC}	Maximum Quiescent Supply Current			0.5	1.0	mA	

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CCI} = 2.5V ±5%; V_{CCO} = 2.5V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency				200	MHz	
t_{PLH}	Propagation Delay	PECL_CLK ≤ 150MHz CMOS_CLK ≤ 150MHz	2.6 2.3	4.0 3.1	5.2 4.0	ns	Note 1.
t_{PLH}	Propagation Delay	PECL_CLK > 150MHz CMOS_CLK > 150MHz	2.8 2.3	3.8 3.1	5.0 4.0	ns	
$t_{sk(o)}$	Output–to–Output Skew	PECL_CLK CMOS_CLK			200 200	ps	Note 1.
$t_{sk(pp)}$	Part–to–Part Skew	PECL_CLK < 150MHz CMOS_CLK < 150MHz			2.6 1.7	ns	Notes 1., 2.
$t_{sk(pp)}$	Part–to–Part Skew	PECL_CLK > 150MHz CMOS_CLK > 150MHz			2.2 1.7	ns	Notes 1., 2.
$t_{sk(pp)}$	Part–to–Part Skew	PECL_CLK CMOS_CLK			1.2 1.0	ns	Notes 1., 3.
DC	Output Duty Cycle	f_{CLK} < 134 MHz f_{CLK} ≤ 250 MHz	45 40	50 50	55 60	% %	Input DC = 50% Input DC = 50%
t_r, t_f	Output Rise/Fall Time		0.3		1.2	ns	0.5 – 1.8 V

1. Tested using standard input levels, Production tested @ 150MHz.
2. Across temperature and voltage ranges, Includes output skew.
3. For a specific temperature and voltage, Includes output skew.

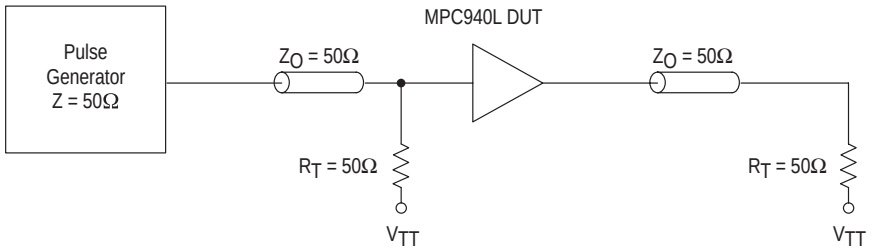


Figure 1. LVCMOS_CLK MPC940L AC test reference for V_{CC} = 3.3V and V_{CC} = 2.5V

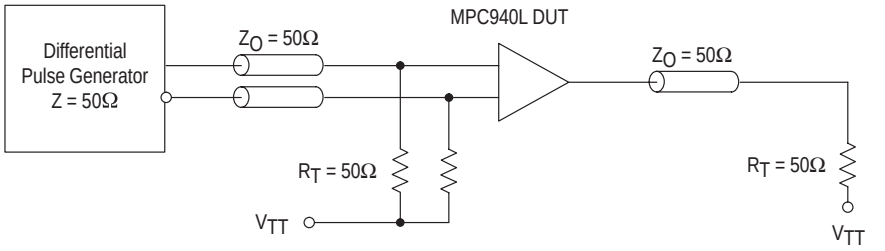


Figure 2. PECL_CLK MPC940L AC test reference for V_{CC} = 3.3V and V_{CC} = 2.5V

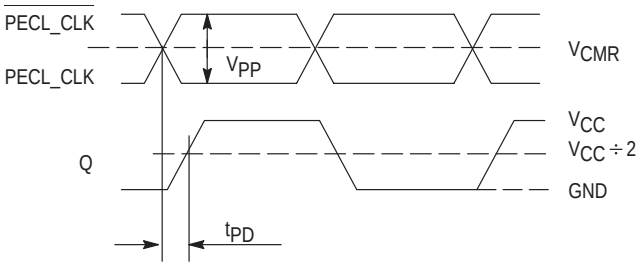


Figure 3. Propagation delay (t_{PD}) test reference

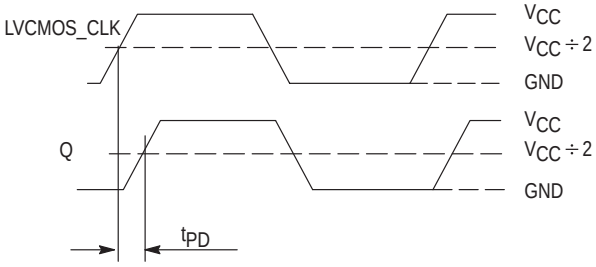
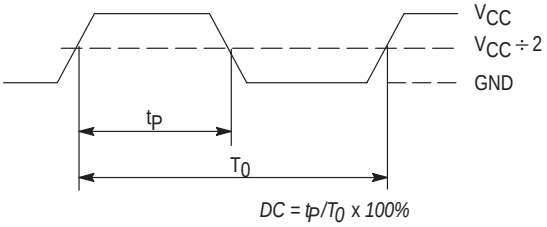
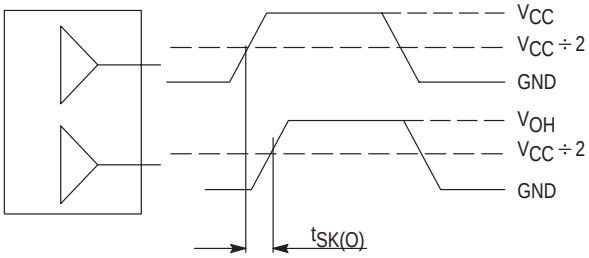


Figure 4. LVCMOS Propagation delay (t_{PD}) test reference



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 5. Output Duty Cycle (DC)



The pin–to–pin skew is defined as the worst case difference in propagation delay between any two similar delay path within a single device

Figure 6. Output–to–output Skew $t_{SK(O)}$

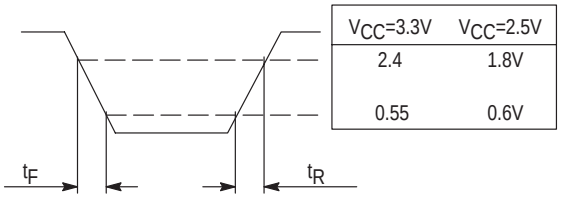


Figure 7. Output Transition Time Test Reference

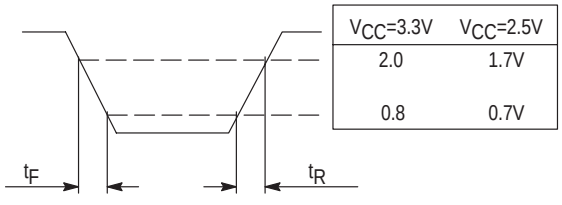
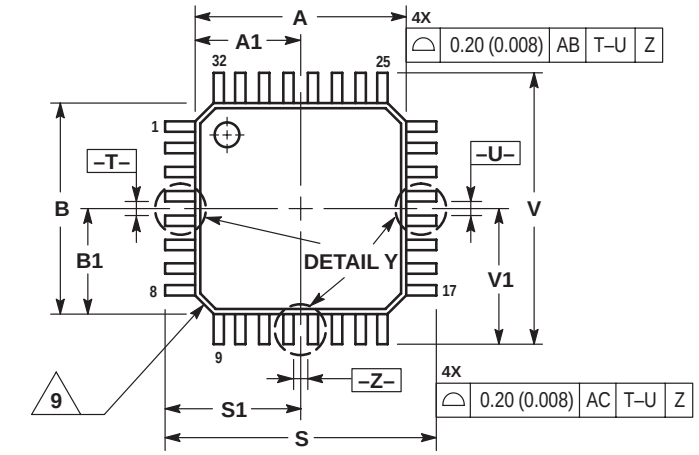
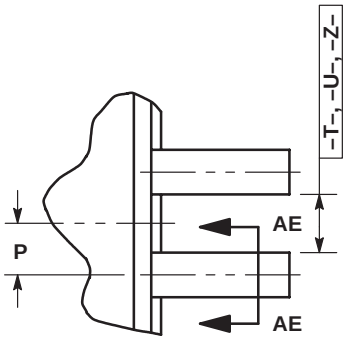


Figure 8. Input Transition Time Test Reference

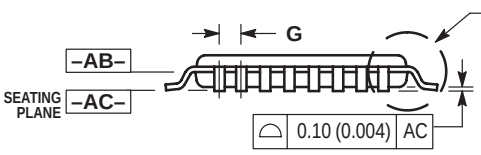
OUTLINE DIMENSIONS

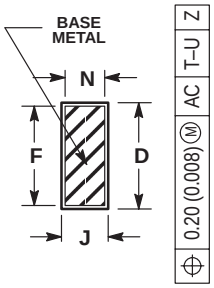
FA SUFFIX
QFP PACKAGE
CASE 873A–02
ISSUE A



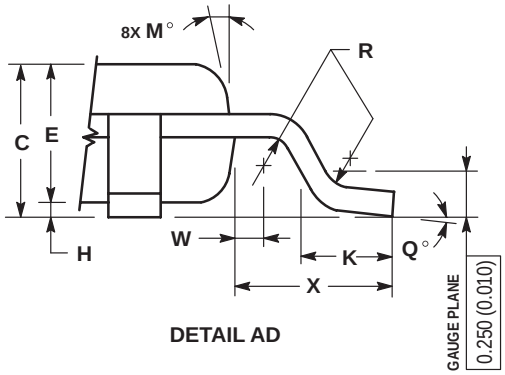


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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