**MOTOROLA**

SEMICONDUCTOR TECHNICAL DATA

## The MRFIC Line
# 1.8 GHz Power Amp/Switch

Designed primarily for use in DECT, Japan Personal Handy System (PHS) and other wireless Personal Communication Systems (PCS) applications. The MRFIC1807 includes a single–stage power amplifier and transmit/receive switch in a low–cost SOIC–16 package. The amplifier portion employs a depletion mode power GaAs MESFET and produces up to +27 dBm output with +19 dBm input. On–chip power control circuitry allows bias adjustment for optimum performance. The T/R switch is capable of handling up to +28 dBm through the transmit path without significant increase in insertion loss. The switch is controlled by CMOS logic level signals — no negative control voltage required. The MRFIC1807 is sized to be driven by the MRFIC1806 Driver/ Ramp IC.

Together with the rest of the MRFIC1800 GaAs ICs, this family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone.

- Usable 1500–2200 MHz
- 8.0 dB Gain Including Switch
- +26 dBm Minimum Output Power at Antenna Port
- 1.0 dB Typ RX Path Insertion Loss
- Simple Off–Chip Matching for Maximum Flexibility
- 3.0 to 5.0 V Supply
- No Spurious Outputs for Load VSWR up to 8:1
- CMOS Level Switching Signal for T/R Switch
- Order MRFIC1807R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1807

**MRFIC1807**

1.8 GHz POWER AMPLIFIER
AND TRANSMIT/RECEIVE
SWITCH
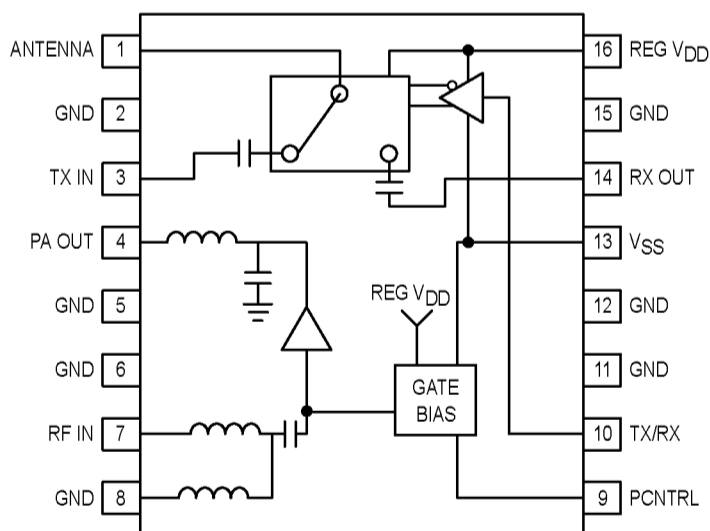GaAs MONOLITHIC
INTEGRATED CIRCUIT
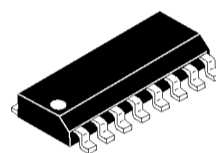
CASE 751B–05
(SO–16)



Figure 1. Pin Connection and Functional Block Diagram

**MOTOROLA**

ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C Unless Otherwise noted)

| Rating | Symbol | Limit | Unit |
|---|---|---|---|
| PA Supply Voltage | $V_{DD}$ | 6.0 | Vdc |
| Supply Voltage | REG $V_{DD}$ | 4.5 | Vdc |
| Supply Voltage | $V_{SS}$ | −4.0 | Vdc |
| RF Input Power | $P_{in}$ | +25 | dBm |
| Switch Control Voltage | TX/RX | 6.0 | Vdc |
| PA Control Voltage | PCNTRL | 3.0 | Vdc |
| Ambient Operating Temperature | $T_A$ | −10 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Thermal Resistance, Junction to Case | $\theta_{JC}$ | 24 | °C/W |

RECOMMENDED OPERATING RANGES

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| RF Input Frequency | $f_{RF}$ | 1.5 to 2.2 | GHz |
| PA Supply Voltage | $V_{DD}$ | 3.0 to 5.0 | Vdc |
| Supply Voltage | REG $V_{DD}$ | 2.9 to 3.1 | Vdc |
| Supply Voltage | $V_{SS}$ | −2.75 to −2.25 | Vdc |
| RF Input Power | $P_{IN}$ | +5.0 to +23 | dBm |
| Switch Control Voltage, High (TX Mode) | TX/RX | 2.8 to 3.5 | Vdc |
| Switch Control Voltage, Low (RX Mode) | TX/RX | −0.2 to 0.2 | Vdc |
| PA Control Voltage | PCNTRL | 0.0 to 2.5 | Vdc |

ELECTRICAL CHARACTERISTICS (1)

**Transmit Mode** ($V_{DD}$ = 3.5 V, REG $V_{DD}$ = 3.0 V, $T_A$ = 25°C, $V_{SS}$ = −2.5 V, PCNTRL 0 V to 2.5 V, $P_{IN}$ = 20 dBm @ 1.9 GHz, TX/RX = 3 V, $P_{OUT}$ Measured at ANT Port)

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Small Signal Gain ($P_{IN}$ = 0 dBm, PCNTRL set for $I_{DDQ}$ = 180 mA) | 7.0 | 8.0 | — | dB |
| Output Power (PCNTRL adjusted for efficiency ≥ 35%) | 26 | 26.8 | — | dBm |
| Output 1.0 dB Compression (PCNTRL set for $I_{DDQ}$ = 180 mA) | — | 25 | — | dBm |
| Harmonic Output (PCNTRL set for $P_{OUT}$ = 26 dBm) | — | −40 | — | dBc |
| Switch RX to TX Switching Time | — | 0.1 | — | μsec |
| TX/RX Control Input Current, Pin 10 | — | 0.2 | — | mA |
| Drain Efficiency ($P_{out}$ = 26 dBm) (2) | — | 40 | — | % |
| Supply Current, $I_{SS}$ | — | 0.8 | 1.2 | mA |
| Supply Current, REG $I_{DD}$ | — | 0.8 | 1.2 | mA |
| PCNTRL Control Input Current (Pin 9) | — | 15 | — | μA |
| Leakage Power at RX Port | — | −1 | + 6 | dBm |

**Receive Mode** ($V_{DD}$ = 0 V, REG $V_{DD}$ = 3.0 V, $V_{SS}$ = −2.5 V, TX/RX = 0 V, $T_A$ = 25°C, Freq = 1.9 GHz)

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| ANT to RX Insertion Loss | — | 1.0 | 1.3 | dB |
| Switch TX to RX Switching Time | — | 1.0 | — | μsec |
| Supply Current, REG $I_{DD}$ | — | 60 | 250 | μA |
| Supply Current, $I_{SS}$ | — | 60 | 250 | μA |

NOTES:
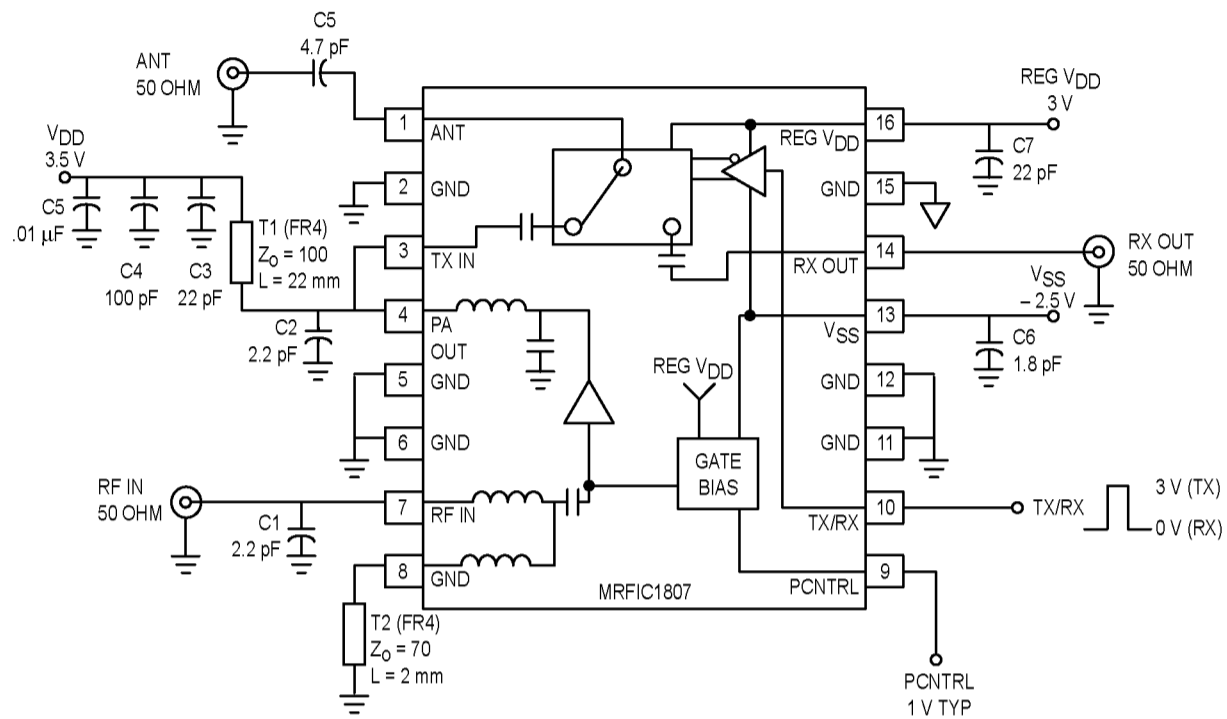1. Measured with circuit configuration shown in Figure 2.
2. Includes switch loss.

**Figure 2. 1.9 GHz Applications Circuit Configuration**

**Table 1. Small Signal S−Parameters**
($V_{DD}$ = 3.5 V, $I_{DDQ}$ = 180 mA, $T_A$ = 25°C, no input or output matching)

| Freq (GHz) | $S_{11}$ | | $S_{21}$ | | $S_{12}$ | | $S_{22}$ | |
|---|---|---|---|---|---|---|---|---|
| | Mag | Angle | Mag | Angle | Mag | Angle | Mag | Angle |
| 1.5 | 0.614 | −171.5 | 2.203 | 82.6 | 0.104 | 74.5 | 0.741 | 175.4 |
| 1.6 | 0.695 | 175.7 | 1.871 | 71.7 | 0.110 | 69.2 | 0.746 | 171.5 |
| 1.7 | 0.747 | 167.3 | 1.647 | 63.4 | 0.108 | 64.0 | 0.745 | 167.4 |
| 1.8 | 0.777 | 160.3 | 1.473 | 56.2 | 0.106 | 58.7 | 0.746 | 163.0 |
| 1.9 | 0.799 | 154.2 | 1.341 | 49.2 | 0.120 | 54.0 | 0.753 | 158.9 |
| 2.0 | 0.814 | 148.3 | 1.230 | 43.0 | 0.118 | 49.6 | 0.758 | 154.8 |
| 2.1 | 0.826 | 142.5 | 1.128 | 36.8 | 0.114 | 45.2 | 0.764 | 150.6 |
| 2.2 | 0.835 | 137.0 | 1.041 | 31.2 | 0.120 | 40.6 | 0.767 | 146.7 |
| 2.3 | 0.842 | 131.4 | 0.959 | 26.4 | 0.127 | 37.0 | 0.780 | 143.4 |
| 2.4 | 0.856 | 126.6 | 0.895 | 21.1 | 0.124 | 33.8 | 0.796 | 139.8 |
| 2.5 | 0.870 | 121.7 | 0.840 | 16.0 | 0.126 | 30.4 | 0.808 | 136.4 |
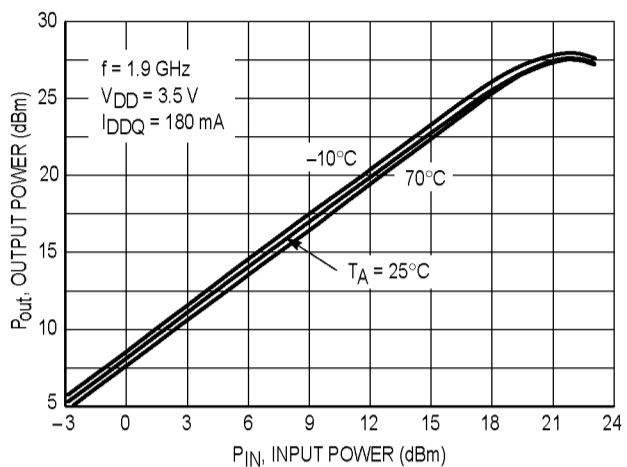
**Figure 3. Output Power versus Input Power**
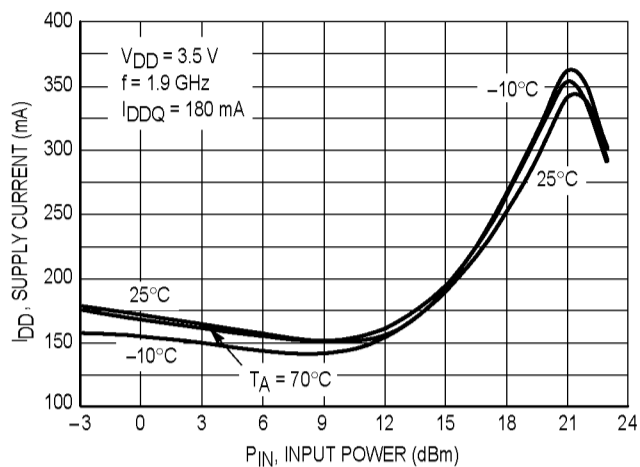


**Figure 4. Supply Current versus Input Power**
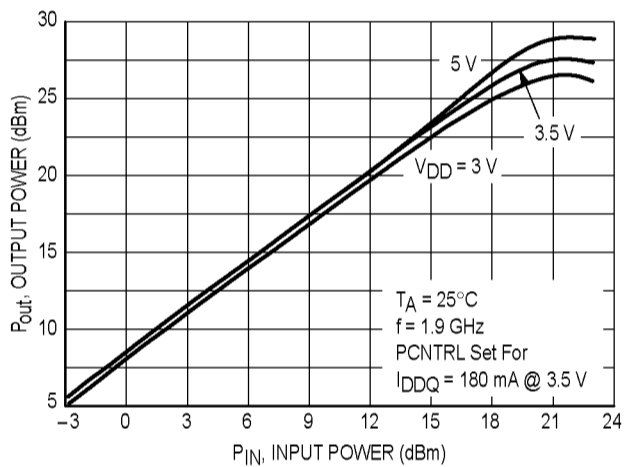


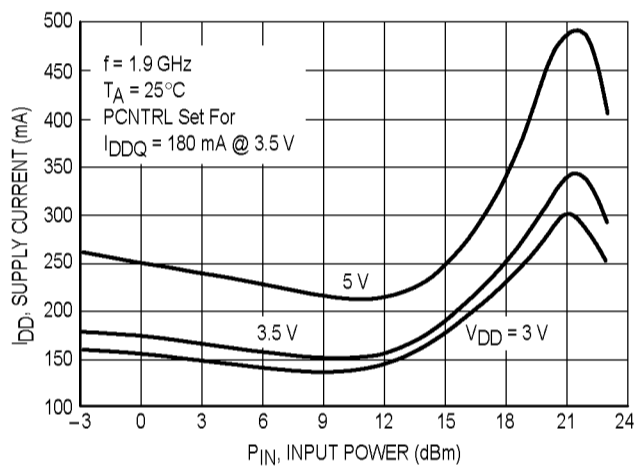**Figure 5. Output Power versus Input Power**



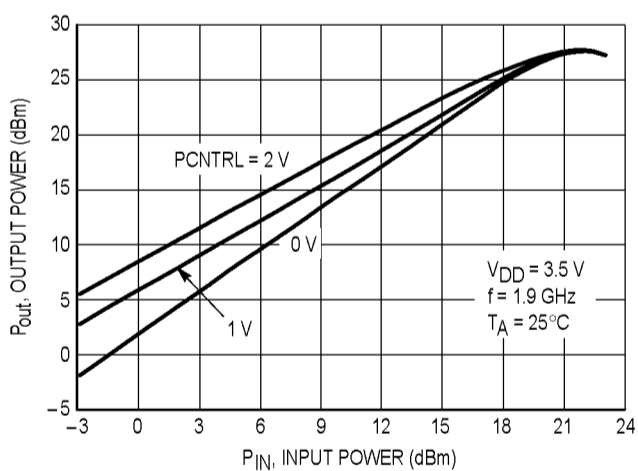**Figure 6. Supply Current versus Input Power**
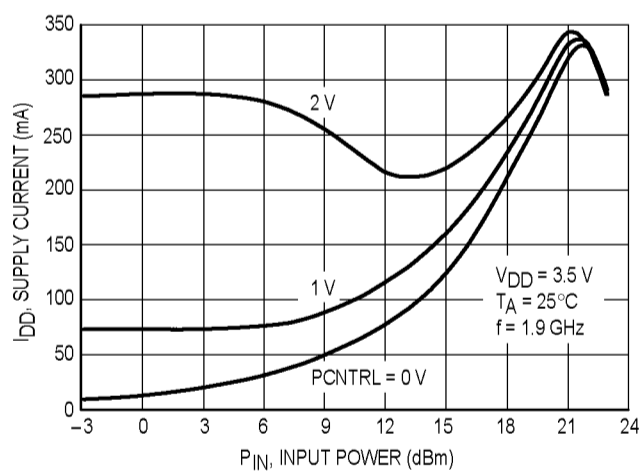


**Figure 7. Output Power versus Input Power**



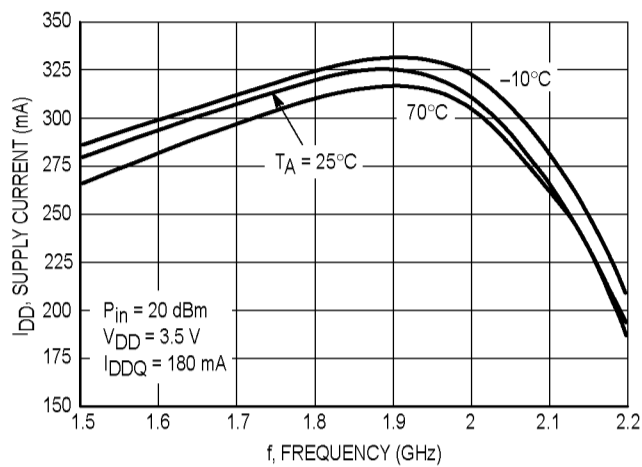**Figure 8. Supply Current versus Input Power**
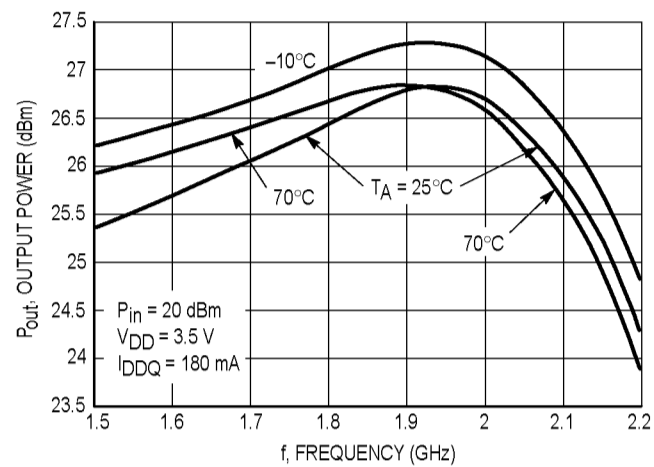
Figure 9. Supply Current versus Frequency
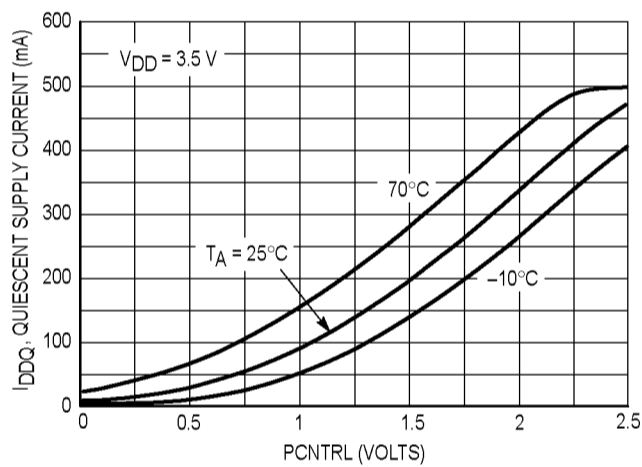
Figure 10. Output Power versus Frequency
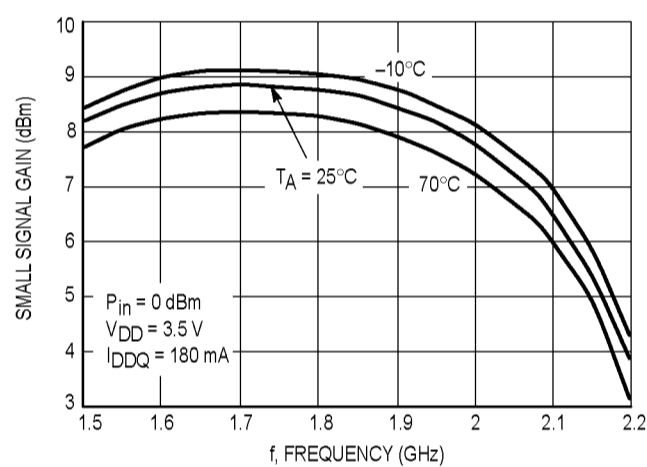
Figure 11. Quiescent Supply Current versus PCNTRL

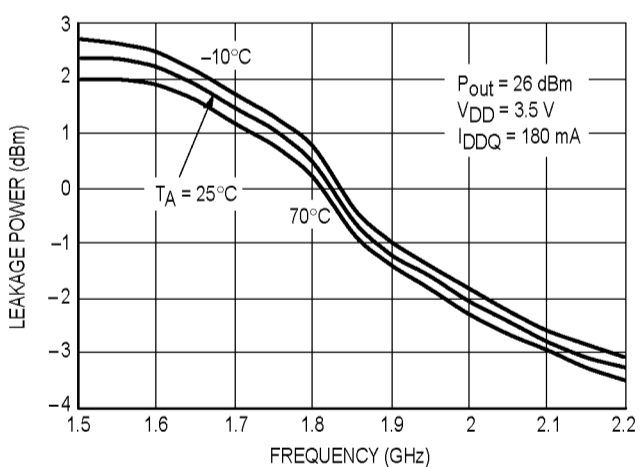Figure 12. Small Signal Gain versus Frequency

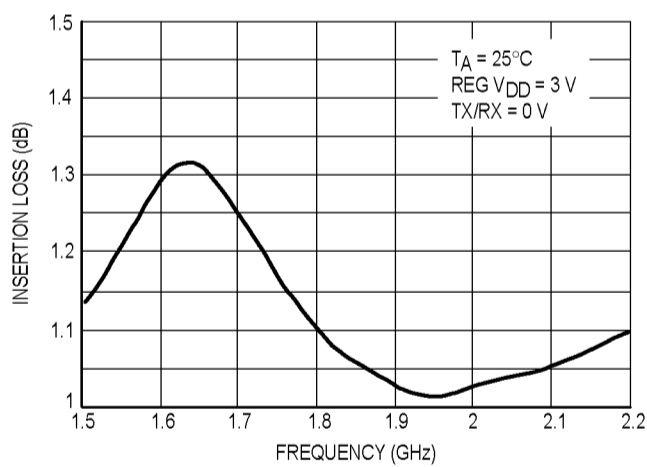Figure 13. Leakage Power at RX Port in TX
Mode versus Frequency

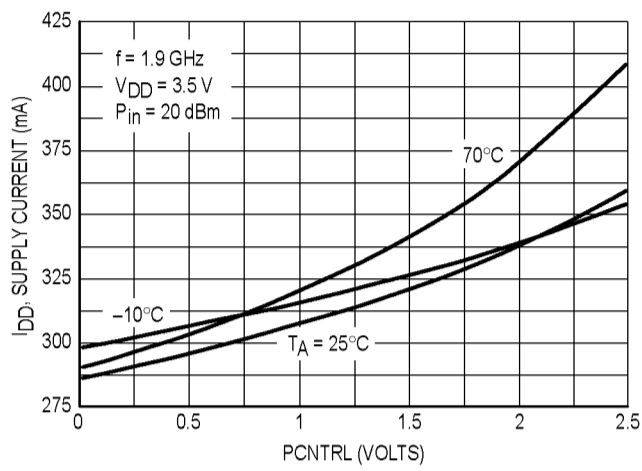Figure 14. RX Path Insertion Loss in RX Mode
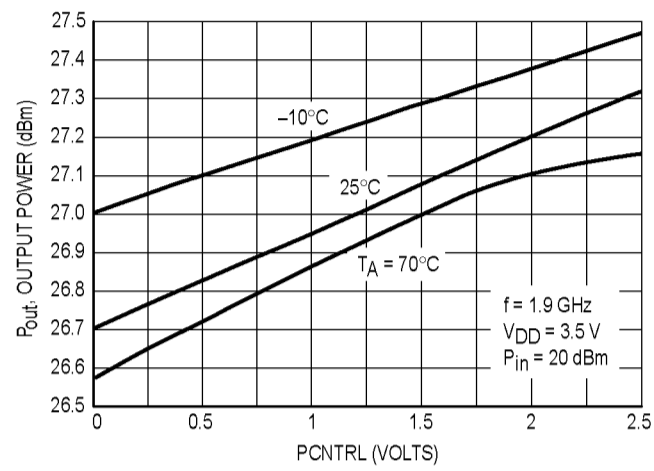versus Frequency

**Figure 15. Supply Current versus PCNTRL**



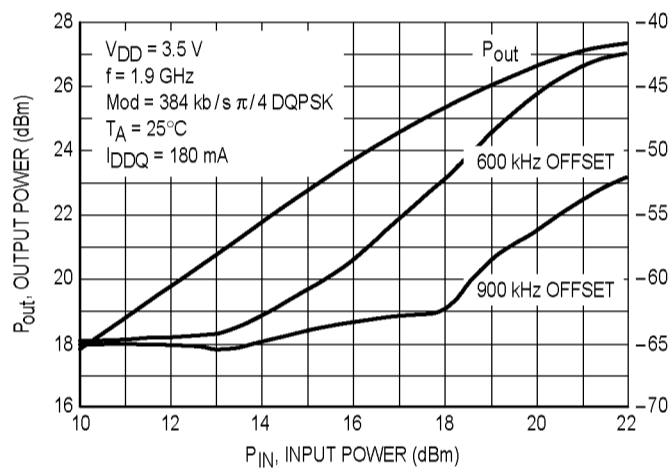**Figure 16. Output Power versus PCNTRL**



**Figure 17. Output Power and Adjacent Channel
Power Ratio versus Input Power**

# DESIGN AND APPLICATIONS INFORMATION

## DESIGN PHILOSOPHY

The MRFIC1807 is designed to operate with the MRFIC1806 Driver/Ramp IC in 1.9 GHz Personal Communication System (PCS) applications such as Europe's DECT and Japan's PHS. The design incorporates a depletion mode GaAs power MESFET with a high–power transmit/receive switch and associated bias circuitry in one low–cost SOIC–16 package.

The power MESFET is sized to produce at least 27 dBm saturated output power, including switch loss, from a 3.5 V supply, but the output power can be controlled using the PCNTRL input. This control voltage also allows setting of the quiescent current of the FET. PCNTRL can be set to give best efficiency or linearity for the particular system application. The TX/RX control pin allows fast switching of the T/R switch for TDMA applications. When switching from transmit to receive, the battery supply voltage should be removed from the PA (Pin 4), to avoid excessive current drain. This is usually accomplished using an external pass transistor controlled by the TX/RX signal. Alternatively, if PCNTRL is reduced to 0 V during RX mode, the bias current is reduced to nearly zero.

The Transmit/Receive switch is a reflective MESFET design which is optimized for low loss and power handling in transmit mode. The design can handle 28 dBm of transmit power without significant increase in insertion loss. A regulated 3.0 Volt supply is required at pin 16 for the T/R switch and the bias and control circuitry.

## DECT APPLICATIONS

Figure 2 shows the component values for a DECT implementation of the MRFIC1807. For use in equipment designed for DECT, the power amplifier is operated close to saturation to improve device efficiency. Maximum power output at the antenna connector is 24 dBm during a burst. The constant envelope characteristics of the GMSK modulation allow non–linear amplification without spectral regrowth. The transmit signal must be shaped or "ramped" to meet system transmit turn on time requirements of 10 μsec minimum while not splattering into adjacent channels. A turn on time on greater than

2.0 μsec has been shown to give adequate adjacent channel power performance. Most DECT realizations have the modulation applied to the transmit VCO so the most straight forward way of implementing this ramping function is at the power amplifier. The MRFIC1806 Driver/Ramp IC has an on–chip ramping circuit specifically designed for DECT. When ramped in this manner, the MRFIC1806 will supply the appropriately ramped RF signal to the MRFIC1807 which only has to be turned on and off with TX/RX. Alternate off–chip ramping can be implemented either with external components or at baseband. Consult the MRFIC1806 datasheet for more information.
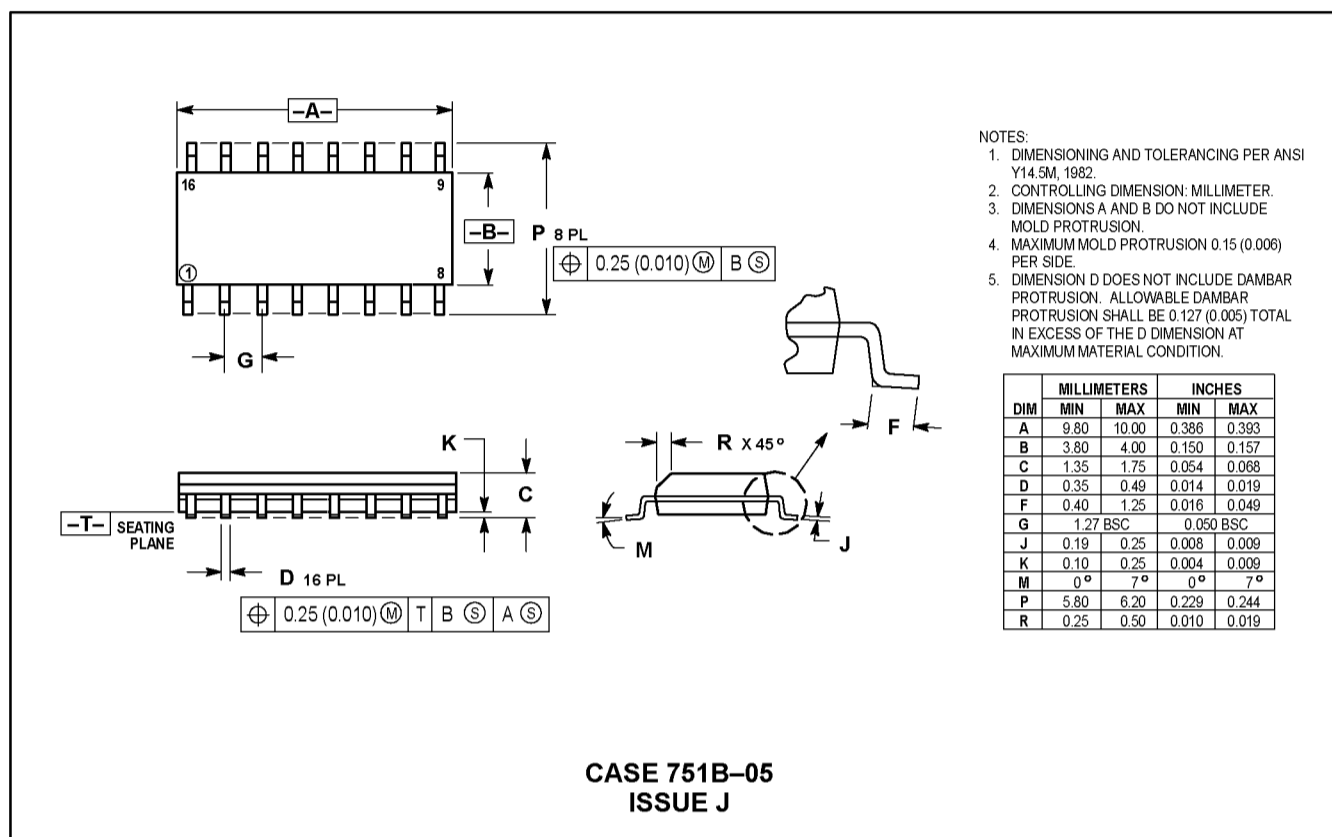
## PHS APPLICATIONS

For Japan's Personal Handy System applications, the modulation is $\pi$/4 DQPSK. When amplified with a non–linear amplifier, the signal will regrow the sidebands which have been carefully filtered at baseband, resulting in adjacent channel interference. To avoid this spectral regrowth, the amplifier must be operated "backed off" from saturation. The amount of backoff required has been shown to be a function of amplifier saturated output capability and may be as high as 5.0 dB. The PHS specification calls for a maximum average power during a burst to be 19 dBm. This is consistent with 5.0 dB backoff from the DECT operating point so the same DECT operating condition could be used. Alternatively, PCNTRL can be adjusted for a lower bias point to improve efficiency or higher bias for better linearity. With $\pi$/4 DQPSK modulation, ramping can be accomplished in the encoder so no external ramp circuit is needed. See the MRFIC1806 data sheet for further details.

## EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

# PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
|     | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

**CASE 751B–05**
**ISSUE J**