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MRFIC1859

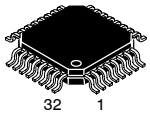
Dual-Band/GSM 3.6 V Integrated Power Amplifier

The MRFIC1859 is a dual–band, single supply RF Power Amplifier for GSM900/DCS1800 hand held radios. The on–chip spur free voltage generator reduces the number of external components by eliminating the need for a negative voltage supply. The device output power can be controlled open loop without the use of directional coupler and detection diode. The MRFIC1859 is General Packet Radio Service (GPRS) compatible. The device is packaged in a TQFP–32EP with exposed backside pad allowing excellent electrical and thermal performance through a solderable contact.

- Single Positive Supply Solution
- Input/Output External Matching
- High Power and Efficiency
- Typical 3.6 V Characteristics:
  P_{out} = 36.2 dBm, PAE = 53% for GSM
  P_{out} = 34 dBm, PAE = 43% for DCS
- Crosstalk Harmonic Leakage of –27 dBm Typical (GSM)

DUAL–BAND GSM 3.6 V IPA

SEMICONDUCTOR TECHNICAL DATA



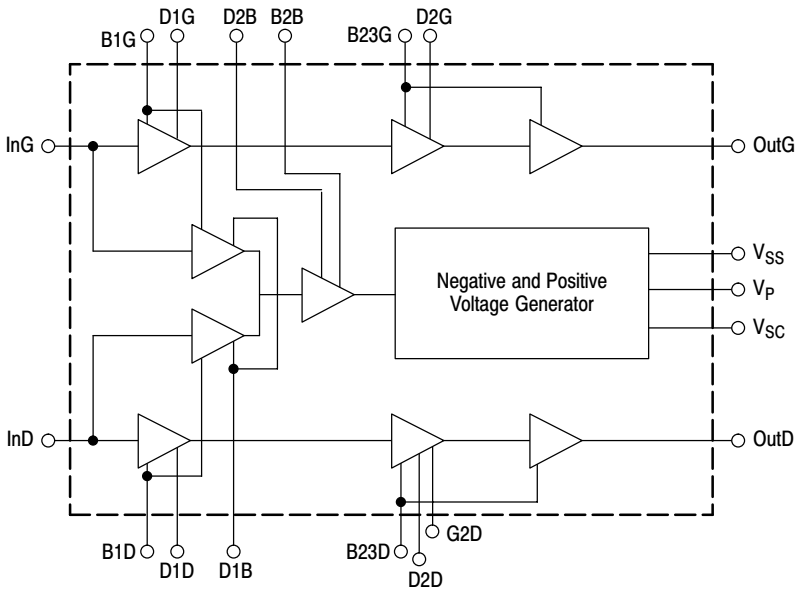
(Scale 2:1)

PLASTIC PACKAGE
CASE 873E
(TQFP–32EP)

ORDERING INFORMATION

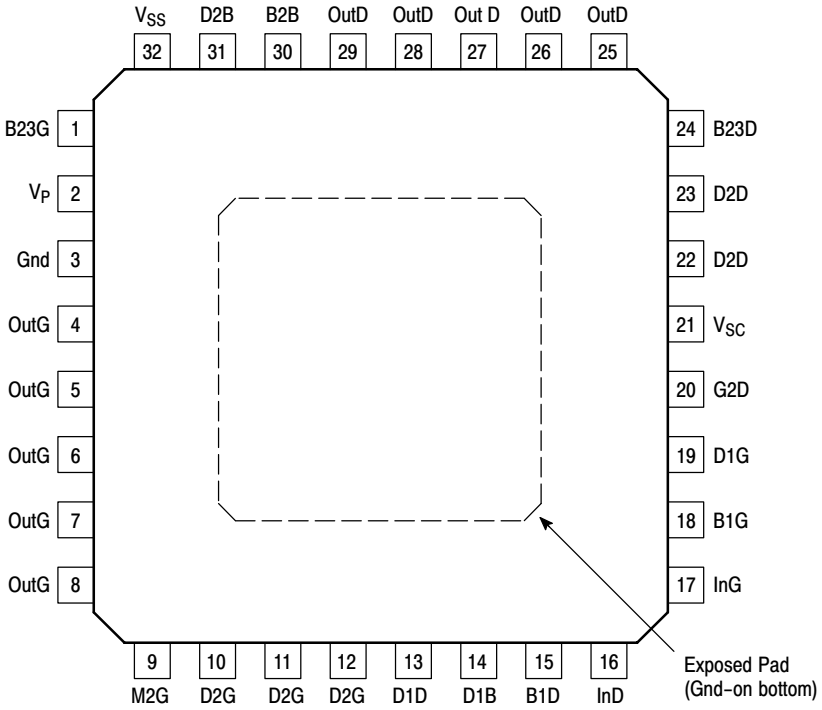
Device	Operating Temperature Range	Package
MRFIC1859R2	T_C = –35 to 100°C	TQFP–32EP

Simplified Block Diagram



This device contains 21 active transistors.

PIN CONNECTIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	$V_{D1B,D2B}$ $V_{D1G,D2G,}$ D3G,D1D, D2D,D3D	6.0	V
RF Input Power	InG, InD	12	dBm
RF Output Power GSM Section DCS Section	 OutG OutD	 38 36	dBm
Operating Case Temperature Range	T_C	–35 to 100	°C
Storage Temperature Range	T_{stg}	–55 to 150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	15	°C/W

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Contitions or Electrical Characteristics tables.
2. Meets Human Body Model (HBM) ≤100 V and Machine Model (MM) ≤60 V. Additional ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply	$V_{D1B,D2B}$ $V_{D1G,D2G,}$ D3G,D1D, D2D,D3D	2.8	–	5.5	V
Input Power GSM	InG	3.0	–	10	dBm
Input Power DCS	InD	5.0	–	12	dBm

ELECTRICAL CHARACTERISTICS ($V_{D1B, D2B}$ = 3.6 V, $V_{D1G,D2G,D3G}$ = 3.6 V or $V_{D1D,D2D,D3D}$ = 3.6 V, Peak measurement at 12.5% duty cycle, 4.6 ms period, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
GSM SECTION (P_{in} = 3.0 dBm)					
Frequency Range	BW	880	–	915	MHz
Output Power	P_{out}	35	36.2	–	dBm
Power Added Efficiency	PAE	45	53	–	%
Output Power @ Low Voltage ($V_{D1G,D2G,D3G}$= 3.0 V)	P_{out}	33.5	34.7	–	dBm
Harmonic Output $2f_o$ $\geq 3f_o$		 – –	 –35 –60	 –30 –45	dBc
Second Harmonic Leakage at DCS Output (Crosstalk isolation)		–	–25	–15	dBm
Input Return Loss	$\|S_{11}\|$	–	12	–	dB
Output Power Isolation with Buffer On (P_{in} = 3.0 dBm, $V_{D1B,D2B}$ = 3.6 V, $V_{D1G,D2G,D3G}$ = 0 V)	P_{on}	–	–8.0	–3.0	dBm
Output Power Isolation (P_{in} = 3.0 dBm, $V_{D1B,D2B}$ = 0 V, $V_{D1G,D2G,D3G}$ = 0 V)	P_{off}	–	–42	–	dBm
Noise Power in Rx Band 925 to 960 MHz (100 kHz measurement bandwidth) 925 to 935 MHz 935 to 960 MHz	NP	 	 –90 -90	 –67 –79	dBm
Negative Voltage (P_{in} = 2.0 dBm, $V_{D1B, D2B}$ = 3.0 V)	V_{SS}	–	–	–4.85	V
Negative Voltage Settling time (P_{in} = 3.0 dBm, $V_{D1B,D2B}$ stepped from 0 to 3.0 V)	T_S	–	0.7	2.0	µs
Stability–Spurious Output (P_{out} = 5.0 to 35 dBm, Load VSWR = 6:1 all Phase Angle, Source VSWR = 3:1, at any phase angle Adjust $V_{D1G,D2G,D3G}$ for specified power)	P_{spur}	–	–	–60	dBc
Load Mismatch Stress (P_{out} = 5.0 to 35 dBm, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust $V_{D1G,D2G,D3G}$ for specified power)		No Degradation in Output Power Before and After Test			
Positive Voltage (P_{in} = 3.0 dBm, V_{D1B} = V_{D2B} = 3.0 V)	V_P	6	10	–	V
DCS SECTION (P_{in} = 5.0 dBm)					
Frequency Range	BW	1710	–	1785	MHz
Output Power	P_{out}	33	34	–	dBm
Power Added Efficiency	PAE	35	43	–	%
Output Power @ Low Voltage ($V_{D1D,D2D,D3D}$= 3.0 V)	P_{out}	31.5	32.4	–	dBm
Harmonic Output $2f_o$ $\geq 3f_o$		 – –	 –40 –35	 –35 –30	dBc
Input Return Loss	$\|S_{11}\|$	–	12	–	dB
Output Power Isolation with Buffer On (P_{in} = 5.0 dBm, $V_{D1B,D2B}$ = 3.6 V, $V_{D1D,D2D,D3D}$ = 0 V)	P_{on}	–	–8.0	–2.0	dBm
Output Power Isolation (P_{in} = 5.0 dBm, $V_{D1B,D2B}$ = 0 V, $V_{D1D,D2D,D3D}$ = 0 V)	P_{off}	–	–36	–	dBm
Noise Power in Rx Band 1805 to 1880 MHz (100 kHz measurement bandwidth)	NP	–	–85	–71	dBm
Negative Voltage (P_{in} = 5.0 dBm, $V_{D1B,D2B}$ = 3.0 V)	V_{SS}	–	–	–4.85	V
Negative Voltage Settling time (P_{in} = 5.0 dBm, $V_{D1B,D2B}$ stepped from 0 to 3.0 V)	T_S	–	0.7	2.0	µs
Stability–Spurious Output (P_{out} = 3.0 to 33 dBm, Load VSWR = 6:1 all Phase Angle, Source VSWR = 3:1, at any phase angle Adjust $V_{D1D,D2D,D3D}$ for specified power)	P_{spur}	–	–	–60	dBc

ELECTRICAL CHARACTERISTICS (continued) ($V_{D1B, D2B}$ = 3.6 V, $V_{D1G,D2G,D3G}$ = 3.6 V or $V_{D1D,D2D,D3D}$ = 3.6 V, Peak measurement at 12.5% duty cycle, 4.6 ms period, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DCS SECTION (continued) (P_{in} = 5.0 dBm)					
Load Mismatch Stress (P_{out} = 3.0 to 33 dBm, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust $V_{D1D,D2D,D3D}$ for specified power)		No Degradation in Output Power Before and After Test			
Positive Voltage (P_{in} = 5.0 dBm, V_{D1B} = V_{D2B} = 3.0 V)	V_P	6	10	–	V

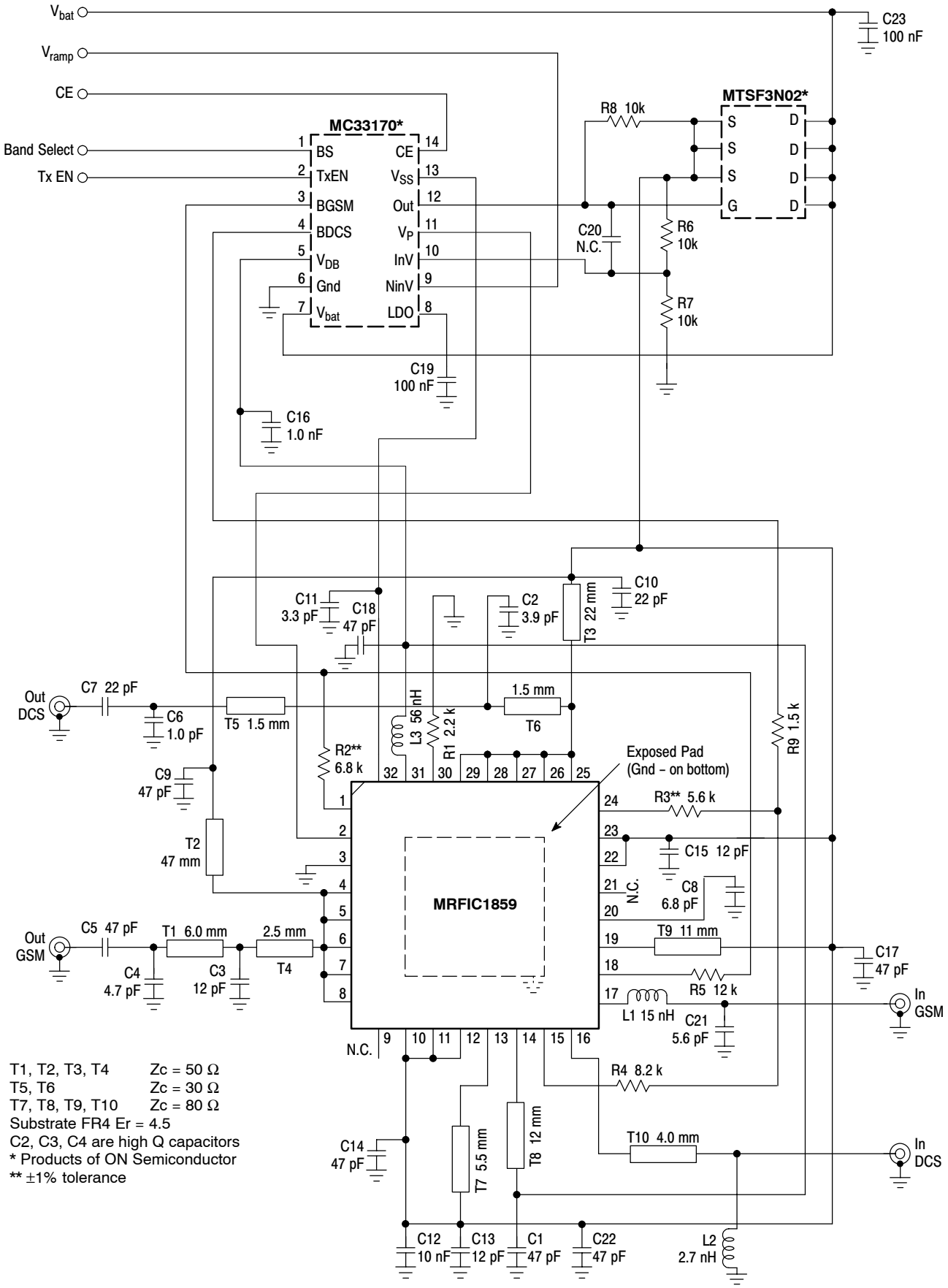
PIN FUNCTION DESCRIPTION

Pin No.	Symbol	I/O	Description	Functionality
1	B23G	I	GSM Bias for 2nd and 3rd stage	Bias pin of GSM second and third stages. Biasing circuit is made of an internal resistor connected to RF transistor gate, and in series with a current source, connected to V_{SS} (Pin 32). An external resistor allows to tune biasing point for best gain (Class AB). To switch off GSM line–up, setting this pin (and Pin 18) to high impedance, which will apply V_{SS} (–5.0 V) to the gates, i.e., a voltage two times lower than FET threshold voltage.
2	V_P	O	Positive voltage	A buffer amplifier is designed to produce the required negative voltage, based on RF signal amplification and rectification. Also a positive voltage is generated in the same way, with rectification and a voltage doubler. This voltage supplies an op amp in order to drive a NMOS as drain switch. Refer to application schematic, with MC33170 and MTSF3N02 (products of On Semiconductor).
3	Gnd		Ground	
4,5,6,7,8	OutG	O	GSM output	RF output and power supply for output GSM stage. Supply voltage is provided through those five pins. An external matching network is required to provide optimum load impedance.
9		N.C.		
10,11,12	D2G	I	GSM 2nd stage drain	Power supply for GSM second stage, and inter–stage matching. Wire bonds and pins form the required inductor for optimum inter–matching tuning. Make note that decoupling capacitor on those pins needs to be placed as close as possible to the pins. Refer to application schematic for component value.
13	D1D	I	DCS 1st stage drain	Power supply for DCS first stage, and inter–staging matching. This pin associated with a printed line (80 Ω) forms the required inductor for a proper match.
14	D1B	I	Buffer 1st stage drain	Power supply for buffer amplifier first stage, and inter–staging matching. This pin, associated with a printed line (80 Ω) forms the required inductor for a proper match.
15	B1D	I	DCS 1st stage Bias	Same function as Pin 18 for DCS amplifier.
16	InD	I	DCS RF Input	RF input for DCS amplifier. A series inductor or line and a parallel inductor are required for a proper matching to 50 Ω and maximum gain. See application circuit.
17	InG	I	GSM RF Input	RF input for GSM amplifier. An inductor and a capacitor are required for a proper matching to 50 Ω and maximum gain. See application circuit.
18	B1G	I	GSM 1st stage Bias	Bias pin of GSM first stage and associated buffer stage. Biasing circuit is made of an internal resistor connected to RF transistor gate, and in series with a current source, connected to V_{SS} (Pin 32). An external resistor allows to tune biasing point for best gain (Class AB). See comments on Pin 1.
19	D1G	I	GSM 1st stage drain	Power supply for GSM first stage, and inter–stage matching. This pin, associated with a printed line (80 Ω) form the required inductor for a proper match.
20	G2D	I	DCS 2nd stage gate	Access to DCS 2nd stage gate. A shunt capacitor connected to this pin contributes to the inter–stage matching between 1st and 2nd DCS stages.
21	V_{SC}	O	Check for Negative voltage	An opened drain transistor connected to this pin, with V_{SS} as gate voltage, gives a checking signal for negative voltage generation. Used in application circuit to forbid on state to the NMOS Drain switch when V_{SS} is not working. Prevents IC degradation when bias is not present. This pin is not used with MC33170 which has its own protection circuit.

PIN FUNCTION DESCRIPTION (continued)

Pin No.	Symbol	I/O	Description	Functionality
22,23	D2D	I	DCS 2nd stage drain	Power supply for DCS driver stage, and inter–staging matching. These pins form the required inductor for a proper match.
24	B23D	I	DCS Bias for 2nd and 3rd stage	Same as Pin 1 for DCS amplifier.
25,26,27, 28,29	OutD	O	DCS RF Output	RF output and power supply for output DCS stage. Supply voltage is provided through those five pins. An external matching network is required to provide optimum load impedance.
30	B2B	I	Buffer 2nd state Bias	Like Pins 1, 15, and 18, this is a bias pin. Pin 30 is used to bias 2nd stage of buffer amplifier.
31	D2B	I	Buffer 2nd stage Drain	Drain supply and matching of buffer amplifier to maximize V_{SS} and V_P voltages.
32	V_{SS}	O	Negative Voltage	A buffer amplifier is designed to produce the required negative voltage, based on RF signal amplification with a two stages wide band amplifier and rectification of the resulting signal. An external zener diode is used to regulate this voltage and provide to the gates a stabilized biasing voltage. V_{SS} is also used to switch off the unused amplifier. Refer to Bias Pins 1, 18 and 15, 24.
Exposed Pad	Gnd	I	Main Gnd	The bottom pad of the TQFP–32EP package is used for electrical/RF grounding and thermal dissipation. The PCB pattern where it fits has to be tailored for good ground and thermal continuity (with many ground via holes).

Figure 1. Application Schematic



T1, T2, T3, T4 Zc = 50 Ω
T5, T6 Zc = 30 Ω
T7, T8, T9, T10 Zc = 80 Ω
Substrate FR4 Er = 4.5
C2, C3, C4 are high Q capacitors
* Products of ON Semiconductor
** ±1% tolerance

GSM TYPICAL CHARACTERISTICS

Figure 2. Output Power versus Frequency

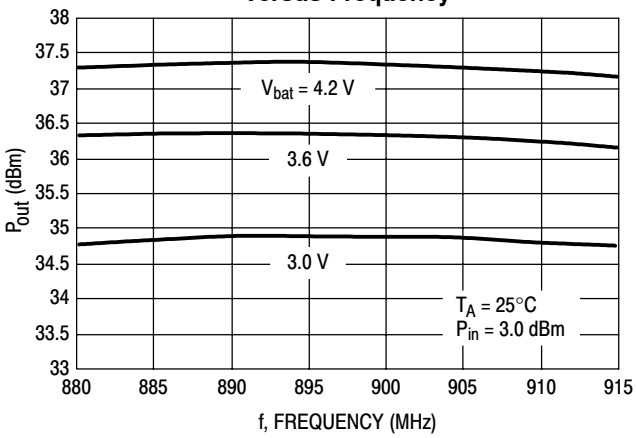


Figure 3. Power Added Efficiency versus Frequency

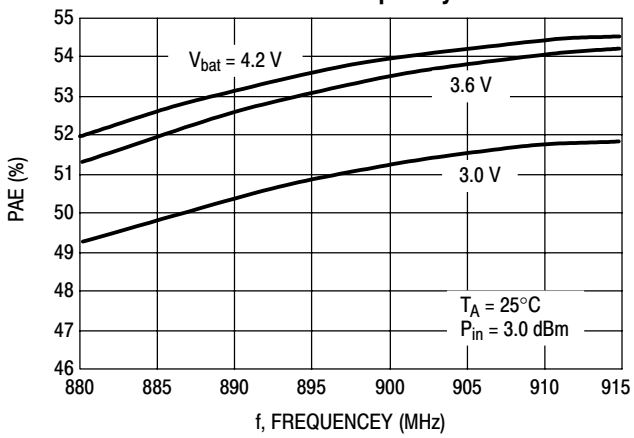


Figure 4. Output Power versus Frequency

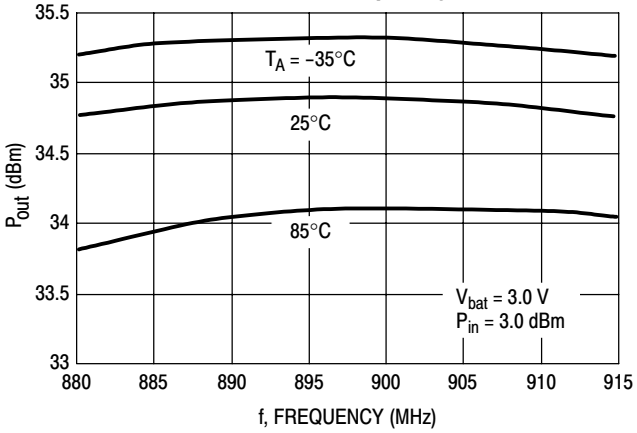


Figure 5. Output Power versus Frequency

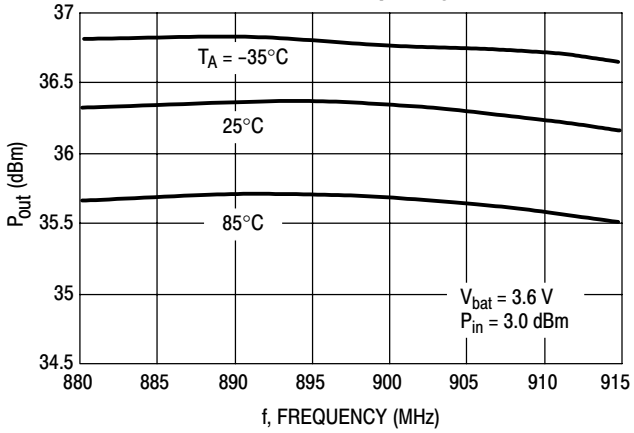


Figure 6. Output Power versus Frequency

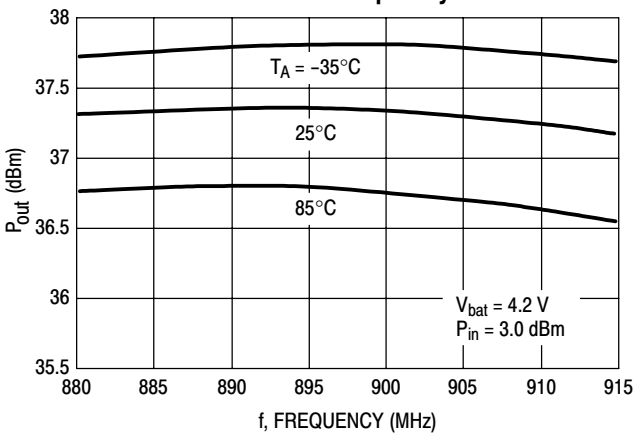


Figure 7. Power Added Efficiency versus Frequency

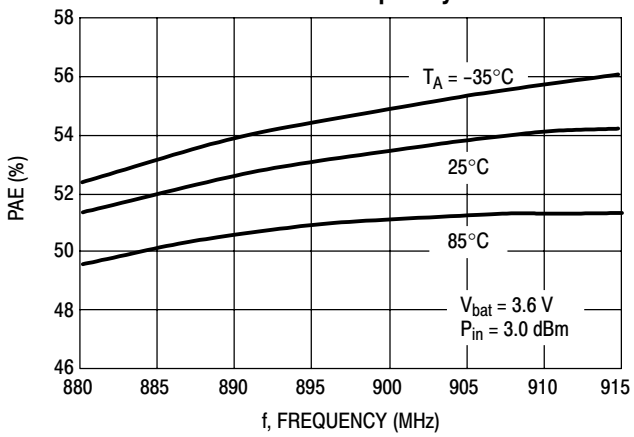


Figure 8. Second Harmonics versus Frequency

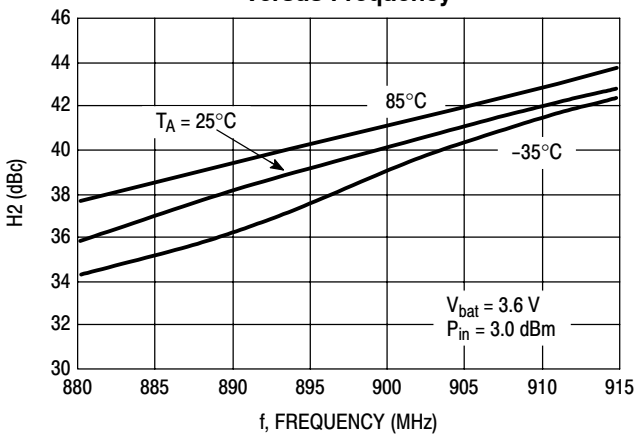


Figure 9. Third Harmonics versus Frequency

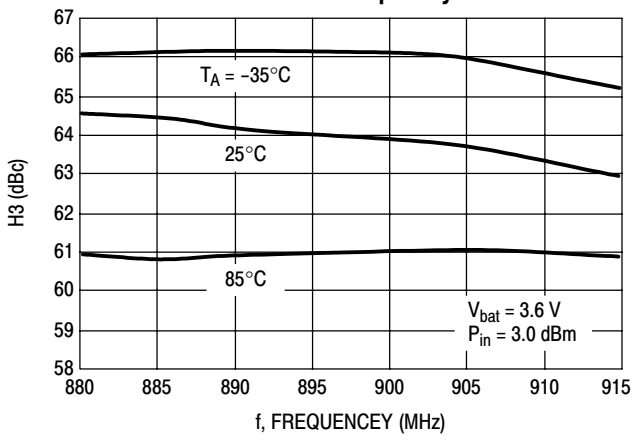


Figure 10. Positive Voltage Generator Output versus Frequency

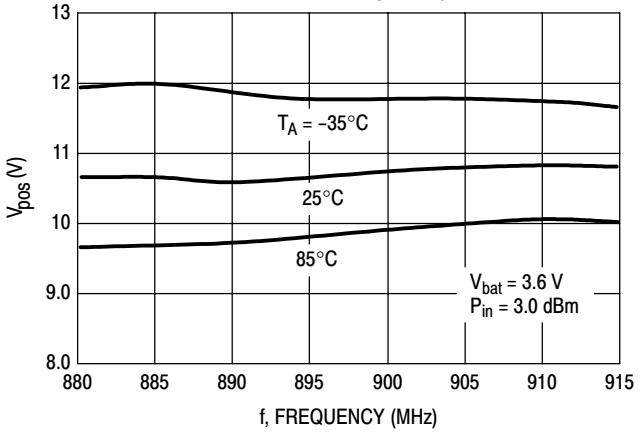


Figure 11. Crosstalk versus Frequency

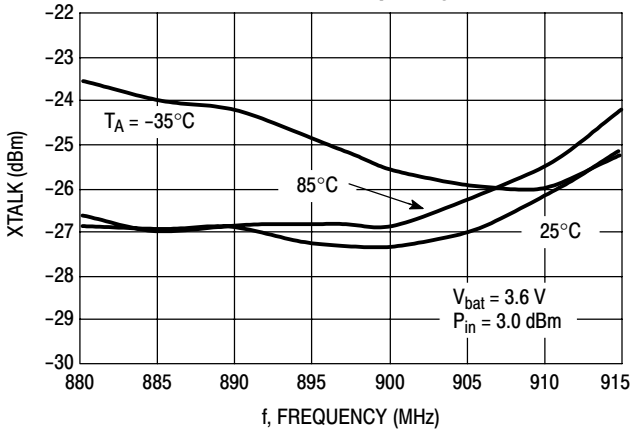


Figure 12. Output Power versus V_{ramp}

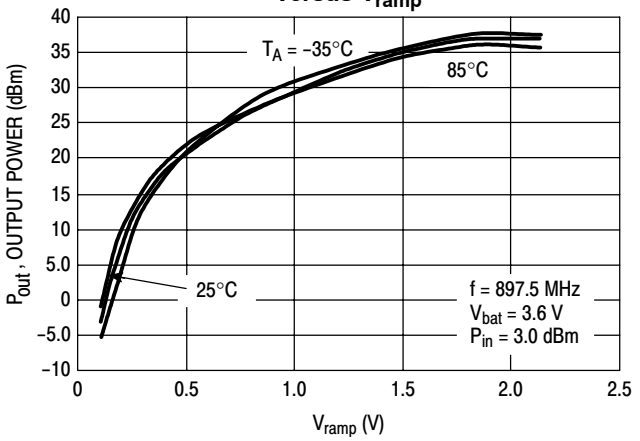
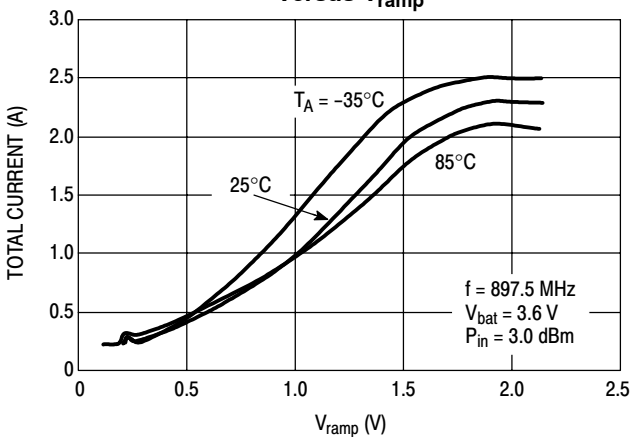


Figure 13. Total Current versus V_{ramp}



DCS TYPICAL CHARACTERISTICS

Figure 14. Output Power versus Frequency

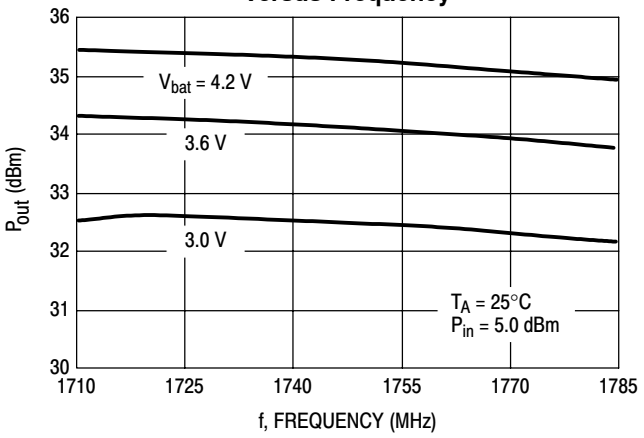


Figure 15. Power Added Efficiency versus Frequency

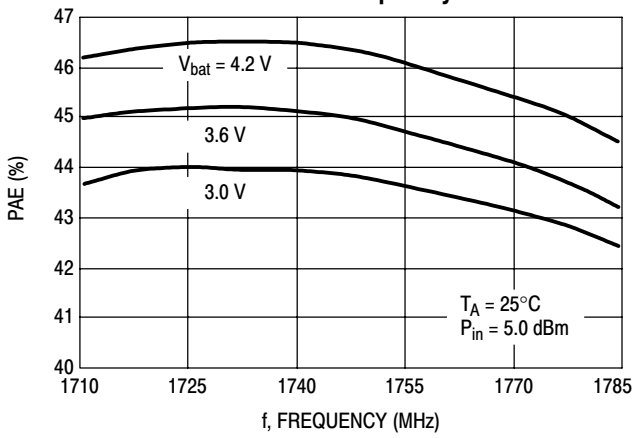


Figure 16. Output Power versus Frequency

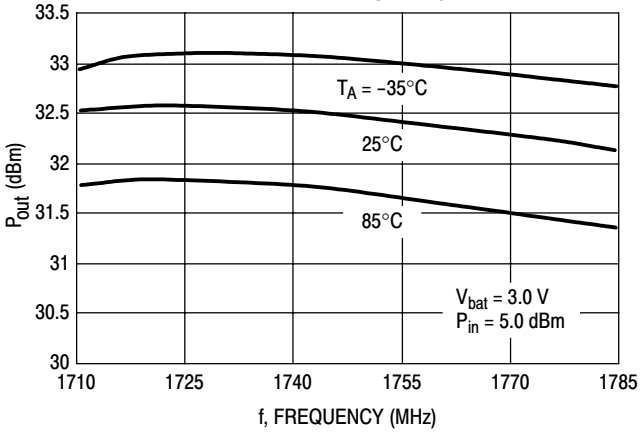


Figure 17. Output Power versus Frequency

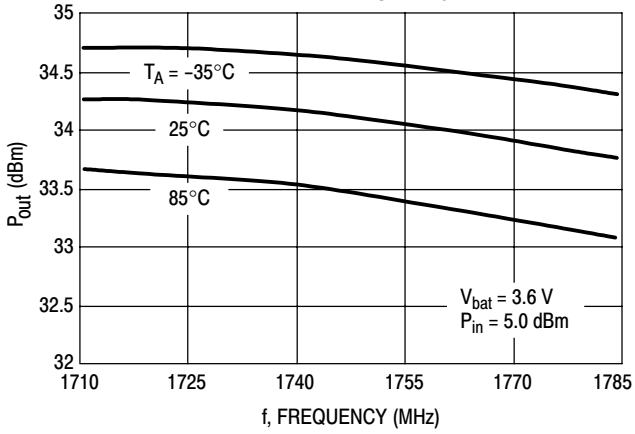


Figure 18. Output Power versus Frequency

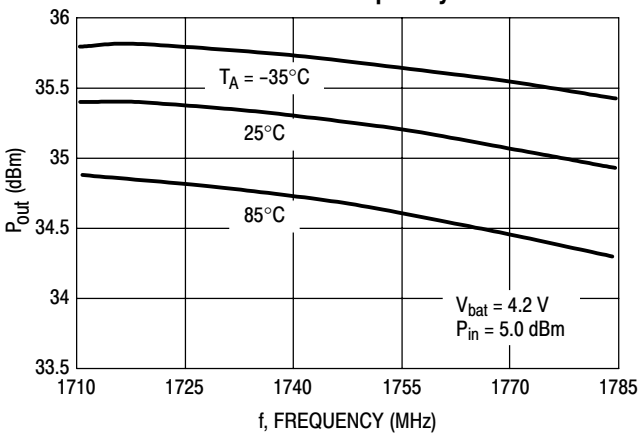
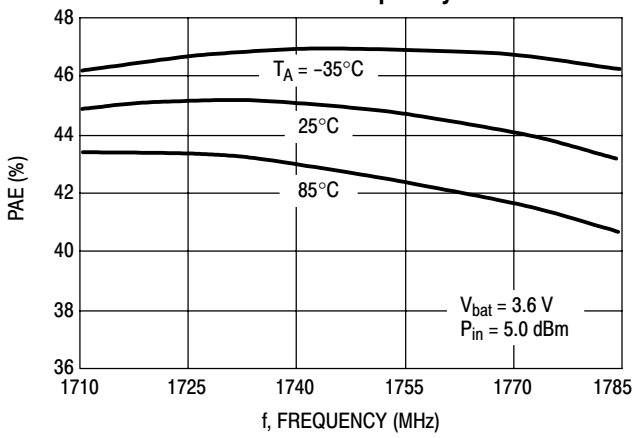


Figure 19. Power Added Efficiency versus Frequency



DCS TYPICAL CHARACTERISTICS

Figure 20. Second Harmonics versus Frequency

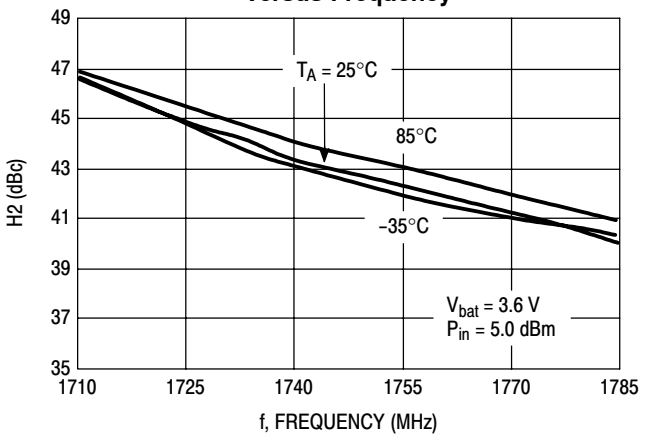


Figure 21. Third Harmonics versus Frequency

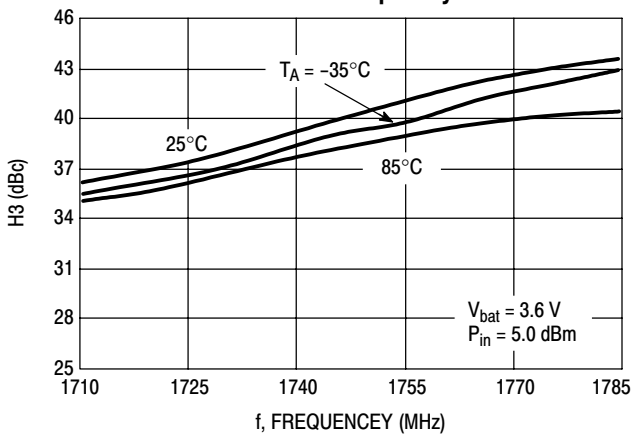


Figure 22. Positive Voltage Generator Output versus Frequency

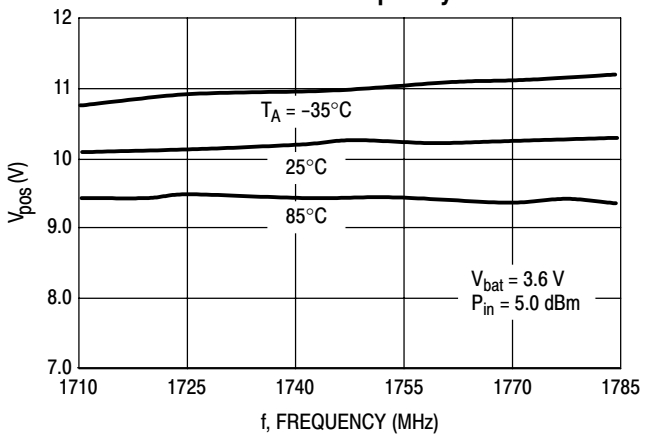


Figure 23. Output Power versus V_{ramp}

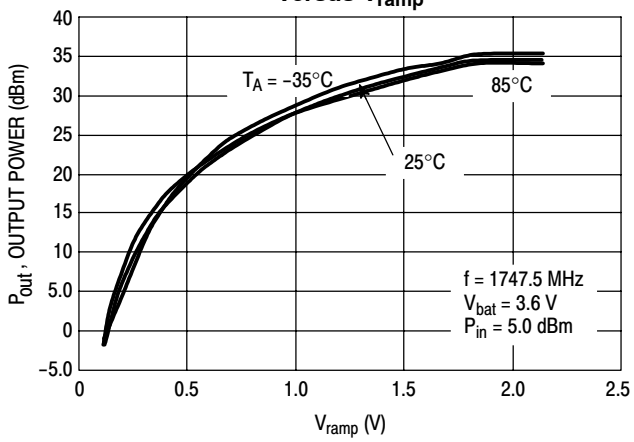
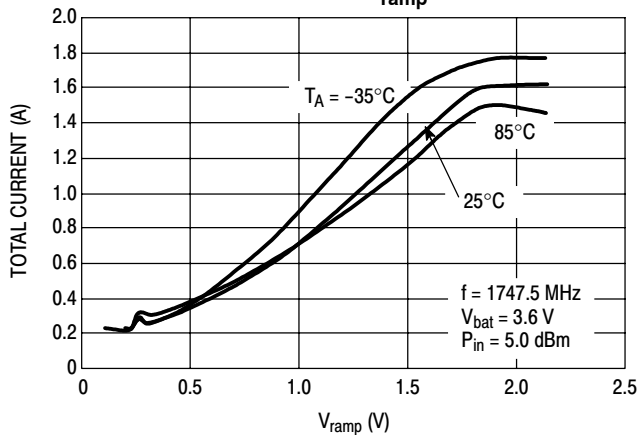


Figure 24. Total Current versus V_{ramp}



Design Philosophy

The MRFIC1859 is a dual–band single supply RF integrated power amplifier designed for use in GSM900/DCS1800 handheld radios under 3.6 V operation. With matching circuit modifications, it is also applicable for use in triple band GSM900/DCS1800/PCS1900 equipment. Typical performances in GSM/DCS at 3.6 V are: GSM: 35.8 dBm with 53% PAE and, DCS: 34 dBm with 43% PAE.

It features a large band (900 to 1800 MHz) internal Negative Voltage Generator based on RF rectification of the input carrier after its amplification by two dedicated buffer stages (See Simplified Block Diagram). This method eliminates spurs found on the output signal when using dc/dc converter type negative voltage generators, either on or off chip. The buffer generates also a step–up positive voltage, which can be used to drive a NMOS drain switch.

External Circuit Considerations

The MRFIC1859 can be tuned by changing the values and/or positions of the appropriate external components (see Figure 1: Application Schematic). While tuning the RF line–up, it is recommended to apply external negative supply in order to prevent any damage to the power amplifier stages. Poor tuning on the input may not provide enough RF power to operate the negative voltage generator properly.

Input matching is a shunt–C, series–L, low pass structure for GSM and a shunt–L, series–L high pass structure for DCS. It should be optimized at the rated input power (e.g. 3.0 dBm in GSM, 5.0 dBm in DCS). Since the input lines feed both 1st stages and 1st stage buffers, input matching should be iterated with buffer and Q1 drain matching. Note that dc blocking capacitors are included on chip.

First stage buffer amplifier is tuned with a short 80 Ω microstrip line which may be replaced by a chip inductor. Second stage buffer amplifier is supplied and matched through a discrete chip inductor. Those two elements are tuned to get the maximum output from voltage generator. The overall typical buffer current (DB1 + DB2) is about 60 mA in GSM and 100 mA in DCS. However, the negative generator needs a settling time of 1.0 µs (see burst mode paragraph). During this transient period of time, both stages are biased to IDSS, which is about 200 mA each.

The step–up positive voltage available at Pin 2, which is approximately 10 V in each band, can be used to drive a NMOS drain switch for best performances.

Q1 drains are supplied and matched through 80 Ω printed microstrip lines that could be replaced by discrete chip inductors as well. Their lengths (or equivalent inductor values) are tuned by sliding the RF decoupling capacitors along to get the maximum gain on the first stages.

Q2 drains are supplied through 60 Ω printed microstrip lines that contribute also to the interstage matching in order to optimum drive to the final stages.

The line length for Q2G and Q2D is small, so replacing it with discrete inductors is not practical.

Q3 stages are fed via 50 Ω printed microstrip lines that must handle the high supply current of that stages (2.0 Amp peak) without significant voltage drop. This line can be buried in an inner layer to save PCB space or be a discrete RF choke.

Output matching is accomplished in both bands with two stages low pass networks. Easy implementation is achieved with shunt capacitors mounted along a 50 Ω microstrip transmission line. Value and position are chosen to reach a load line of 2.0 Ω while conjugating the device output parasitics. The networks must also properly terminate the second and third harmonic level. Use of high–Q capacitors for the first output matching capacitor circuits is recommended in order to get the best output power and efficiency performances.

Note: the choice of output matching capacitor type and supplier will affect H2 and H3 level and efficiency, because of series resonant frequency.

Tuning Methodology

The following section gives the user some guidelines and hints to tune and optimize the MRFIC1859 operation inside their own radio PCB. First of all, one must keep in mind that negative and positive voltage generation is based on RF carrier rectification. This means that RF input signal must always be present when running the part as a standalone solution. Therefore, in order to ease the tuning phase, it is recommended to apply the negative voltage externally in order to avoid any damage to the large RF MESFET transistors. This is particularly true if one uses the complete application with MC33170 (product of On Semiconductor) as control IC to do the optimization. In that case, both negative and positive voltage should be provided externally.

The RF decoupling capacitors have been selected as 47 pF for GSM band (C17, C14, C22, C9. C1, and C8) and 22 pF or 12 pF for DCS band (C10, C15, and C13). But those can be optimized depending on their size and source, for example 12 pF were used at some places for DCS to provide better decoupling of the harmonics too, thus providing some extra performance.

The recommended tuning procedure consists of several steps that need to be performed in sequential order. Several iterations can be performed if appropriate. Due to low interaction between line–ups, each band can be tuned independently.

- Optimize the buffer operation using D1B (T8 line) and D2B matching (L3 inductor). Simultaneously, tune GSM or DCS input matching using L1, C21 or L2, T10, respectively. Check the margin on P_{in} to generate V_{SS} and V_P (those voltages should still meet their specification with a 5.0 dB reduction in P_{in}). A small shunt capacitor can be placed on V_P to maximize that voltage.
- Optimize RF line up linear gain using D1G, D2G matching (T9 line) or D1D, D2D, G2D matching (T7 line, C8) for GSM or DCS line–up, respectively. The goal is to maximize and center small signal gain. P_{in} has to be reduced for this exercise, hence the negative voltage needs to be applied externally. A broad band measurement is helpful to visualize the frequency response. Linear gain should peak at around 40 dB for GSM and 32 dB for DCS. The input matching has to be checked again and eventually refined during this step.
- Optimize output matching using T4, C3, T1, C4 and T2 for GSM or T6, C2, T5, C6, T3 for DCS, respectively. Those elements set the P_{out}/PAE trade–off and harmonics rejection performance.

- Finally, one can iterate some of the above steps to fine tune RF behavior and also to find the best configuration for Cross–Talk and Harmonics content reduction. For example, D2B inductor L3 and V_{SS} decoupling capacitor C11 have a small influence on the GSM second harmonic leaking through the DCS output.

The nominal impedance seen from the IPA package pins have been measured on the demoboard (after removing the MRFIC1859) and are listed in the following table. They can be taken as a starting point for the optimization. Also this gives the equivalent lumped element if one uses a lumped element instead of microstrip line.

Impedance on the different GSM I/Os: (expressed in Ω at 900 MHz)

– InG = 16.2 + j83.5
– OutG = 1.9 – j2.3
– D2G = close to 0 since decoupled as short as possible
– D1G = 1 + j19.8 (3.5 nH)
– D1B = 1.2 + j28.7 (5.0 nH)
– D2B = infinite since 56 nH behaves as choke

Impedance on the different DCS I/Os: (expressed in Ω at 1750 MHz)

– InD = 12.5 + j36.5
– OutD = 3.6 – j4.4
– D2D = close to 0 since decoupled as short as possible
– G2D = 0.9 + j6.8 (0.64 nH)
– D1D = 1.1 + j20.8 (1.9 nH)
– D1B = 8.8 + j84.7 (7.6 nH)
– D2B = infinite since 56 nH behaves as choke

One should note that except for RF_{in}/RF_{out} impedance, all others should be "in theory" pure reactive shunt elements. The fact that their resistive part is not zero is linked to the finite quality factor of the equivalent inductor and also to the limited accuracy of the measurement (when close to the Smith chart border).

Control Considerations

The MRFIC1859 application uses drain control technique developed for our generations of GaAs IPAs. This method relies on the fact that for an RF power amplifier operating in saturation mode, the RF output power is proportional to the square of the Amplifier drain voltage: P_{out} (Watt) = k * V_D (V) * V_D (V).

A dedicated control IC MC33170 has been designed to manage all those control, biasing and band selection functions. When the emitting order is sent (TxEn = High), the MC33170 activates the power supply V_{Dbuf} of the negative voltage generator NVG (V_{Dbuf} = V_{bat}), involving the presence of V_{neg} as well as a positive V_P of about 9.0 V. Once V_{neg} detected and regulated at –5.0 V, the MC33170 enables a N–channel MOSFET to be driven.

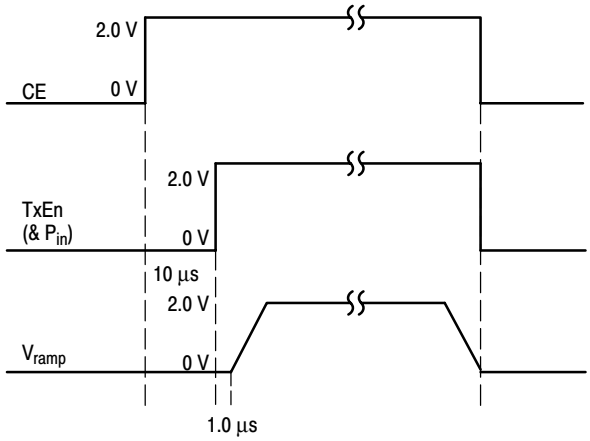
The NMOS is used as a ballast transistor whose drain–source resistance is controlled by V_{ramp}. This allows to supply the PA with a voltage from 0 V (V_{ramp} = 0 V) to V_{bat} (V_{ramp} = 2.0 V) and hence to control the output power. Such a way of control provides an excellent predictability of the RF output power (since the output voltage is proportional to the drain voltage) and eliminates the need for a power or current detection loop.

The band selection is achieved by setting the BS pin of the MC33170 to 0 V (GSM) or 1.0 V (DCS), hence biasing the GSM or DCS transistors through BiasGSM and BiasDCS pins.

Burst Mode

In order to perform burst mode measurements, the following time can be used as a guideline.

Figure 25.



– First the MC33170 must be awaken through CE to activate its Low Drop Out Regulator. The BS pin has also to be set according to the selected frequency band.
– Then TxEn is set high which supply the buffer stages and activates the Negative and Positive Voltage Generation. TxEn signal can be used to switch the input power (using a driver or attenuator) in order to provide higher isolation for on/off burst dynamic.
– V_{ramp} (Pin 1) can be applied soon after TxEn since the internal negative voltage generator settles in less than 1.0 µs.

References (Motorola Application Notes)

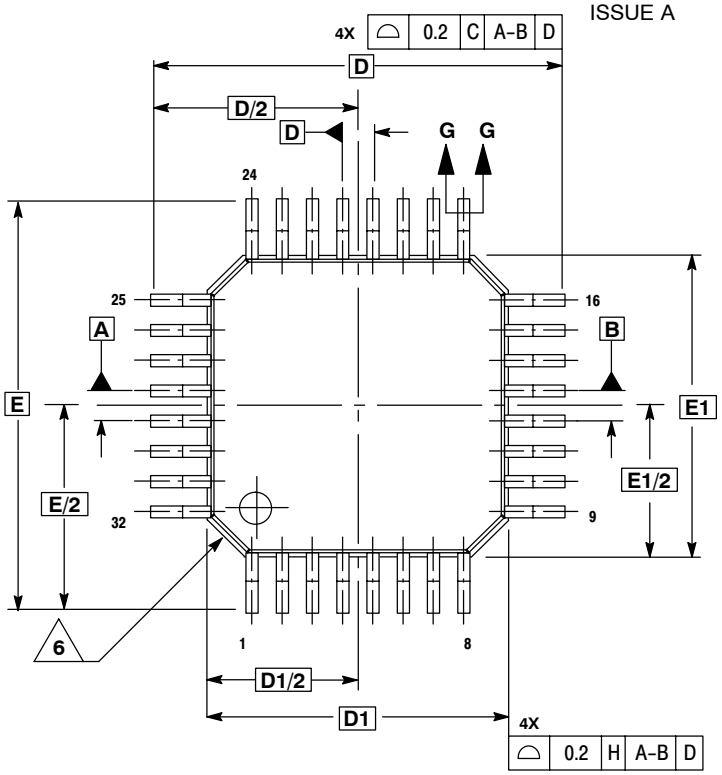
AN1599 – Power Control with the MRFIC0913 GaAs Integrated Power Amplifier and MC33169 Support IC.
AN1697 – GSM900/DCS1800 Dual–Band 3.6 V Power Amplifier Solution with Open Loop Control Scheme.

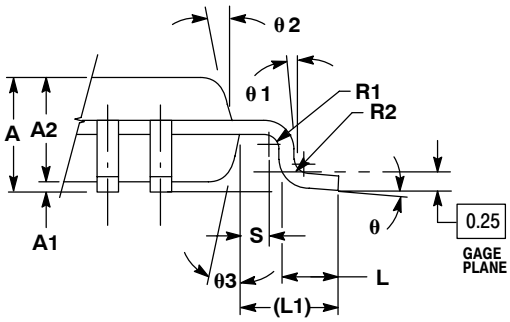
NOTES

NOTES

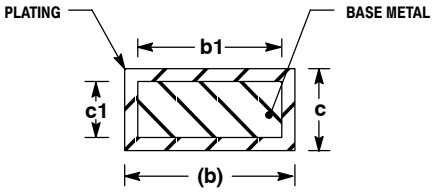
OUTLINE DIMENSIONS

PLASTIC PACKAGE
CASE 873E–02
(TQFP–32EP)
ISSUE A

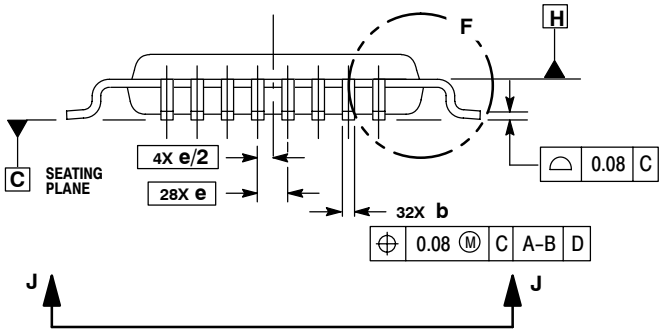




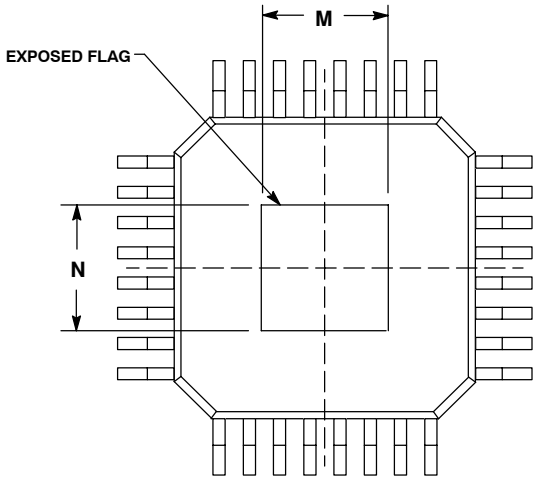
DETAIL F



SECTION G–G



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25–MM PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08–MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN A PROTRUSION AND ADJACENT LEAD IS 0.07–MM
6. EXACT SHAPE OF CORNERS IS OPTIONAL.



VIEW J–J

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.13
A1	0.039	0.089
A2	0.95	1.05
b	0.17	0.27
b1	0.17	0.23
C	0.09	0.2
C1	0.09	0.16
D	7 BSC	
D1	5 BSC	
e	0.5 BSC	
E	7 BSC	
E1	5 BSC	
L	0.45	0.75
L1	1 REF	
M	2.09	2.19
N	2.09	2.19
R1	0.08	---
R2	0.08	0.2
S	0.2	---
θ	0°	7°
θ1	0°	---
θ2	11°	13°
θ3	11°	13°

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