Preliminary

OKI semiconductor

MSC6458

OKI 4-BIT 1-CHIP MICROCONTROLLER

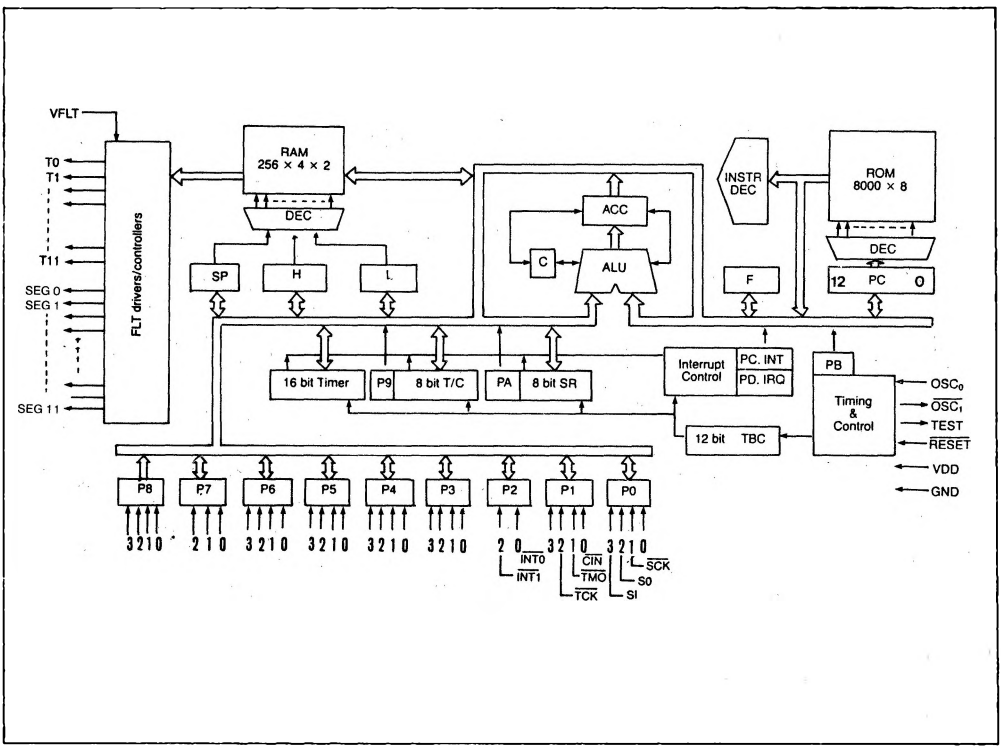
GENERAL DESCRIPTION

The MSC6458 is a high-speed, 4-bit 1-chip microcontroller with built-in FLT drivers/controllers developed to support relatively large control systems.

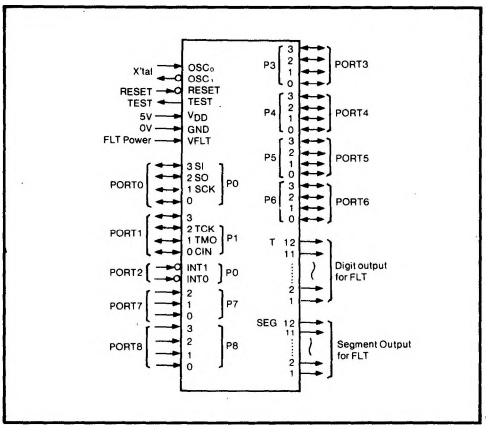
FEATURES

- ROM: 8000 × 8 bits
- RAM: 512 × 4 bits
- Ports: I/O 24 ports (8 having IOL = 20 mA)
  Input 9 (2 also serving as interrupt inputs)
- FLT drivers (Withstand voltage 40V): 12 (IOH = 20mA)
  12 (IOH = 6mA)
- Interrupts: 7 lines (2 external, 5 internal)
- Built-in counters: 12 bits, timebase counter
  16 bits, programmable counter
  8 bits, high-speed programmable timer/event counter
- Serial I/O: Built-in 8-bit SIO register
- Oscillation circuit: Crystal or ceramic oscillation
- Number of instructions: 147
- Cycle time: 930 ns (4.3MHz)
- Operating ranges: 4.5 to 5.5V (4.3MHz)
  Voltage: 3.0 to 6.0V (1MHz)
  Temperature: −40 to +85°C
- Power dissipation (typical)
  (display off): 9mA (5V, 4.3MHz)
  2mA (3V, 1MHz)
- Power down: STOP instruction
- Package: 64-pin shrink DIP/64-pin FLAT

BLOCK DIAGRAM

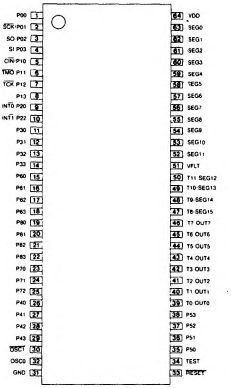


LOGIC SYMBOL



PIN CONFIGURATION (TOP VIEW)

64 PIN PLASTIC SHRINK DIP



PIN DESCRIPTION

Terminal	Input/ Output	Function	When reset
P00 P01/$\overline{SCK}$ P02/SO P03/SI	Input/ Output	I/O port I/O port (also used as serial clock input $\overline{SCK}$) I/O port (also used as serial data output SO) I/O port (also serial data input SI)	"1"
P10/$\overline{CIN}$ P11/$\overline{TMO}$ P12/$\overline{TCK}$ P13	Input/ Output	I/O port (also used as count input $\overline{CIN}$) I/O port (also used as timer output $\overline{TMO}$) I/O port (also used timer clock input $\overline{TCK}$) I/O port	"1"
P20/$\overline{INT0}$ P22/$\overline{INT1}$	Input	Input Port with Latch (falling edge sensitive) also used as interrupt input $\overline{INT0}$ Input Port with Latch ('0' level sensitive) also used as interrupt input $\overline{INT1}$	–
P30 ~ P33	Input/ Output	I/O port	"1"
P60 ~ P63	Input/ Output	I/O port	"0"
P40 ~ P43 P50 ~ P53	Output/ Input	I/O port (I_{OL}=20mA MAX)	"0"
P70 ~ P72 P80 ~ P83	Input	Input port with pull down register Pull down register of P70 ~ P72 can be removed by instruction	
SEG0 ~ SEG11	Output	FLT segment driver (dynamic)	"0"
T11/SEG12 ~ T8/SEG15	Output	FLT segment driver (dynamic)/Timing output	"0"
T7/OUT7 ~ T0/OUT0	Output	FLT segment driver (static)/Timing output	"0"
$\overline{OSC0}$ $\overline{OSC1}$	Input/ Output	Crystal connection terminal for system clock oscillation	–
$\overline{RESET}$	Input	System reset input	–
TEST	Output	Test pin (Open)	–
VFLT	Input	Power supply for FLT driving	–
VDD GND	Input	System Power Supply	–

FUNCTIONAL DESCRIPTION

1. ROM

The ROM, organized in 8 bits, has a maximum capacity of 8000 bytes.

2. RAM

The RAM is organized in 4 bits per word, with a capacity of 512 words.

It is separated into two banks each 256 words long. Bank selection is accomplished via internal ports. The RAM location in the banks is addressed by the H and L registers or by the second byte of each instruction.

3. Ports (24 I/O, 7 input)

The 24 pseudo-bidirectional I/O ports effect or control the exchange of data with external sources. The ports are specified by the L register or by codes contained in instructions. Ports 4 and 5 may draw IOL up to 20mA.

The seven input ports have built-in pulldown resistors. Up to 84 keys can be scanned by assembling them in key matrices with the timing outputs of the FLT drivers (with 12 segments × 12 timings on display; also during automatic display).

4. Interrupt Input Pins (2 terminals)

The $\overline{INT0}$/P20 and $\overline{INT1}$/P22 pins are interrupt input pins. External interrupt request flags of $\overline{INT0}$/P20 pin and $\overline{INT1}$/P22 pin can be set by using interrupt input pins:

$\overline{INT0}$/P20 pin ... positive edge or negative edge input.

$\overline{INT1}$/P22 pin ... "0" level input.

These flags are automatically reset when the appropriate external interrupts occur. These pins are available for use as input ports when not used as interrupt input pins.

5. FLT Drivers/Controllers (Automatic Display)

The FLT drivers have a withstand voltage of 40V in the positive direction from the GND level. They comprise 12 ports that can draw 20mA as IOH (Timing outputs) and 12 ports that can draw 6mA as such (Segment outputs).

A choice of four display modes is supported as listed below. A display RAM area is allocated as part of the RAM space. Data is automatically displayed when transferred to the display RAM. (Two different display frequencies are selectable.) Static output data can be displayed by controlling the FLT drivers by programming.

Display modes (@4.194304 MHz)

(1) 12 Segments × 12 Timings
1/12 duty (85.3/341.3 Hz)

(2) 16 Segments × 8 Timings
1/8 duty (128/512 Hz)

(3) 16 Segments × 4 Timings +4 output*
1/4 duty (256/1024Hz)

(4) 16 Segments+8 output*
Program controlled

*output: static outputs

6. Stack (STACK) and Stack Pointer (SP)

The PC is saved in the stack when an interrupt occurs or a CAL instruction is executed. It is recovered by the execution of an RT instruction.

One fourth of the RAM space (128 words maximum, 32 levels) is available as a stack area. A 4-word RAM area is used for "one" level in the stack.

The stack pointer is an 8-bit up-down counter (the MSB and 2 bits from LSB being fixed at '1') indicating the next stack address to use. It enables the RAM space to be used as a pushdown stack. Data can also be transferred between stack pointer and the H/L registers.

7. Interrupts

Seven interrupt lines are provided for eight sources and eight levels of interrupts as follows (two external inputs):

(1) Display interrupt
Update to timing signals (positive edge)

(2) External interrupt1
Negative edge on the $\overline{INT0}$/P20 pin

(3) External interrupt2
Positive edge on the $\overline{INT0}$/P20 pin

(4) External interrupt3
'0' input on the $\overline{INT1}$/P22 pin

(5) Timebase interrupt
12-Bit timebase counter overflow

(6) Timer interrupt
16-Bit timer and timer register matched signal

(7) Counter interrupt
8-Bit counter and counter register matched signal

(8) Serial/O interrupt
8-Bit shift register shift end signal

8. 12-Bit Timebase Counter

The timebase counter is made up of a 12-bit binary counter. It generates an interrupt request every time it overflows as a result of dividing the OSC0 input 2^{12}.

9. 16-Bit Programmable Timer/Event Counter

Comprising a 16-bit register, a 16-bit binary counter, a comparator circiut, and a control circuit, the programmable timer generates an interrupt request when the register and counter values are matched.

10. 8-Bit High-Speed Programmable Timmer/Event Counter

The high-speed programmable timer/event counter comprises an 8-bit register, an 8-bit binary counter, a comparator circuit, and a control circuit. Starting and stopping the counter can be controlled by instructions. It generates an interrupt request when the register and counter values are matched.

11. 8-Bit Serial I/O

Serial I/O consists of an 8-bit shift register, a 3-bit shift counter, and a control circuit. It is used for serial data input and output. Serial data input and output takes place synchronized with a shift clock, which is selectable between internal and external clocks. The shift counter automatically terminates a data transfer on counting eight shift clock pulses and generates an interrupt request.

12. Registers (Acc, H, L, F)

The accumulator (Acc) is a 4-bit register used to perform data transfers or calculations with the RAM, other registers, ports and so on.

The H and L registers are each a 4-bit register. They transfer data to and from Acc and SP (stack pointer) and address the RAM. The L register is also used to specify ports to use.

The F register is made up of four independent flip-flops. It can be used as a program "flag" or general-purpose register because each of these flip-flops permits set/reset testing and transferring 4-bit parallel data to and from Acc by instructions.

13. Timing Control (TC)

A '0' input on the $\overline{\text{RESET}}$ pin for a certain period initializes internal circuitry and ports.

As the input side of clock pulses, the OSC0 pin accepts clock pulses from an external source. Clock pulses may also be obtained by configuring an oscillation circuit with a crystal oscillator or ceramic resonator connected to OSC0 and $\overline{\text{OSC1}}$.

Load Instructions, etc.

Mnemonic		Code	Bytes	Cycles	Description
LAI	n	90–9F	1	1	A ← n
LLI	n	80–8F	1	1	L ← n
LHI	n	3E · 7n	2	2	H ← n
LHLI	nn	15 · nn	2	2	HL ← nn
LMI	nn	14 · nn	2	2	M (w) ← nn
LAL		21	1	1	A ← L
LLA		2D	1	1	L ← A
LAH		22	1	1	A ← H
LHA		2E	1	1	H ← A
LAM		38	1	1	A ← M
LMA		2F	1	1	M ← A
LAM+		24	1	1	A ← M, L ← L+1, Skip if L = "0"
LAM−		25	1	1	A ← M, L ← L−1, Skip if L = "F"
LMA+		26	1	1	M ← A, L ← L+1, Skip if L = "0"
LMA−		27	1	1	M ← A, L ← L−1, Skip if L = "F"
LAMM	n2	39–3B	1	1	A ← M, H ← H ⩛ n2
LAMD	mm	10 · mm	2	2	A ← Md
LMAD	mm	11 · mm	2	2	Md ← A
X		28	1	1	A ⟷ M
X+		3C	1	1	A ⟷ M, L ← L+1, Skip if L = "0"
X−		2C	1	1	A ⟷ M, L ← L−1, Skip if L = "F"
XM	n2	29–2B	1	1	A ⟷ M, H ← H ⩛ n2
LMT	mm	19 · mm	2	4	M (w) ← T (Md (w), A)
LAF		3E · 54	2	2	A ← F
LFA		3E · 5C	2	2	F ← A
LHLS		3E · 53	2	2	HL ← SP
LSHL		3E · 5B	2	2	SP ← HL
IP		20	1	1	A ← P
OP		23	1	1	P ← A
IPD	p	3D · pD	2	2	A ← Pp
OPD	p	3D · pC	2	2	Pp ← A
OPT		18	1	3	P4, P5 ← T (M (w), A)

Interrupt Control Instructions

Mnemonic	Code	Bytes	Cycles	Description
MEI	3E · 60	2	2	MEIF ← "1"
MDI	3E · 61	2	2	MEIF ← "0"
EIXD	3D · E8	2	2	EIXDF ← "1"
EIXU	3D · E9	2	2	EIXUF ← "1"
EIXL	3D · EA	2	2	EIXLF ← "1"
EIDP	3D · EB	2	2	EIDPF ← "1"
EITB	3D · D8	2	2	EITBF ← "1"
EITM	3D · D9	2	2	EITMF ← "1"
EICT	3D · DA	2	2	EICTF ← "1"
EISR	3D · DB	2	2	EISRF ← "1"
DIXD	3D · E4	2	2	EIXDF ← "0"
DIXU	3D · E5	2	2	EIXUF ← "0"
DIXL	3D · E6	2	2	EIXLF ← "0"
DIDP	3D · E7	2	2	EIDPF ← "0"
DITB	3D · D4	2	2	EITBF ← "0"
DITM	3D · D5	2	2	EITMF ← "0"
DICT	3D · D6	2	2	EICTF ← "0"
DISR	3D · D7	2	2	EISRF ← "0"
TIXD	3D · E0	2	2	Skip if EIXDF = "1"
TIXU	3D · E1	2	2	Skip if EIXUF = "1"
TIXL	3D · E2	2	2	Skip if EIXLF = "1"
TIDP	3D · E3	2	2	Skip if EIDPF = "1"
TITB	3D · D0	2	2	Skip if EITBF = "1"
TITM	3D · D1	2	2	Skip if EITMF = "1"
TICT	3D · D2	2	2	Skip if EICTF = "1"
TISR	3D · D3	2	2	Skip if EISRF = "1"
TQXD	3D · 20	2	2	Skip if IRQXDF = "1"
TQXU	3D · 21	2	2	Skip if IRQXUF = "1"
TQXL	3D · 22	2	2	Skip if IRQXLF = "1"
TQDP	3D · 23	2	2	Skip if IRQDPF = "1"
TQTB	3D · C0	2	2	Skip if IRQTBF = "1"
TQTM	3D · C1	2	2	Skip if IRQTMF = "1"
TQCT	3D · C2	2	2	Skip if IRQCTF = "1"
TQSR	3D · C3	2	2	Skip if IRQSRF = "1"
RQXD	3D · 24	2	2	IRQXDF ← "0"
RQXU	3D · 25	2	2	IRQXUF ← "0"
RQXL	3D · 26	2	2	IRQXLF ← "0"
RQDP	3D · 27	2	2	IRQDPF ← "0"
RQTB	3D · C4	2	2	IRQTBF ← "0"
RQTM	3D · C5	2	2	IRQTMF ← "0"
RQCT	3D · C6	2	2	IRQCTF ← "0"
RQSR	3D · C7	2	2	IRQSRF ← "0"

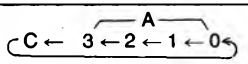
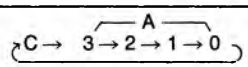
Increment/Decrement Instructions

Mnemonic		Code	Bytes	Cycles	Description
INA		30	1	1	A ← A+1, Skip if A = "0"
INL		31	1	1	L ← L+1, Skip if L = "0"
INH		32	1	1	H ← H+1, Skip if H = "0"
INM		33	1	1	M ← M+1, Skip if M = "0"
DCA		34	1	1	A ← A−1, Skip if A = "F"
DCL		35	1	1	L ← L−1, Skip if L = "F"
DCH		36	1	1	H ← H−1, Skip if H = "F"
DCM		37	1	1	M ← M−1, Skip if M = "F"
INMD	mm	12 · mm	2	2	Md ← Md+1, Skip if Md = "0"
DCMD	mm	13 · mm	2	2	Md ← Md−1, Skip if Md = "F"

Bit Handling Instructions, etc.

Mnemonic		Code	Bytes	Cycles	Description
TAB	n2	54−57	1	1	Skip if A (n2) = "1"
RAB	n2	64−67	1	1	A (n2) ← "0"
SAB	n2	74−77	1	1	A (n2) ← "1"
TPB	n2	50−53	1	1	Skip if P (n2) = "1"
RPB	n2	60−63	1	1	P (n2) ← "0"
SPB	n2	70−73	1	1	P (n2) ← "1"
TMB	n2	58−5B	1	1	Skip if M (n2) = "1"
RMB	n2	68−6B	1	1	M (n2) ← "0"
SMB	n2	78−7B	1	1	M (n2) ← "1"
TFB	n2	5C−5F	1	1	Skip if F (n2) = "1"
RFB	n2	6C−6F	1	1	F (n2) ← "0"
SFB	n2	7C−7F	1	1	F (n2) ← "1"
TPBD	p, n2	3D · p0~3	2	2	Skip if Pp (n2) = "1"
RPBD	p, n2	3D · p4~7	2	2	Pp (n2) ← "0"
SPBD	p, n2	3D · p8~B	2	2	Pp (n2) ← "1"
TC		09	1	1	Skip if C = "1"
RC		08	1	1	C ← "0"
SC		07	1	1	C ← "1"

Arithmetic Instructions

Mnemonic		Code	Bytes	Cycles	Description
ADCS		01	1	1	C, A ← C+A+M, Skip if C = "1"
ADS		02	1	1	A ← A+M, Skip if Cy = "1"
ADC		03	1	1	C, A ← C+A+M
AIS	n	3E · 4n	2	2	A ← A+n, Skip if Cy = "1"
DAA		06	1	1	A ← A+6
DAS		0A	1	1	A ← A+10
AND		0D	1	1	A ← A ∧ M
OR		05	1	1	A ← A ∨ M
EOR		04	1	1	A ← A ⊻ M
CMA		0B	1	1	A ← $\overline{A}$
CIA		0C	1	1	A ← $\overline{A}$+1
RAL		0E	1	1	
RAR		0F	1	1	
CAM		16	1	1	Skip if A = M
CAI	n	3E · 0n	2	2	Skip if A = n
CMI	n	3E · 1n	2	2	Skip if M = n
CLI	n	3E · 2n	2	2	Skip if L = n
CPI	p, n	17 · pn	2	2	Skip if Pp = n

Branch Instructions, etc.

Mnemonic		Code	Bytes	Cycles	Description
JCP	a6	C0–FF	1	1	PC ← a6
JA		1A	1	2	PC ← (PC ← A) +1
JM		1B	1	2	PC ← (M (w), A)
JP	a12	40–4F 00–FF	2	2	PC ← a12
CAL	a12	A0–AF 00–FF	2	4	ST ← PC+2, PC ← a12, SP ← SP–4
CZP	a	Ba	1	4	ST ← PC+1, PC ← 2a, SP ← SP–4
LJP	a13	3F 3F 00–1F 00 FF	3	4	PC ← a13
LCAL	a13	3F 3F 80–9F 00 FF	3	4	ST ← PC+3, PC ← a13, SP ← SP–4
RT		1E	1	4	PC ← ST, SP ← SP+4
RTS		1F	1	4	PC ← ST, SP ← SP+4, then Skip

Counter Control Instructions, etc.

Mnemonic	Code	Bytes	Cycles	Description
LCTM	3E · 51	2	2	CTR ← M (w)
LMCT	3E · 59	2	2	M (w) ← CT
ECT	3D · BB	2	2	CTF ← "1" (Counter Start)
DCT	3D · B7	2	2	CTF ← "0" (Counter Stop)
TCT	3D · B3	2	2	Skip if CTF = "1"
LTMM	3E · 50	2	3	TMR ← M (2w)
LMTM	3E · 58	2	3	M (2w) ← TM
LSRM	3E · 52	2	2	SR ← M (w), SC ← "0" SC: Shift Counter
LMSR	3E · 5A	2	2	M (w) ← SR
ESR	3D · BA	2	2	SRF ← "1" (Shift Register Start)
DSR	3D · B6	2	2	SRF ← "0" (Shift Register Stop)
TSR	3D · B2	2	2	Skip if SRF = "1"

CPU Control Instructions, etc.

Mnemonic	Code	Bytes	Cycles	Description
PUSH	1C	1	3	ST ← C, A, H, L, SP ← SP−4
POP	1D	1	3	C, A, H, L ← ST, SP ← SP+4
HALT	3D · B8	2	2	Halt CPU
STOP	3D · B9	2	2	Stop CPU
NOP	00	1	1	No Operation

Explanations of Instruction Symbols

A	: Accumulator (4-bit)
H	: H register (4-bit)
L	: L register (4-bit)
F	: F register (4-bit)
M	: RAM word addressed by the H and L registers
Md	: RAM word addressed by second byte of an instruction code
M (w)	: Two RAM words addressed by the H and L register/H3-0 and L3-1 (8-bit)
Md (w)	: Two RAM words addressed by second byte of an instruction code (8-bit)
M (2w)	: Four RAM words addressed by the H and L register/H3-0 and L3-2 (16-bit)
ST	: Four RAM words (16-bit) allocated as a stack area
SP	: Stack pointer (8-bit)
PC	: Program counter
P	: Port specified by the L register (4-bit)
Pp	: Port specified by 4 high-order bits of second byte of an instruction code (4-bit)
CTR	: 8-Bit counter/register
CT	: 8-Bit programmable counter
CTF	: Programmable counter start flag
TMR	: 16-Bit timer/register
TM	: 16-Bit programmable timer
SR	: 8-Bit shift register
SRF	: Shift register start flag
(X, Y)	: ROM address data specified by a11-4 as X and a3-0 as Y (12-bit)
T (X, Y)	: ROM table data specified by a11-4 as X and a3-0 as Y (8-bit)
n	: Immediate data (4-bit)
nn	: Immediate data (8-bit)
n2	: Two low-order bits of an instruction code
(n2)	: Bit specified by the two low-order bits of an instruction code
a	: ROM address data
aX	: ROM address data (X-bit)
mm	: RAM address data (8-bit)
C	: Carry flag
Cy	: Flag indicating a carry in a calculation result