OKI semiconductor

MSM5128-20GSK

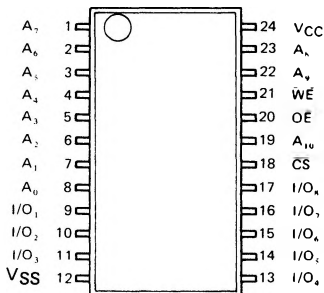## 2048-WORD x 8-BIT C-MOS STATIC RAM (E3-S-013-32)

GENERAL DESCRIPTION

The MSM5128GS is a 2048-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM5128GS is also a CMOS silicon gate device which requires very little power during standby (maximum standby current of $50\mu A$) when there is no chip selection. Stored data is retained if the power voltage drops to 2V, thereby enabling battery back-up.

A byte system is adopted, and since there is pin compatibility with standard ultra-violet EPROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, $\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

- Single 5V Supply
- Battery Back-up at 2V
- Operating temperature range Ta = $-40°C$ to $+85°C$
- Low Power Dissipation

  Standby;   1.0 μA MAX Ta = $25°C$
                 10 μA MAX Ta = $60°C$
                 50 μA MAX Ta = $85°C$
  Operation; 200 mW TYP

- High Speed (Equal Access and Cycle Time)
  MSM5128-20; 200 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- 24 Pin Flat PKG

PIN CONFIGURATION
(Top View)

A$_7$	1		24	V$_{CC}$
A$_6$	2		23	A$_8$
A$_5$	3		22	A$_9$
A$_4$	4		21	$\overline{WE}$
A$_3$	5		20	$\overline{OE}$
A$_2$	6		19	A$_{10}$
A$_1$	7		18	$\overline{CS}$
A$_0$	8		17	I/O$_8$
I/O$_1$	9		16	I/O$_7$
I/O$_2$	10		15	I/O$_6$
I/O$_3$	11		14	I/O$_5$
V$_{SS}$	12		13	I/O$_4$

$A_0 \sim A_{10}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS} : Supply Voltage

FUNCTIONAL BLOCK DIAGRAM
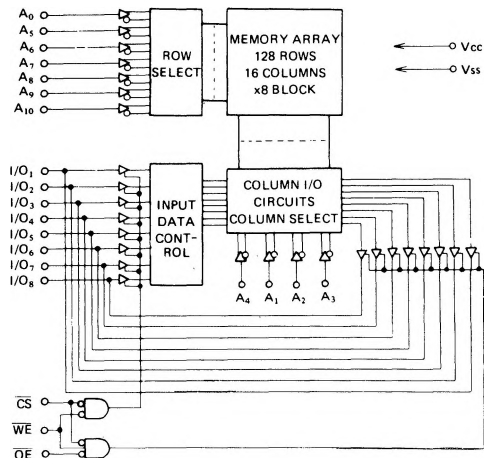
TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	−40 to 85	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Retention Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = –40°C to +85°C)

Parameter	Symbol		MSM5128-20			Unit	Test Condition	
			Min.	Typ.	Max.			
Input Leakage Current	I_{LI}		–1		1	µA	V_{IN} = 0 to V_{CC}	
Output Leakage Current	I_{LO}		–1		1	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}	
Output Voltage	V_{OH}		2.4			V	I_{OH} = –1 mA	
	V_{OL}				0.4	V	I_{OL} = 2.1 mA	
Standby Supply Current	I_{CCS}	Ta 25°C		0.1	1.0	µA	$\overline{CS} \geqq V_{CC}$ – 0.2V V_{IN} = 0 to V_{CC}	
		60°C			10			
		85°C			50			
	I_{CCS1}			0.3	1	mA	$\overline{CS}$ = V_{IH} t_{cyc} = Min. cycle	
Operating Supply Current	I_{CCA}			35	50	mA	Min. cycle	Ta = 0 ~ 85°C
				35	60	mA		Ta = –40 ~ 85°C

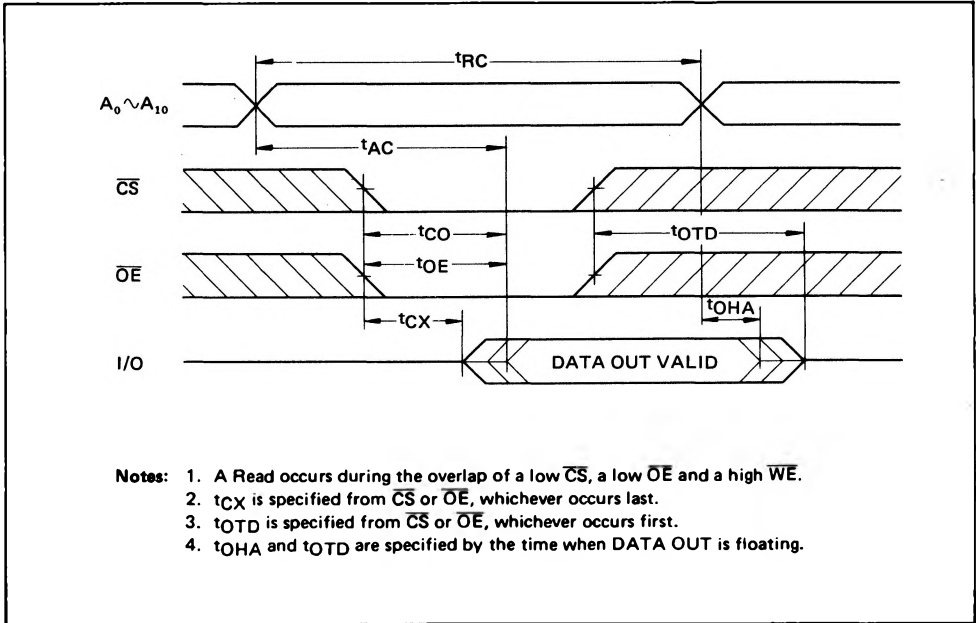## AC CHARACTERISTICS
Test Condition

Parameter	Conditions
Input Pulse Level	V_{IH}=2.2V, V_{IL}=0.8V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = –40°C to +85°C)

Parameter	Symbol	MSM5128-20		Unit
		Min.	Max.	
Read Cycle Time	t_{RC}	200		ns
Address Access Time	t_{AC}		200	ns
Chip Select Access Time	t_{CO}		200	ns
Output Enable to Output Valid	t_{OE}		120	ns
Chip Selection to Output Active	t_{CX}	20		ns
Output Hold Time from Address Change	t_{OHA}	20		ns
Output 3-state from Deselection	t_{OTD}	0	60	ns

READ CYCLE

Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

WRITE CYCLE

$(V_{cc} = 5V \pm 10\%, T_a = -40°C$ to $+85°C)$

Parameter	Symbol	MSM5128-20		Unit
		Min.	Max.	
Write Cycle Time	t_{WC}	200		ns
Address to Write Setup Time	t_{AS}	20		ns
Write Time	t_W	120		ns
Write Recovery Time	t_{WR}	20		ns
Data Setup Time	t_{DS}	80		ns
Data Hold from Write Time	t_{DH}	10		ns
Output 3-State from Write	t_{OTW}		60	ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE
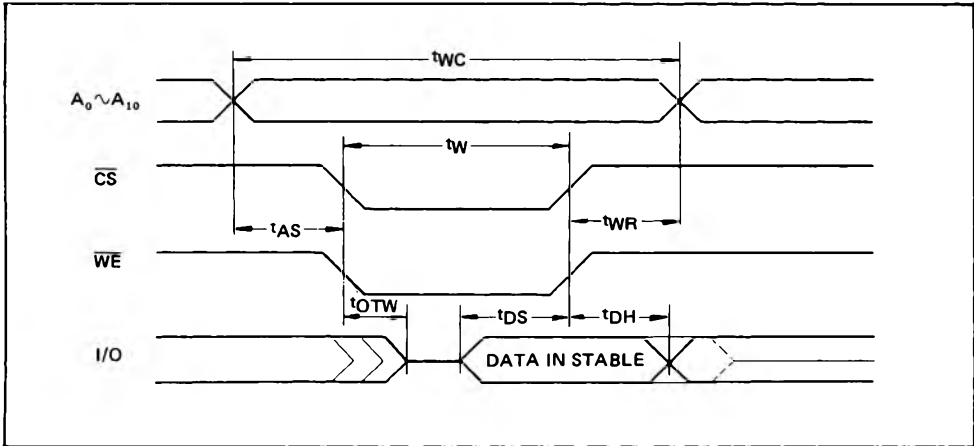
LOW V$_{CC}$ DATA RETENTION CHARACTERISTICS

(T_a = –40°C to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V$_{CC}$ for Data Retention	V$_{CCH}$	2			V	V$_{IN}$ = 0V to V$_{CC}$, $\overline{CS}$ = V$_{CC}$
Data Retention Current	I$_{CCH}$		0.05	20	µA	V$_{CC}$ = 2V $\overline{CS}$ = V$_{CC}$ V$_{IN}$ = 0V to V$_{CC}$
$\overline{CS}$ to Data Retention Time	t$_{SU}$	0			ns	
Operation Recovery Time	t$_R$	t$_{RC}$			ns	
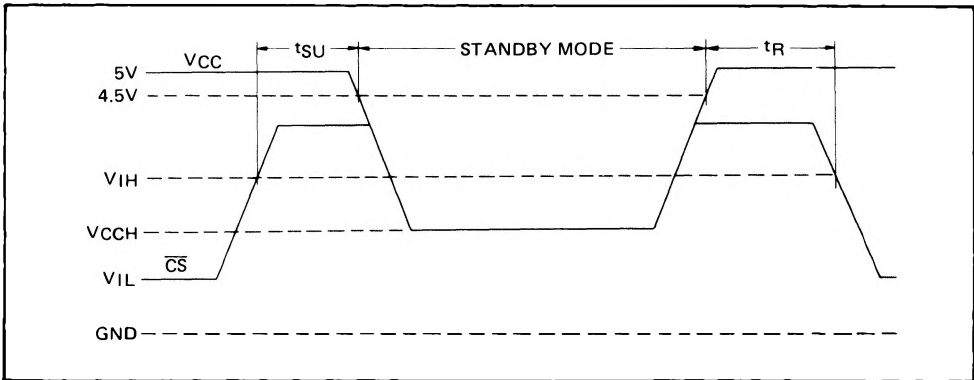
CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.