

MSM6408

HIGH-SPEED 4-BIT SINGLE CHIP MICROCONTROLLER

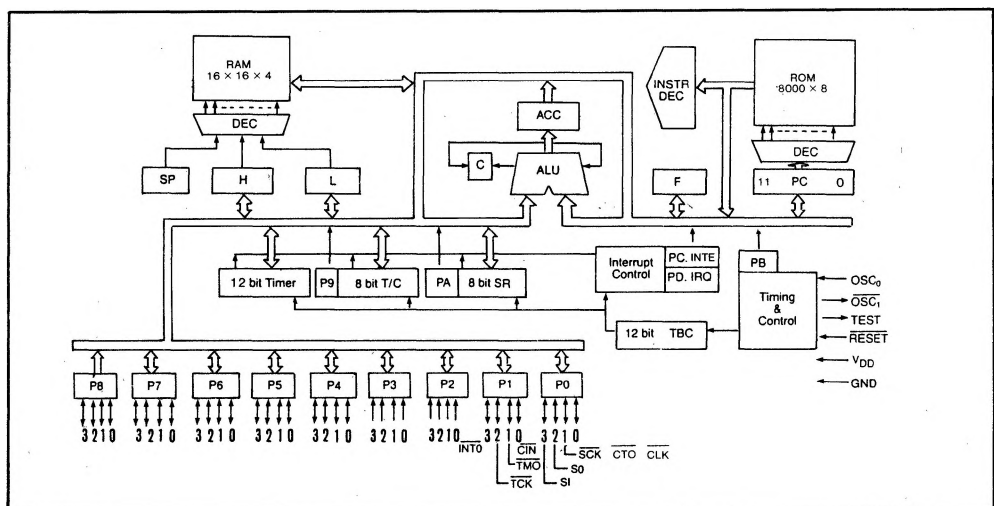
GENERAL DESCRIPTION

The OKI MSM6408 microcontroller is a low power, high-performance single-chip device implemented in complementary metal oxide semiconductor technology. 64K bits of mask program ROM, 1024 bits of data RAM, 36 Input/Output lines, a programmable timer/event-counter, and oscillator are integrated onto one chip. Program memory is byte wide and data-paths are organized in 4-bit nibbles. RAM and I/O lines are bit addressable. 122 instructions include binary, BCD operations; bit set, reset, test; 8-bit I/O; relative jumps; multifunctional instructional (increment, modify, skip) 8-bit wide table output; subroutine call and return.

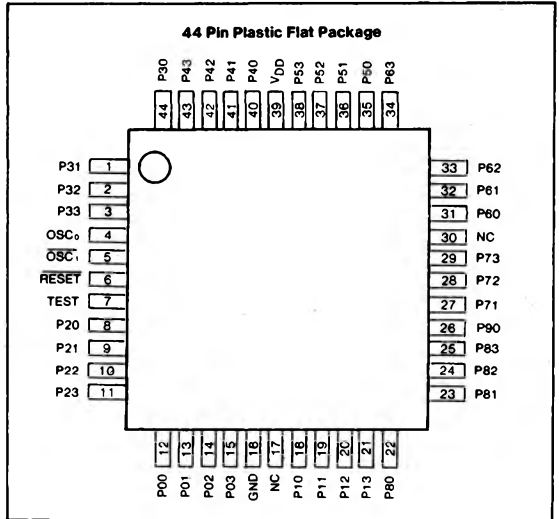
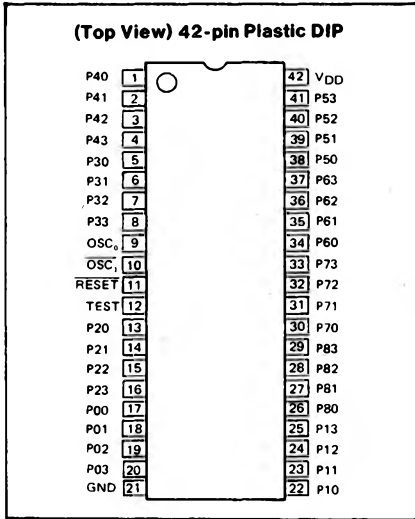
FEATURES

- 8000 × 8 MASK ROM
An evaluation board is available for up to 8K × 8.
- 256 × 4 RAM (including the stack area)
- 9 × 4 Ports, 36 I/O lines
4 lines for input ports having a latch, and the other 32 lines for bit operation are available.
- Three built-in counters
12-bit time-base counter
12-bit programmable timer
8-bit high-speed programmable timer/event counter
- Built-in 8-bit serial I/O register (with 3-bit counter)
- Five interrupts with five priority levels
(4 internal, 1 external)
- 32 stack levels (in RAM)
- Power down features
- Instruction execution time
1.0 μs 4.0 MHz clock
- Instruction systems suitable for control
- 122 instructions
- Mask option
P60-63 for input port
- Full static operation
- Low power consumption
TYP 0.4 μW at V_{DD}=2V
TYP 5 μW at V_{DD}=5V 0Hz clock
- 5V single power supply, 42-pin DIP or 44-pin FLAT

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin name	Input/output	Function	When reset
P00 / SCK P01 / SO P02 / SI P03 / SI	Input/output	4-bit input/output port. P01 to P03 are also used as serial interface terminals.	"1"
P10 / CIN P11 / TMO P12 / TCK P13	input/output	4-bit input port with latch. Built-in pull up register for all bit input.	"1"
P20 / INT P21 P22 P23	Input	4-bit input port with a latch. P20 is shared with INT input. (Fall trigger input) P21 ~ 23 are level input. Built-in pull up register for all bit input.	The latch is reset.
P30-33	Input/output	4-bit input/output port	"1"
P40-43	Input/output	4-bit input/output port	8-bit output port
P50-53	Input/output	4-bit input/output port	
P60-63	Input/output	4-bit input/output port *1	"0"
P70-73	Input/output	4-bit input/output port	"0"
P80-83	Input/output	4-bit input/output port	"0"
OSC ₀ OSC ₁	Input/output	X'tal connection terminal for system clock oscillation	Oscillation wave
TEST	Output	(Test terminal for Maker)	Pulse output
RESET	Input	System reset input terminal	
VDD GND		Power source voltage supply	

Note: When each port is used for output, it is possible to drive one TTL (one input).

*1 Can be made as a port dedicated to input (mask option).

INSTRUCTION LIST

	Mnemonic	Description	Code	Byte	Cycle
Load, Push, Pop	LAI n	A ← n	9n	1	1
	LLI n	L ← n	8n	1	1
	LHLI nn	HL ← nn	15nn	2	2
	LMI nn	M(w) ← nn	14nn	2	2
	LAL	A ← L	21	1	1
	LLA	L ← A	2D	1	1
	LAH	A ← H	22	1	1
	LHA	H ← A	2E	1	1
	LAM	A ← M	38	1	1
	LMA	M ← A	2F	1	1
	LAM+	A ← M, L ← L+1, Skip if L=0	24	1	1
	LAM-	A ← M, L ← L-1, Skip if L=F	25	1	1
	LMA+	M ← A, L ← L+1, Skip if L=0	26	1	1
	LMA-	M ← A, L ← L-1, Skip if L=F	27	1	1
	LAMM n ₂	A ← M, H ← HV n ₂	39-3B	1	1
	LAMD mm	A ← Md	10mm	2	2
	LMAD mm	Md ← A	11mm	2	2
	LMTD mm	Md(w) ← T (M(w), A), T=ROM table	19mm	2	3
	LMCT	M(w) ← CT	3E59	2	2
	LCTM	CT ← M(w)	3E51	2	2
	LMSR	M(w) ← SR	3E5A	2	2
	LSRM	SR ← M(w)	3E52	2	2
LTMM	TM ← (M(w), A)	3E50	2	2	
PUSH	ST ← C, A, H, L, SP ← SP-4	1C	1	3	
POP	C, A, H, L, ← ST SP ← SP+4	1D	1	3	
Exchange	X	A ↔ M	28	1	1
	XM n ₂	A ↔ M, H ← HV n ₂	29-2B	1	1
	X+	A ↔ M, L ← L+1, Skip if L=0	3C	1	1
	X-	A ↔ M, L ← L-1, Skip if L=F	2C	1	1
Increment/ Decrement	INA	A ← A+1, Skip if A=0	30	1	1
	INM	A ← M+1, Skip if M=0	33	1	1
	INL	L ← L+1, Skip if L=0	31	1	1

INSTRUCTION LIST (Continued)

	Mnemonic	Description	Code	Byte	Cycle
Increment/Decrement	INH	$H \leftarrow H+1$, Skip if $M=0$	32	1	1
	INMD mm	$Md \leftarrow Md+1$, Skip if $Md=0$	12mm	2	2
	DCA	$A \leftarrow A-1$, Skip if $A=F$	34	1	1
	DCM	$M \leftarrow M-1$, Skip if $M=F$	37	1	1
	DCL	$L \leftarrow L-1$, Skip if $L=F$	35	1	1
	DCH	$H \leftarrow H-1$, Skip if $H=F$	36	1	1
	DCMD mm	$Md \leftarrow Md-1$, Skip if $Md=F$	13mm	2	2
Arithmetic	ADS	$A \leftarrow A+M$, Skip if $Cy=1$	02	1	1
	ADCS	$A, C \leftarrow A+M+C$, Skip if $Cy=1$	01	1	1
	ADC	$A, C \leftarrow A+M+C$	03	1	1
	AIS n	$A \leftarrow A+n$, Skip if $Cy=1$	3E4n	2	2
	DAA	$A \leftarrow A+6$	06	1	1
	DAS	$A \leftarrow A+10$	0A	1	1
	AND	$A \leftarrow A \vee M$	0D	1	1
	OR	$A \leftarrow A \vee M$	05	1	1
	EOR	$A \leftarrow A \vee M$	04	1	1
	CMA	$A \leftarrow \bar{A}$	0B	1	1
	CIA	$A \leftarrow \bar{A}+1$	0C	1	1
	RAL	Rotate Left with C	0E	1	1
	RAR	Rotate Right with C	0F	1	1
	TC	Skip if $C=1$	09	1	1
	SC	$C \leftarrow 1$	07	1	1
	RC	$C \leftarrow 0$	08	1	1
	Compare	CAI n	Skip if $A=n$	3E0n	2
CLI n		Skip if $L=n$	3E2n	2	2
CPI p, n		Skip if $Pp=n$	17pn	2	2
CMI n		Skip if $M=n$	3E1n	2	2
CAM		Skip if $A=M$	16	1	1
Bit operation	TAB n_2	Skip if $Abit(n_2)=1$	54-57	1	1
	RAB n_2	$Abit(n_2) \leftarrow 0$	64-67	1	1
	SAB n_2	$Abit(n_2) \leftarrow 1$	74-77	1	1
	TMB n_2	Skip if $Mbit(n_2)=1$	58-5B	1	1
	RMB n_2	$Mbit(n_2) \leftarrow 0$	68-6B	1	1

INSTRUCTION LIST (Continued)

	Mnemonic	Description	Code	Byte	Cycle
Bit operation	SMB n	Mbit (n ₂) ← 1	78-7B	1	1
	TFB n ₂	Skip if Fbit (n ₂) = 1	5C-5F	1	1
	RFB n ₂	Fbit (n ₂) ← 0	6C-6F	1	1
	SFB n ₂	Fbit (n ₂) ← 1	7C-7F	1	1
	TPB n ₂	Skip if Pbit (n ₂) = 1	50-53	1	1
	RPB n ₂	Pbit (n ₂) ← 0	60-63	1	1
	SPB n	Pbit (n ₂) ← 1	70-73	1	1
	TPBD p n ₂	Skip if Ppbit (n ₂) = 1	3D p ₀ ~ ₃	2	2
	RPBD p n ₂	Ppbit (n ₂) = 0	3D p ₄ ~ ₇	2	2
	SPBD p n ₂	Ppbit (n ₂) = 1	3D p ₈ ~ _B	2	2
Interrupt	MEI	MEIF ← 1	3E60	2	2
	MDI	MEIF ← 0	3E61	2	2
	EITB	EITBF ← 1	3DC9	2	2
	EITM	EITMF ← 1	3DCA	2	2
	EICT	EICTF ← 1	3DCB	2	2
	EIEX	EIEXF ← 1	3DC8	2	2
	DITB	EITBF ← 0	3DC5	2	2
	DITM	EITMF ← 0	3DC6	2	2
	DICT	EICTF ← 0	3DC7	2	2
	DIEX	EIEXF ← 0	3DC4	2	2
	TITB	Skip if EITBF = 1	3DC1	2	2
	TITM	Skip if EITMF = 1	3DC2	2	2
	TICT	Skip if EICTF = 1	3DC3	2	2
	TIEX	Skip if EIEXF = 1	3DC0	2	2
	TOEX	Skip if IRQEX = 1	3D20	2	2
	TQTB	Skip if IRQTB = 1	3DD0	2	2
	TQTM	Skip if IRQTM = 1	3DD1	2	2
	TQCT	Skip if IRQCT = 1	3DD2	2	2
	TQSR	Skip if IRQSR = 1	3DD3	2	2
	RQEX	IRQEX ← 0	3D24	2	2
RQTB	IRQTB ← 0	3DD4	2	2	
RQTM	IRQTM ← 0	3DD5	2	2	
RQCT	IRQCT ← 0	3DD6	2	2	
RQSR	IRQSR ← 0	3DD7	2	2	

INSTRUCTION LIST (Continued)

	Mnemonic	Description	Code	Byte	Cycle
Shift resistor	ECT	CTF ← 1 (start)	3DBB	2	2
	ESR	SRF ← 1 (start)	3DBA	2	2
	DCT	CTF ← 0 (stop)	3DB7	2	2
Counter	DSR	SRF ← 0 (stop)	3DB6	2	2
	TCT	Skip If CTF = 1	3DB3	2	2
	TSR	Skip If SRF = 1	3DB2	2	2
Branch	JCP a ₆	PC ← a ₆	C0~FF	1	1
	JP a ₁₂	PC ← a ₁₂	4a ₁₂	2	2
	LJP a ₁₃	PC ← a ₁₃	3F	3	4
	CZP a	ST ← PC+1, PC ← 2a, SP ← SP-4	Ba	1	4
	CAL a ₁₂	ST ← PC+2, PC ← a ₁₂ , SP ← SP-4	Aa ₁₂	2	4
	RT	PC ← ST, SP ← SP+4	IE	1	4
	RTS	PC ← ST, SP ← SP+4, Skip unconditional	IF	1	4
	JA	PC ← (PC - A) + 1	IA	1	1
	JM	PC ← (M(w), A)	IB	1	2
Input/Output	IP	A ← P	20	1	1
	IPD p	A ← Pp	3DpD	2	2
	OP	P ← A	23	1	1
	OPD p	Pp ← A	3DpC	2	2
CPU control	NOP	No Operation	00	1	1
	HALT	Halt CPU	3DB8	2	2
	STOP	Stop Clock	3DB9	2	2

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	$T_a = 25^\circ\text{C}$	-0.3 to 7	V
Input Voltage	V_I		-0.3 to V_{DD}	V
Output Voltage	V_O		-0.3 to V_{DD}	V
Power Dissipation	P_D	$T_a = 25^\circ\text{C}$ per package	200 max.	mW
		$T_a = 25^\circ\text{C}$ per output	50 max.	mW
Storage Temperature	T_{stg}	-	-55 to +150	$^\circ\text{C}$

OPERATING RANGE

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	$f_{(OSC)} \leq 1 \text{ MHz}$	3 to 6	V
		$f_{(OSC)} \leq 4.0 \text{ MHz}$	4.5 to 5.5	V
Data-Hold Voltage	V_{DDH}	$f_{(OSC)} = 0 \text{ Hz}$	2 to 6	V
Operating Temperature	T_{OP}	-	-40 to +85	$^\circ\text{C}$
Fan Out	N	MOS Load	15	-
		TTL Load	1	

DC CHARACTERISTICS

($V_{DD} = 5V \pm 10\%$, $T_a = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" Input Voltage*1,*2	V_{IH}	-	2.4	-	V_{DD}	V
"H" Input Voltage*3,*4	V_{IH}	-	3.6	-	V_{DD}	V
"L" Input Voltage	V_{IL}	-	-0.3	-	0.8	V
"H" Output Voltage*1,*5	V_{OH}	$I_O = -15\mu\text{A}$	4.2	-	-	V
"L" Output Voltage*1	V_{OL}	$I_O = 1.6\text{mA}$	-	-	0.4	V
"L" Output Voltage*5	V_{OL}	$I_O = 15\mu\text{A}$	-	-	0.4	V
Input Current*3	I_{IH}/I_{IL}	$V_I = V_{DD}/OV$	-	-	15/-15	μA
Input Current*2,*4	I_{IH}/I_{IL}	$V_I = V_{DD}/OV$	-	-	1/-30	μA
"H" Output Current*1	I_{OH}	$V_O = 2.4\text{V}$	-0.1	-	-	mA
"H" Output Current*1	I_{OH}	$V_O = 0.4\text{V}$	-	-	-1.2	mA
Input Capacity	C_I	$f = 1\text{MHz}$ $T_a = 25^\circ\text{C}$	-	5	-	pF
Output Capacity	C_O		-	7	-	
Current Dissipation (when stop condition)	I_{DD5}	$V_{DD} = 2\text{V}$, no load $T_a = 25^\circ\text{C}$	-	0.2	5	μA
		No load	-	1	100	μA
Current Dissipation	I_{DD}	Quartz oscillation $f = 4 \text{ MHz}$, no load	-	6	12	mA

*1 Applied to P0, P1, P3, P4, P5, P6, P7 and P8

*2 Applied to P2

*3 Applied to OSC₀

*4 Applied to RESET

*5 Applied to OSC₁

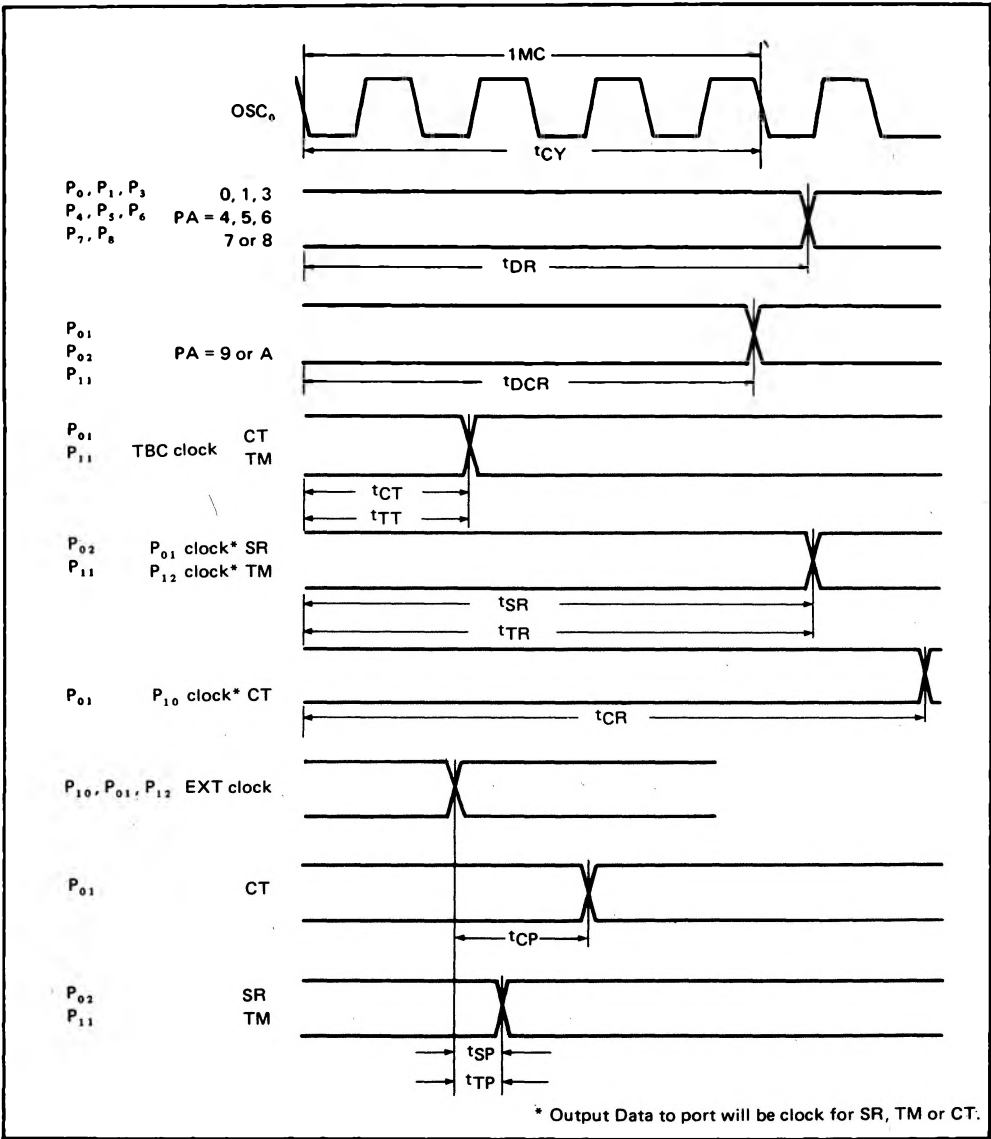
AC CHARACTERISTICS

($V_{DD} = 5V \pm 10\%$, $T_a = -40$ to $+85^\circ\text{C}$)

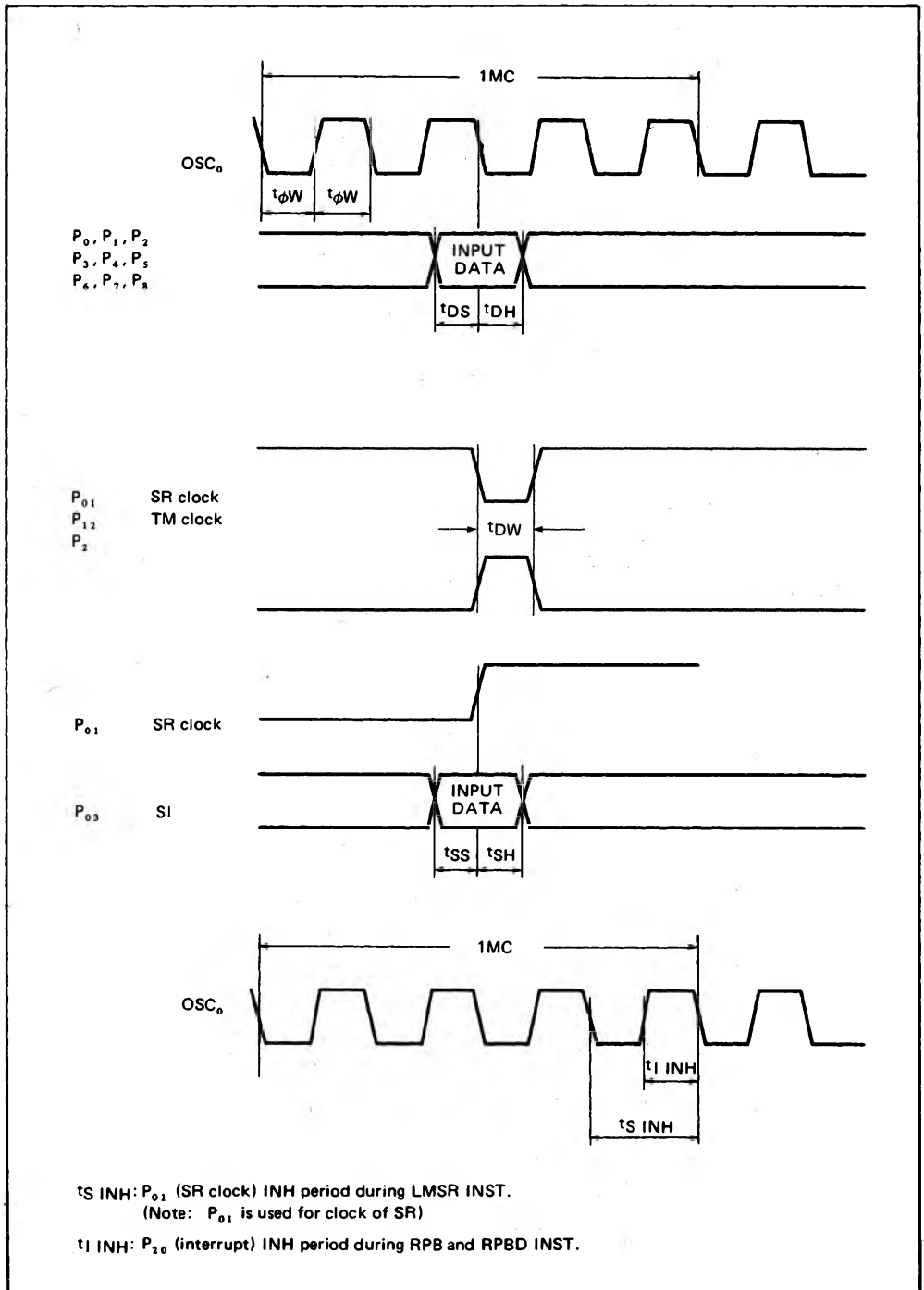
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock Pulse Width Clock (OSC)	$t_{\phi W}$	—	125	—	—	nS
Cycle Time	t_{CY}	—	1	—	—	μS
Input Data Setup Time	t_{DS}	—	120	—	—	nS
Input Data Hold Time	t_{DH}	—	120	—	—	nS
Input Data, Input Clock Pulse Width	t_{DW}	—	120	—	—	nS
SR Data Setup Time	t_{SS}	—	120	—	—	nS
SR Data Hold Time	t_{SH}	—	120	—	—	nS
Data Delay Time	t_{DR}	$C_L = 15\text{pF}$	—	—	$t_{CY} + 300$	nS
Data Delay Time at Mode Switching	t_{DCR}	$C_L = 15\text{pF}$	—	—	$7/8 t_{CY} + 300$	nS
CT/TM Data Delay Time using TBC Clock	t_{CT}/t_{TT}	$C_L = 15\text{pF}$	—	—	$2/8 t_{CY} + 360$	nS
SR/TM Data Delay Time using PR Clock	t_{SR}/t_{TR}	$C_L = 15\text{pF}$	—	—	$t_{CY} + 480$	nS
CT Data Delay Time using PR Clock	t_{CR}	$C_L = 15\text{pF}$	—	—	$10/8 t_{CY} + 480$	nS
CT Data Delay Time using External Clock	t_{CP}	$C_L = 15\text{pF}$	—	—	$2/8 t_{CY} + 360$	nS
SR/TM Data Delay Time using External Clock	t_{SP}/t_{TP}	$C_L = 50\text{pF}$	—	—	360	nS
SR Clock Invalid Time	t_{SINH}	—	$2/8 t_{CY}$	—	—	nS
INT Invalid Time	t_{IINH}	—	$1/8 t_{CY}$	—	—	nS

TIMING CHARTS

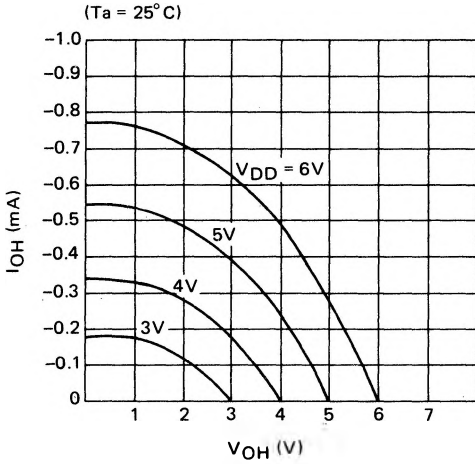
Output Condition



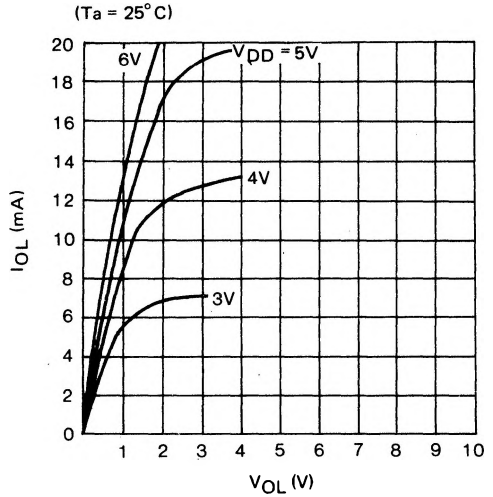
Input Condition



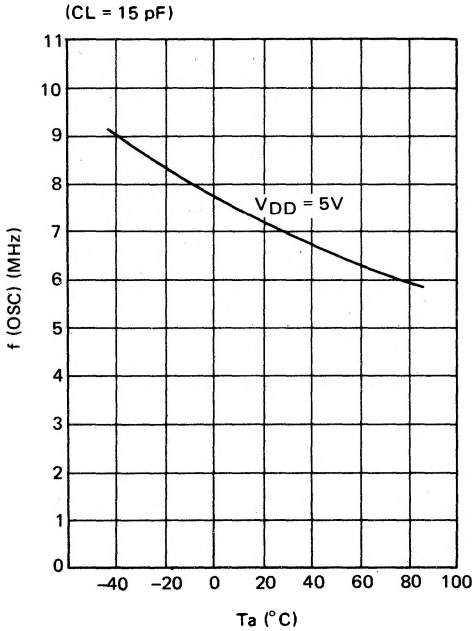
TYP. Current vs Voltage for High State Output
(I_{OH}) (V_{OH})



TYP. Current vs. Voltage for Low State Output
(I_{OL}) (V_{OL})



TYP. Maximum Oscillator Frequency vs
 $f(\text{OSC})$ Temperature
(T_a)



TYP. Maximum Oscillator Frequency vs.
 $f(\text{OSC})$ Supply Voltage
(V_{DD})

