19-0940; Rev 1; 7/95

CMOS 12 Bit Multiplying D/A Converter

General Description

The MX7541 is a high performance CMOS multiplying 12 bit digital-to-analog converter (DAC). Low power operation and 12-bit linearity (0.012%) make it suitable for a wide range of precision data acquisition and control applications.

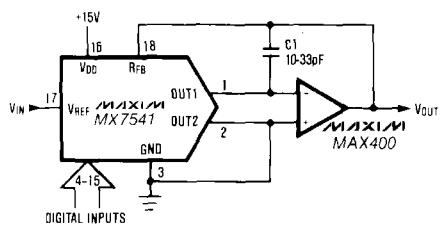
Wafer level laser trimmed thin-film resistors and temperature compensated NMOS switches assure true 12-bit performance over the full operating temperature range. In addition, all digital inputs are compatible with both CMOS and TTL logic levels.

Maxim's MX7541 is electrically and pin compatible with the Analog Devices AD7541. It is available in standard width 18-lead DIP and Small Outline (SO) packages.

Applications

Machine and Motion Control Systems
Automatic Test Equipment
μP Controlled Calibration Circuitry
Programmable Gain Amplifiers
Digitally Controlled Filters
Programmable Power Supplies

Typical Operating Circuit



Unipolar Operation

Features

- **12 Bit Linearity (1/2 LSB)**
- **1 LSB Gain Accuracy**
- **Guaranteed Monotonic**
- **Low Power Consumption**
- **Four-Quadrant Multiplication**
- **TTL and CMOS Compatible**
- **Pin-For-Pin Second Source**

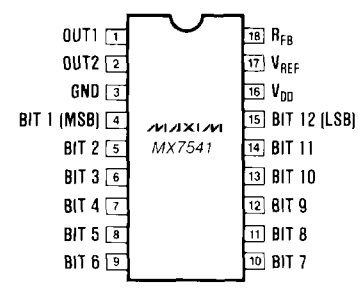
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
MX7541JN	0°C to +70°C	Plastic DIP	1 LSB
MX7541KN	0°C to +70°C	Plastic DIP	½ LSB
MX7541JCWN	0°C to +70°C	Small Outline	1 LSB
MX7541KCWN	0°C to +70°C	Small Outline	½ LSB
MX7541J/D	0°C to +70°C	Dice	1 LSB
MX7541AQ	-25°C to +85°C	CERDIP**	1 LSB
MX7541BQ	-25°C to +85°C	CERDIP**	½ LSB
MX7541AD	-25°C to +85°C	Ceramic	1 LSB
MX7541BD	-25°C to +85°C	Ceramic	½ LSB
MX7541SQ	-55°C to +125°C	CERDIP**	1 LSB
MX7541TQ	-55°C to +125°C	CERDIP**	½ LSB
MX7541SD	-55°C to +125°C	Ceramic	1 LSB
MX7541TD	-55°C to +125°C	Ceramic	½ LSB

* *All devices — 18 lead package.*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Pin Configuration

Top View



ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) ..... -0.3V, V_{DD}
Power Dissipation (Derate 6mW/°C above +75°C) 450mW

Operating Temperature Range
Commercial MX7541J/K ..... 0°C to +70°C
Industrial MX7541A/B ..... -25°C to +85°C
Military MX7541S/T ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

($T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +15V, V_{REF} = +10V, $V_{OUT1} = V_{OUT2}$ = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
DC ACCURACY						
Resolution			12			Bits
Nonlinearity		MX7541J/A/S (Note 2) MX7541K/B/T (Note 3)			±1 ±0.5	LSB
Gain Error (Note 4)		Using R_{FB}, T_A = +25°C T_{MIN} to T_{MAX}			±12.5 ±16.7	LSB
Power Supply Rejection	PSRR	V_{DD} = +14.5V to +15.5V; T_A = 25°C T_{MIN} to T_{MAX}			0.01 0.02	%/%V_{DD}
Output Leakage Current		V_{REF} = ±10V; T_A = +25°C T_{MIN} to T_{MAX}			±50 ±200	nA
Reference Input Resistance	R_{REF}	T_A = 25°C	5		20	kΩ
DYNAMIC PERFORMANCE (Note 5)						
Output Current Settling Time		To 1/2LSB			1	µs
Feedthrough Error		V_{REF} = 20V_{P-P} at 10kHz			1	mV_{P-P}
DIGITAL INPUTS						
Logic HIGH Threshold	V_{INH}		+2.4			V
Logic LOW Threshold	V_{INL}				+0.8	V
Input Leakage Current		Digital Inputs = 0V or V_{DD}			±1	µA
Input Capacitance	C_{IN}	(Note 5)			8	pF
Input Coding		Binary, Offset Binary				
ANALOG OUTPUTS						
Output Capacitance (Note 5)	C_{OUT}	Digital Inputs = V_{INH} OUT1 OUT2 Digital Inputs = V_{INL} OUT1 OUT2			200 60 60 200	pF
POWER REQUIREMENTS						
Operating Supply Range	V_{DD}	Accuracy Not Guaranteed	+5		+16	V
Power Supply Current	I_{DD}	Digital Inputs = V_{INH} or V_{INL}			2	mA

Note 1: $V_{OUT1,2}$ may exceed the Absolute Maximum Voltage rating if the current is limited to 30mA or less.
Note 2: MX7541J/A/S are monotonic to 11 bits.
Note 3: MX7541K/B/T are monotonic to 12 bits.
Note 4: Maximum gain change from +25°C to T_{MIN} or T_{MAX} is ±4.2 LSBs using internal feedback resistor.
Note 5: Guaranteed by design but not 100% tested.

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Detailed Description

The basic MX7541 DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Most applications require only an output op-amp and reference source. The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs.

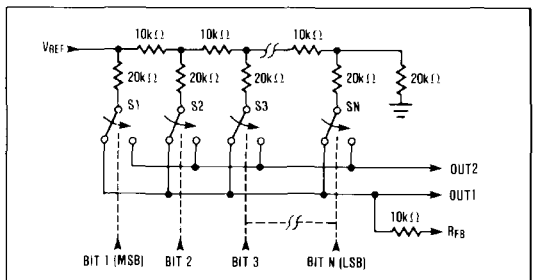

Figure 1. MX7541 Functional Diagram

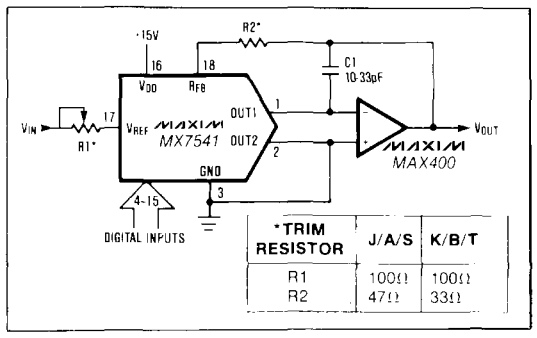

Figure 2. Unipolar Binary Operation

Table 1. Code Table — Unipolar Binary

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{4095}{4096}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2V_{REF}$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{4096}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	0V

Application Information

Unipolar Operation

The most common configuration for the MX7541 is shown in Figure 2. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. The code table is given in Table 1. Note that the polarity of the output is the inverse of the reference input.

In many applications, gain adjustment of the MX7541 will not be necessary. In those cases, and also when gain is trimmed but only at the reference source, resistors R1 and R2 in Figure 2 can be omitted. However, if the trims are required and the DAC is to operate over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used at R1 and R2.

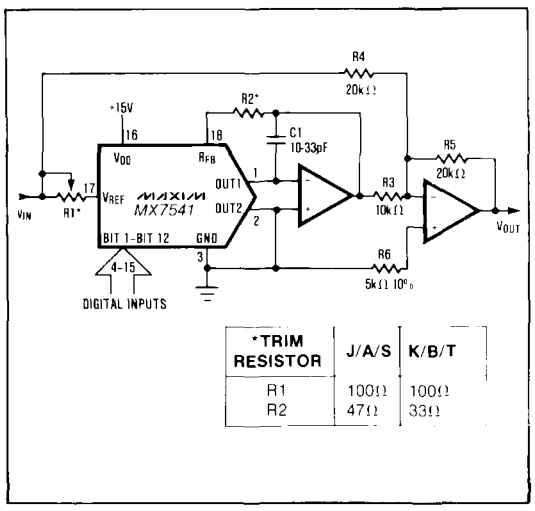

Figure 3. Bipolar Operation (4-Quadrant Multiplication)

Table 2. Code Table — Bipolar (Offset Binary) Operation

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{2047}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	0V
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{2048}\right)$

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Bipolar Operation

Bipolar, or four-quadrant, operation is shown in Figure 3. A second amplifier and three matched resistors are required. Matching to 0.01% is recommended for 12 bit performance. The code table for the output, which is "offset binary", is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control amplitude.

Output Amplifier Offset

For best linearity, OUT1 and OUT2 should be terminated at exactly 0V. In most applications, OUT1 is connected to the summing junction of an inverting op-amp. The amplifier's offset voltage can degrade the linearity of the DAC by causing OUT1 to be terminated to a non-zero voltage. The resulting error is typically $4/3V_{OS}$ to $2V_{OS}$, a change of $2/3V_{OS}$. An amplifier with 3mV of offset will therefore degrade the linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10 of an LSB's value.

An output amplifier's input bias current (I_B) can also limit the DAC's performance since $I_B \times R_{FB}$ generates an offset error. I_B should therefore be much less than the DAC output current for 1 LSB, typically 250nA with V_{REF} = 10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier's noninverting input is grounded through a "bias current compensation resistor." This resistor adds to the offset at this pin and should not be used.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is mostly dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

Compensation

A compensation capacitor, C1, may be needed when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. Its value depends on the type of op-amp used but typical values range from 10 to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized, and output settling performance improved, by keeping the PC board trace and stray capacitance at OUT1 as small as possible.

Grounding and Bypassing

Since OUT1, OUT2 and the output amp's noninverting input are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, very low resistance (less than 0.2Ω) path. The current at OUT1 and OUT2 varies with input code creating a code dependent error if these terminals are connected to ground (or a virtual ground) through a resistive path.

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic cap, should be connected as close to the DAC's V_{DD} and GND pins as possible.

The MX7541 has high-impedance digital inputs. To minimize noise pick-up, they should be tied to either VDD or GND when not used. It is also good practice to connect active inputs to VDD or GND through high valued resistors (1MΩ) to prevent static charge accumulation if these pins are left floating, such as when a circuit card is left unconnected.

Chip Topography