

# Signetics QUAD 2-INPUT HIGH VOLTAGE NAND GATE

# S5426 N7426

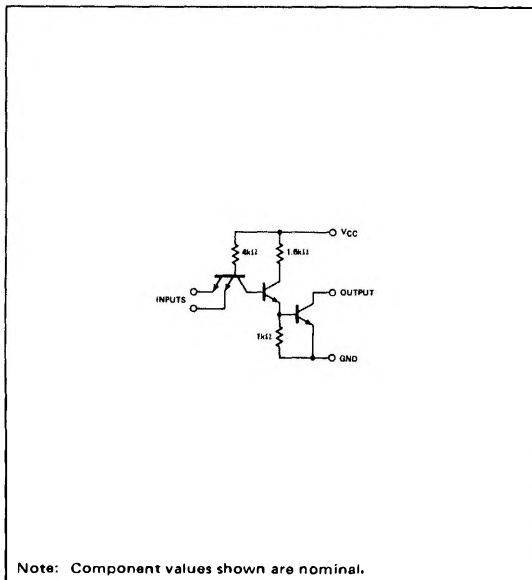
S5426-A,F • N7426-A,F

DIGITAL 54/74 TTL SERIES

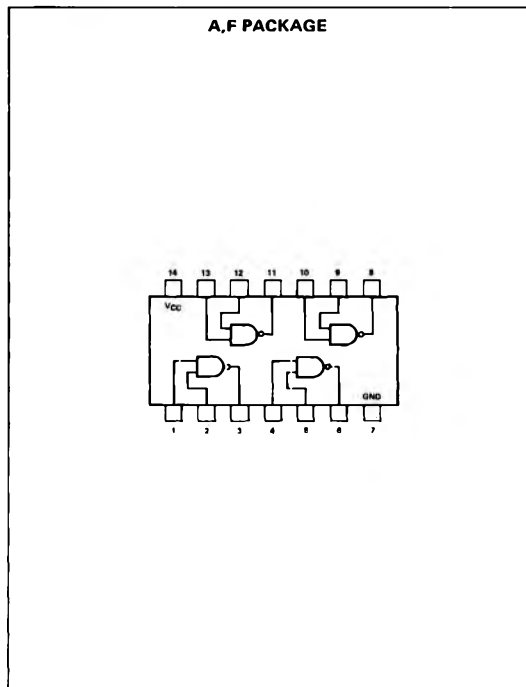
## DESCRIPTION

The 54/7426 Quad 2-Input NAND Gate features standard TTL inputs with high voltage (15 volts) open collector outputs for interface with MOS, lamps or relays.

## SCHEMATIC (each gate)



## PIN CONFIGURATION



## RECOMMENDED OPERATING CONDITIONS

	S5426			N7426			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
Output Voltage, $V_{OH}$			15			15	V
Low-Level Output Current, $I_{OL}$			16			16	mA
Operating Free-Air Temperature Range, $T_A$	-55	25	125	0	25	70	$^{\circ}C$

## ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS *	MIN	TYP **	MAX	UNIT
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$V_{OH}$	High-level output voltage	15			V
$I_{OH}$	High-level output current			50	$\mu A$
$V_{OL}$	Low-level output voltage			0.4	V
$i_{IH}$	High-level input current			40	$\mu A$
	(each input)			1	mA
$I_{IL}$	Low-level input current			-1.6	mA
	(each input)				
$I_{CCH}$	Supply current, high-level output		4	8	mA
$I_{CCL}$	Supply current, low-level output		12	22	mA

SWITCHING CHARACTERISTICS,  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ 

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output	$C_L = 15pF$ ,	$R_L = 1k\Omega$		16	24	ns
$t_{PHL}$	Propagation delay time high-to-low-level output	$C_L = 15pF$ ,	$R_L = 1k\Omega$		11	17	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\* All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .