DESCRIPTION

The 54/7495 is a monolithic universal 4-Bit Shift Register designed with standard TTL techniques. The circuit layout consists of 4 R-S master-slave flip-flops, 4 AND-OR-INVERT gates, and 6 inverters configured to form a versatile register which will perform right-shift, left-shift, or parallel-in, parallel-out operations depending on the logical input level to the mode control.

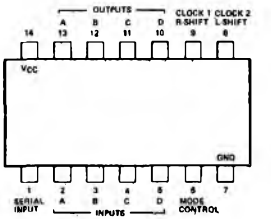
Right-shift operations are performed when a logical 0 level is applied to the mode control. Serial data is entered at the serial input D_S and shifted one position right on each clock 1 pulse. In this mode, clock 2 and parallel inputs D_A thru D_D are inhibited.

Parallel-in, parallel-out operations are performed when a logical 1 level is applied to the mode control. Parallel data is entered at parallel inputs D_A thru D_D and is transferred to the data outputs A_0 thru D_0 on each clock 2 pulse. In this mode, shift-left operations may be implemented by externally tying the output of each flip-flop to the parallel input of the previous flip-flop (D_0 to D_C and etc.), with serial data entry at input D_D.

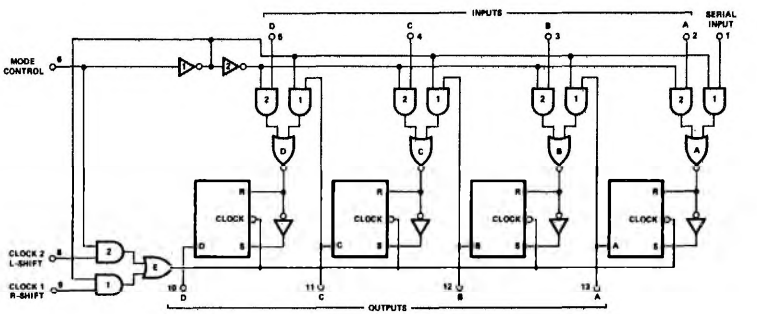
Information must be present at the R-S inputs prior to clocking and transfer of data occurs on the falling edge of the clock pulse.

PIN CONFIGURATIONS

A,F PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}	S5495 Circuits	4.5	5	5.5	V
	N7495 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output				10	
Width of Clock Pulse $t_{p(clock)}$	S5495 Circuits	20	10		ns
	N7495 Circuits	15	10		ns
Setup Time Required at Serial, A, B, C, or D Inputs t_{setup}		10	10		ns
Hold Time Required at Serial, A, B, C, or D Inputs t_{hold}		0	10		ns
Logical 0 Level Setup Time Required at Mode Control (With Respect to Clock 1 inputs)		15			ns
Logical 1 level Setup Time Required at Mode Control (With Respect to Clock 2 input)		15			ns
Logical 0 Level Setup Time Required at Mode Control (With Respect to Clock 2 input)		5			ns
Logical 1 Level Setup Time Required at Mode Control (With Respect to Clock 1 input)		5			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -800μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA				0.4	V
$I_{in(0)}$	Logical 0 level input current at any input except mode control	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at mode control	V_{CC} = MAX, V_{in} = 0.4V				-3.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except mode control	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at mode control	V_{CC} = MAX, V_{in} = 2.4V				80	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX	N7495	39	50	63	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	C_L = 15pF,	R_L = 400Ω	25	36		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs	C_L = 15pF,	R_L = 400Ω		18	27	ns
t_{pd0}	Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs	C_L = 15pF,	R_L = 400Ω		21	32	ns

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.