

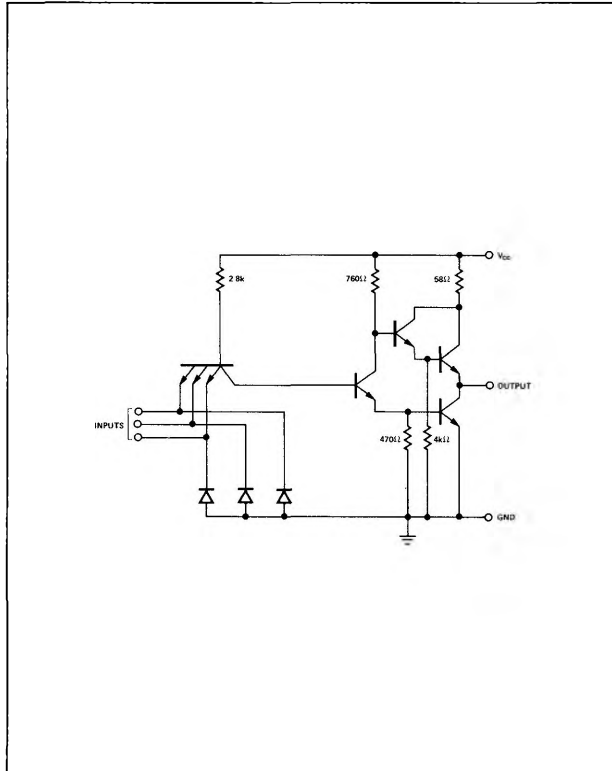
TRIPLE 3-INPUT POSITIVE NAND GATE

S54H10 N74H10

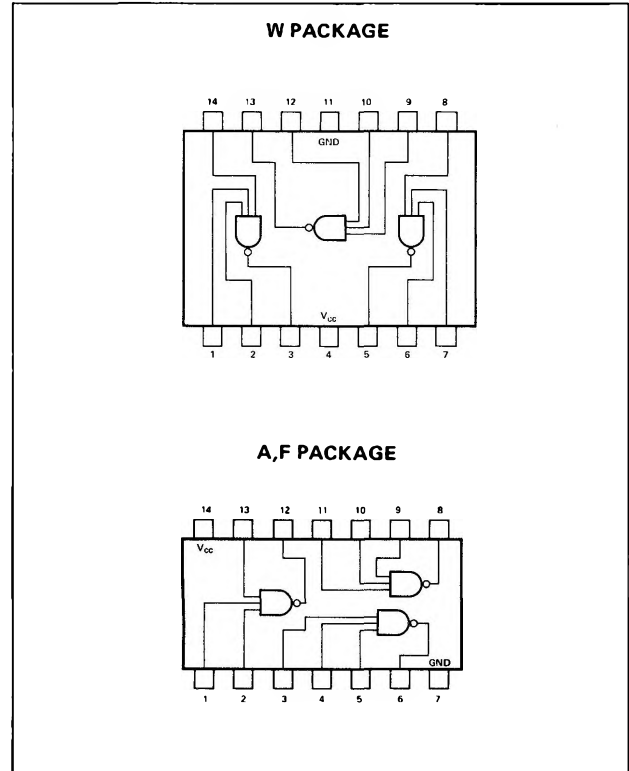
S54H10—A,F,W • N74H10—A,F

DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)



PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} : S54H10 Circuits	4.5	5	5.5	V
N74H10 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Operating Free-Air Temperature Range, T_A : S54H10 Circuits	-55	25	125	$^{\circ}\text{C}$
N74H10 Circuits	0	25	70	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	$V_{CC} = \text{MIN},$	2		V
$V_{in(0)}$	Logical 0 input voltage required of any input terminal to ensure logical 1 level at output	$V_{CC} = \text{MIN},$		0.8	V
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN},$ $I_{load} = -500\mu\text{A}$	$V_{in} = 0.8\text{V},$	2.4	V
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN},$ $I_{sink} = 20\text{mA}$	$V_{in} = 2\text{V},$	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX},$	$V_{in} = 0.4\text{V}$	-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	$V_{CC} = \text{MAX},$ $V_{CC} = \text{MAX},$	$V_{in} = 2.4\text{V}$ $V_{in} = 5.5\text{V}$	50 1	μA mA
I_{OS}	Short circuit output current†	$V_{CC} = \text{MAX}$		-40 -100	mA

SIGNETICS DIGITAL 54/74 TTL SERIES – S54H10 • N74H10

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	$V_{CC} = \text{MAX}, V_{in} = 4.5\text{V}$		19.5	30	mA
$I_{CC(1)}$	Logical 1 level supply current	$V_{CC} = \text{MAX}, V_{in} = 0$		7.5	12.6	mA

SWITCHING CHARACTERISTICS, $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}, N = 10$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	$C_L = 25\text{pF}, R_L = 280\Omega$		6.3	10	ns
t_{pd1}	Propagation delay time to logical 1 level	$C_L = 25\text{pF}, R_L = 280\Omega$		5.9	10	ns

- * For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- ** All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- † Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.