DUAL J-K EDGE-TRIGGERED FLIP-FLOP

S54S112
N74S112

S54S112–B,F,W • N74S112–B

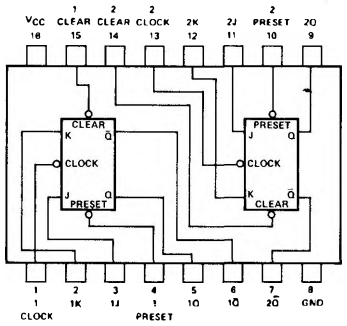
DIGITAL 54/74 TTL SERIES

DESCRIPTION

These monolithic dual J-K flip-flops feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. When the clock goes high the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the truth table as long as minimum setup and hold times are observed. Input data are transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATIONS

B,F,W PACKAGE



TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:

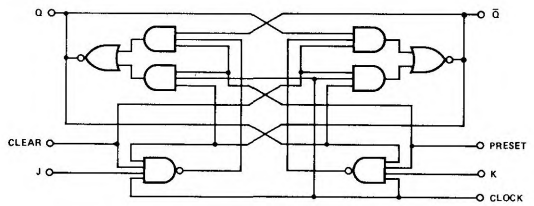
A. t_n = bit time before clock pulse

B. t_{n+1} = bit time after clock pulse

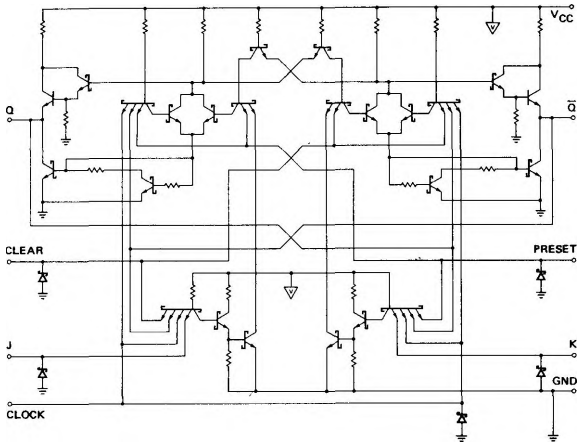
POSITIVE LOGIC

positive logic: Low input to preset sets Q to high level.
Low input to clear resets Q to low level.
Clear and preset are independent of clock.

LOGIC DIAGRAM (each flip-flop)



SCHEMATIC (each flip-flop)



RECOMMENDED OPERATING CONDITIONS

	S54S112			N74S112			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N : High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		80	0		80	MHz
Width of Clock Pulse, $t_{w(clock)}$	6			6			ns
Width of Preset Pulse, $t_{w(preset)}$	8			8			ns
Width of Clear Pulse, $t_{w(clear)}$	8			8			ns
Input Setup Time, t_{setup} (See Note 1)	3			3			ns
Input Hold Time, t_{hold} (See Note 2)	0			0			ns
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS *			MIN	TYP **	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA				-1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V,	I_{OH} = -1mA	S54S112	2.5	3.4		V
				N74S112	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V,	I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V		J or K input			50	µA
				Clock, preset, or clear			100	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V		J or K input			-1.6	mA
				Clock			-4	
				Preset or clear			-7	
I_{OS}	Short-circuit output current†	V_{CC} = MAX,			-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3			30	50	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency		80	125		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset	C_L = 15pF, R_L = 280Ω	2	5	7	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock		2	5	7	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTES:

1. Setup time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.
3. I_{CC} is measured with outputs open, clock grounded, and J-K preset and clear at 4.5V.