

### DIGITAL 54/74 TTL SERIES

#### N74S64 ACTIVE PULL-UP

- TYPICAL PROPAGATION TIME
- TYPICAL POWER DISSIPATION AT 50% DUTY CYCLE

3.5 ns at  $C_L = 15 \text{ pF}$   
39 mW

#### N74S65 OPEN COLLECTOR

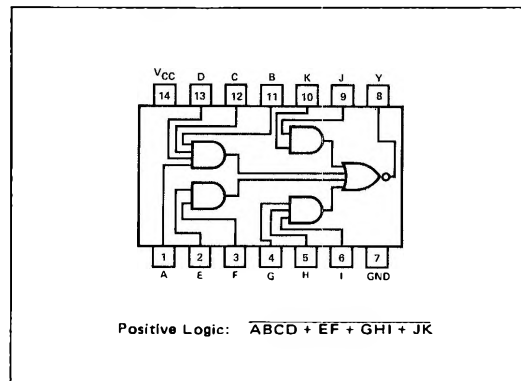
- TYPICAL PROPAGATION TIME
- TYPICAL POWER DISSIPATION AT 50% DUTY CYCLE

5 ns at  $C_L = 15 \text{ pF}$   
36 mW

#### RECOMMENDED MAXIMUM FAN-OUT FROM EACH OUTPUT

	N74S64	N74S65
Loads at a high logic level	20	
Loads at a low logic level	10	10

#### PIN CONFIGURATIONS



#### ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	N74S64			N74S65			UNIT
		MIN	TYP**	MAX	MIN	TYP**	MAX	
$V_{IH}$ High-level input voltage		2			2			V
$V_{IL}$ Low-level input voltage				0.8			0.8	V
$V_I$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$ (N74S64)	2.7	3.4					V
$I_{OH}$ High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$						250	$\mu\text{A}$
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$ High-level input current (each input)	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50			50	$\mu\text{A}$
$I_{IL}$ Low-level input current (each input)	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2			-2	mA
$I_{OS}$ Short-circuit output current ‡	$V_{CC} = \text{MAX}$	-40		-100				mA
$I_{CCH}$ Supply current, high-level output	$V_{CC} = \text{MAX}$ , See Note 1		7	12.5		6	11	mA
$I_{CCL}$ Supply current, low-level output	$V_{CC} = \text{MAX}$ , See Note 2		8.5	16		8.5	16	mA

\* All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTES: 1.  $I_{CCH}$  is measured with all inputs grounded, and the outputs open.

2.  $I_{CCL}$  is measured with all inputs of one gate at 5 V, the remaining inputs grounded, and the outputs open.

#### SWITCHING CHARACTERISTICS, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}, N = 10$

PARAMETER	TEST CONDITIONS NOTE 3	N74S64			N74S65			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH}$ Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}, R_L = 280 \Omega$	2	3.5	5.5	2	5	7.5	ns
	$C_L = 50 \text{ pF}, R_L = 280 \Omega$		5			8		
$t_{PHL}$ Propagation delay time, high-to-low-level output	$C_L = 15 \text{ pF}, R_L = 280 \Omega$	2	3.5	5.5	2	5.5	3.5	ns
	$C_L = 50 \text{ pF}, R_L = 280 \Omega$		5.5			6.5		

NOTE 3: Load circuit and waveforms are shown on page 2-293

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