11-BAND EVR FOR GRAPHIC EQUALIZER

■ GENERAL DESCRIPTION

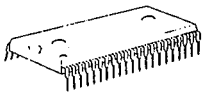
The NJU7307 is a electrical variable resistor (EVR) incorporated 11-band each for left and right channels, especially apply to the stereo type graphic equalizer.

It consists of input controller, channel/band/level selector, 22 latches and resistor network blocks of 11 bands each for left and right channels.

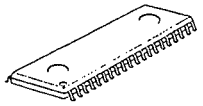
The boost and cut value for each band of each channel can be set independently to each other by the channel/band/level selector controlled by external controller.

The maximum boost and cut range is ±18dB and the boost and cut value is adjusted by ±3dB step.

■ PACKAGE OUTLINE



NJU7307L

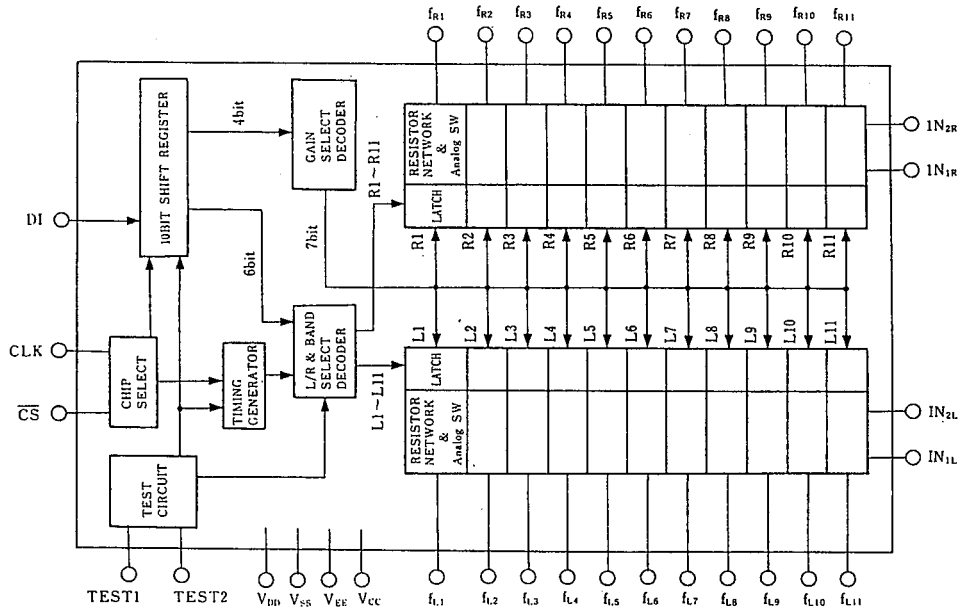


NJU7307G

■ FEATURES

- 11 Bands Each for Left and Right Channels
- Stereo Application Graphic Equalizer
  Each Channel Independent Operation
- Maximum Boost and Cut --- ±18dB
- Boost and Cut Step --- ±3dB
- 10bit Serial Data for the Equalizing
- Flat Level Setting Function
- Operating Voltage --- 15V~30V
- Package Outline --- SDIP 42/SOP 40
- C-MOS Technology

■ BLOCK DIAGRAM



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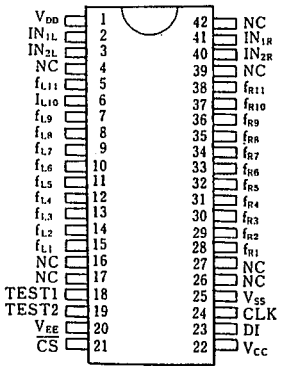
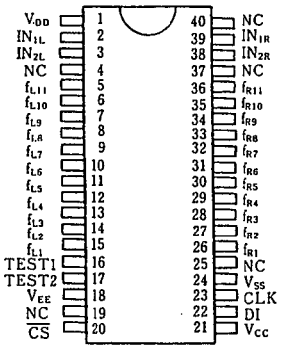
■ PIN CONFIGURATION



NJU7307L



NJU7307G

■ TERMINAL DESCRIPTION

NO.		SYMBOL	FUNCTION
NJU7307L	NJU7307G		
1	1	V_{DD}	Power source for Audio signal +15V
25	24	V_{SS}	GND 0V
20	18	V_{EE}	Power source for Audio signal -15V
22	21	V_{CC}	Power source for Logic +5.0V
2, 41	2, 39	I_{N1L}, I_{N1R}	Audio signal input terminal. Connect to Op-amp inverting terminal
3, 40	3, 38	I_{N2L}, I_{N2R}	Audio signal input terminal. Connect to Op-amp non-inverting terminal
5 to 15	5 to 15	f_{L1} to f_{L11}	Band pass filter connecting terminal.
28 to 38	26 to 36	f_{R1} to f_{R11}	(22 terminals for left/right)
18	16	TEST1	Maker testing terminals.
19	17	TEST2	Normally (except the test) OPEN
21	20	$\overline{CS}$	Chip-select input.
23	22	DI	Serial data input.
24	23	CLK	Clock signal input.
4,16,17 26,27,39 42	4,19,25 37,40	NC	Non connection

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■ FUNCTIONAL DESCRIPTION

(1) Data set and code format

The setting of each band is performed by two signals of data and clock as shown in Fig.1.

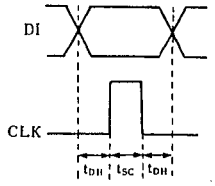
The 10 bits serial data including the information of channel selection (left/right), band selection and its gain are input from DI terminal.

The clock signal input from the CLK terminal shifts the serial data input form DI terminal into the shift register.

The data input from DI terminal is performed during the CS terminal is "L"level. Then the $\overline{CS}$ terminal change from "L" to "H" level, the data in the shift register is latched to the latch.

All "H" of 10 bits code are special code to set 0dB for all bands at once. This function is useful for Power On initialization or flat level setting.

< Data and Shift Clock >



The shift clock should be risen after 1μs from the data changing.
t_{SC}=1μs(MIN)
t_{DH}=1μs(MIN)

< Time Chart >

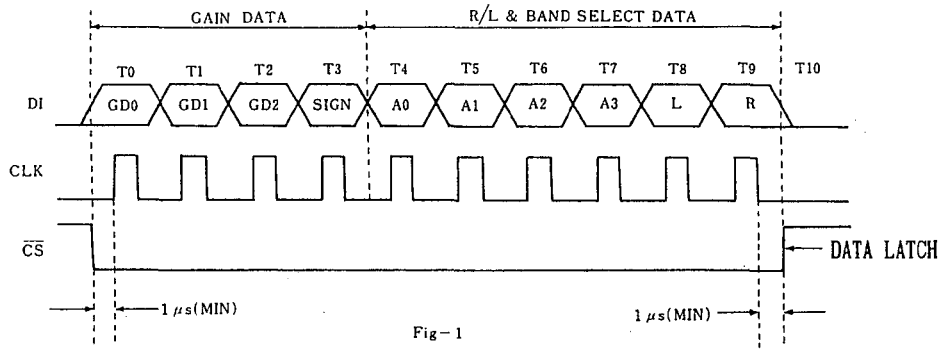


Fig-1

The $\overline{CS}$ terminal should be "L" level during the data input. The setting data is latched at the edge of $\overline{CS}$ signal rising. If the error data is latched, the correct data must be set again from the top.

Note: The clock line should be shielded from the noise.

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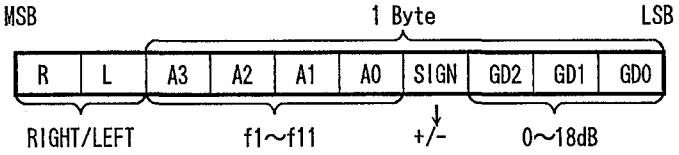
< Data Format >

The data is input by the LSB first format as shown bellow. And the gain data GD2 to GD0, left/right and band selection data are also shown in bellow.



GAIN DATA CODE

GAIN	SIGN	GD2	GD1	GD1
18	0	1	1	0
15	0	1	0	1
12	0	1	0	0
9	0	0	1	1
6	0	0	1	0
3	0	0	0	1
0dB	0	0	0	0
-3	1	0	0	1
-6	1	0	1	0
-9	1	0	1	1
-12	1	1	0	0
-15	1	1	0	1
-18	1	1	1	0

BAND SELECT DATA CODE

BAND	A3	A2	A1	A0
f1	0	0	0	1
f2	0	0	1	0
f3	0	0	1	1
f4	0	1	0	0
f5	0	1	0	1
f6	0	1	1	0
f7	0	1	1	1
f8	1	0	0	0
f9	1	0	0	1
f10	1	0	1	0
f11	1	0	1	1

R/L SELECT DATA CODE

R/L	R	L
RIGHT	1	0
LEFT	0	1
RIGHT & LEFT	1	1

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(2) Power on initialization

The NJU7307 is not incorporated the Power On Initialization Circuits, so that internal circuits are not defined when the power is turned on. Therefore, the flat setting operation are required as 10 bits of "H" data with 10 clock pulse input during the $\overline{CS}$ terminal "L" state, then after change the $\overline{CS}$ terminal level from "L" to "H".

The internal circuits of NJU7307 are initialized by the above operation, then the following input will be accepted.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}-V_{EE}	34	V
	V_{CC}	V_{SS}～V_{SS}+7(V_{DD}≧V_{CC})	
Input Voltage	V_{IN}	V_{SS}-0.3 ～V_{CC}+0.3 (DI,CLK,$\overline{CS}$)	V
		V_{EE}-0.3～V_{DD}+0.3(I_{N1L}～I_{N2L},I_{N1R}～I_{N2R})	
Power Dissipation	PD	250 (SDIP,SOP)	mW
Operating Temperature	T_{opr}	-30 ～ +80	℃
Storage Temperature	T_{stg}	-40 ～ +125	℃

■ ELECTRICAL CHARACTERISTICS

(V_{SS}=0V,V_{DD}≧V_{CC}>V_{SS}≧V_{EE},Ta=25℃)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}-V_{EE}	V_{EE}≧-15V	15	20	30	V
	V_{CC}		4.5	5.0	5.5	
Operating Current	I_{DD}	V_{DD}-V_{EE}=30V			1	mA
	I_{CC}	V_{CC}=5V			0.5	
Input Voltage	V_{IH}	CLK,DI,$\overline{CS}$	0.8V_{CC}		V_{CC}	V
	V_{IL}	Terminals	0		0.2V_{CC}	
Input Pulse Width	t_{PW}	CLK	1			μS
Setup Time	t_{SU}	DI	1			μS
Holding Time	t_{HLD}	DI	1			μS
Operating Frequency	f_{OPR}	CLK			330	kHz
Total Harmonics Distortion	THD1	Flat Status, f=20kHz		0.005	0.01	%
	THD2	Flat Status, f= 1kHz		0.0015	0.003	
	THD3	Boost Status, f=20kHz		0.05	0.10	
	THD4	Boost Status, f= 1kHz		0.015	0.03	
		(Circuit 1)				
Crosstalk	CT	f= 1kHz (Circuit 2)		60		dB
Setting Error	△B	V_{DD}-V_{EE}=30V (Circuit 1)	-1		1	dB
Analog SW Off Leakage Current	I_{off}	f_{L1}～f_{L11}			100	μA
		f_{R1}～f_{R11}				

Note) The setting error of gain is specified by mesureing of Circuit 1 based on internal current flown on Circuit 3.
Actual setting error of gain is affected by external circuit characteristics. Therefore, experimental operation is recommended when designing.

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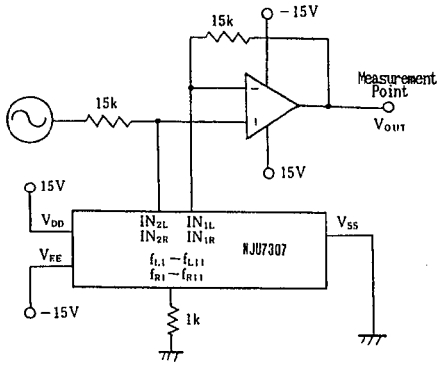
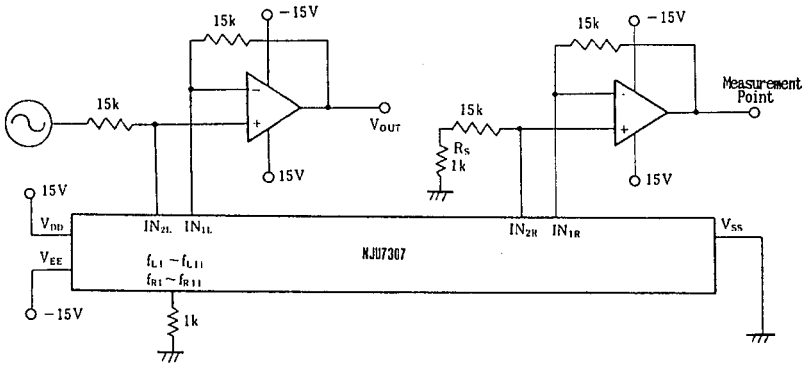
■ MEASUREMENT CIRCUITS

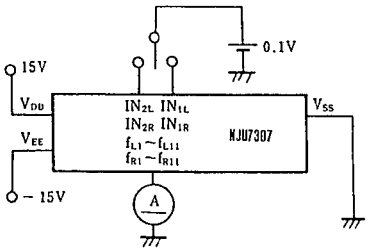
Circuit 1



Circuit 2

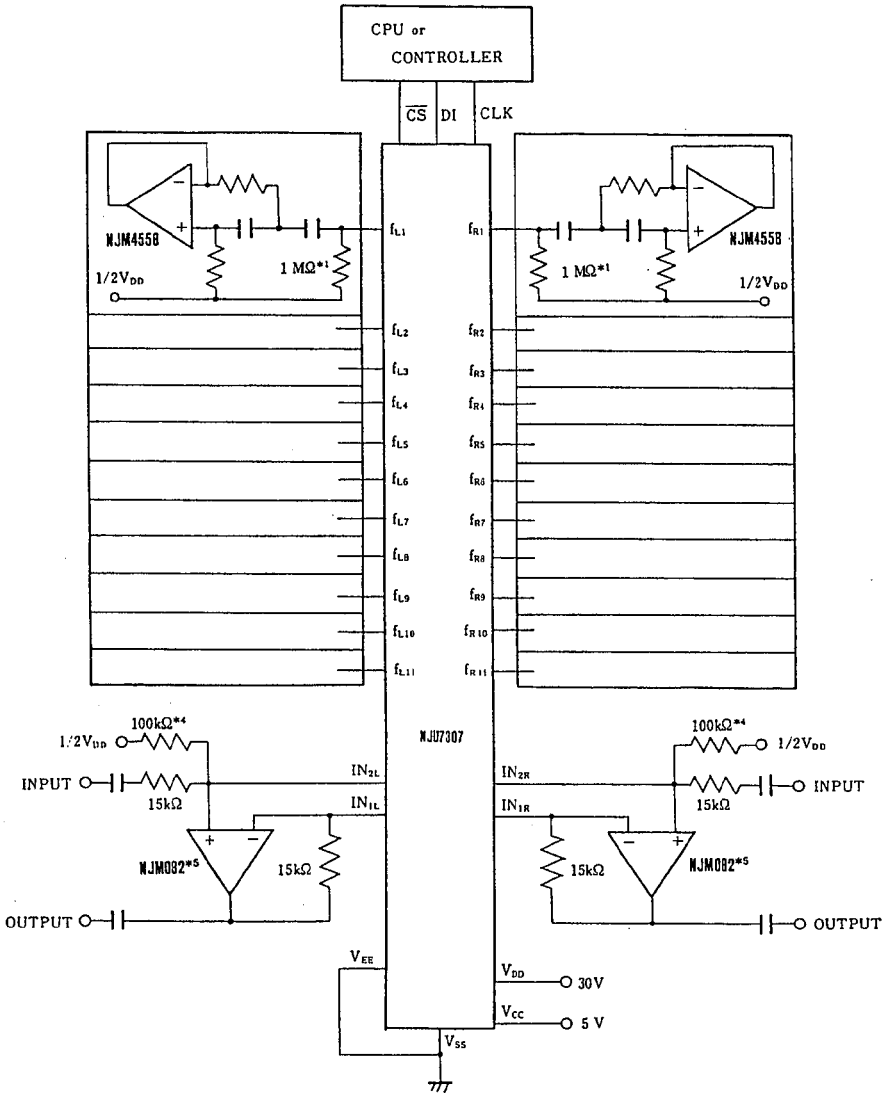


Circuit 3



■ APPLICATION CIRCUIT 1

< Single power supply operation >



*1) In order to reduce the pop-noise, connecting f_{L1}~f_{L11}, f_{R1}~f_{R11} to 1/2 V_{DD} by 1MΩ resistance is recommended.
*2) The best conditions for 3dB/step are as follows:
V_{DD} = 30V
OP-amp feedback resistance: 15kΩ.
Equivalent LC resonant impedance: 1kΩ
*3) TEST1 and TEST2 terminals are normally OPEN.
*4) In order to keep off noise input, connecting to 1/2 V_{DD} by 100kΩ resistance is recommended.
*5) J-FET input OP-AMP is recommended.

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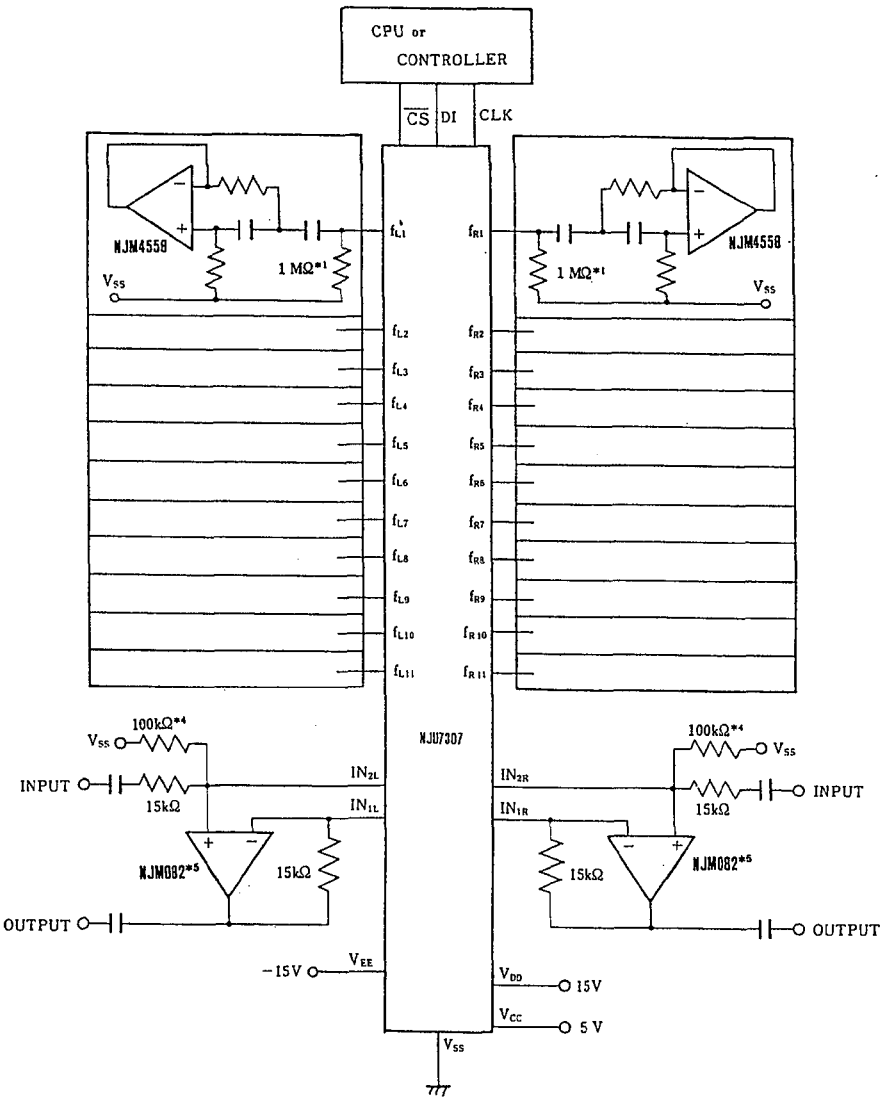
■ APPLICATION CIRCUIT 2

< Dual power supply operation >



*1) In order to reduce the pop-noise, connecting f_{L1}~f_{L11}, f_{R1}~f_{R11} to V_{SS} by 1MΩ resistance is recommended.
*2) The best conditions for 3dB/step are as follows:
V_{DD} = 15V, V_{EE} = -15V
OP-amp feedback resistance: 15kΩ.
Equivalent LC resonant impedance: 1kΩ
*3) TEST1 and TEST2 terminals are normally used as OPEN.
*4) In order to keep off noise input, connecting to 1/2 V_{DD} by 100kΩ resistance is recommended.
*5) J-FET input OP-AMP is recommended.

MEMO

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