ERICSSON

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PBA 3357/3
Dual Channel Complete Line Interface Circuit, DCLIC

Description

The PBA 3357/3 is a Dual Channel Complete Line Interface Circuit (DCLIC) manufactured in thick-film technology.

The PBA 3357/3 Dual CLIC consists of two Ericsson SLIC´s, two Combo 1 Codecs and all other necessary components to interface two seperate analogue extensions to the PCM highway.

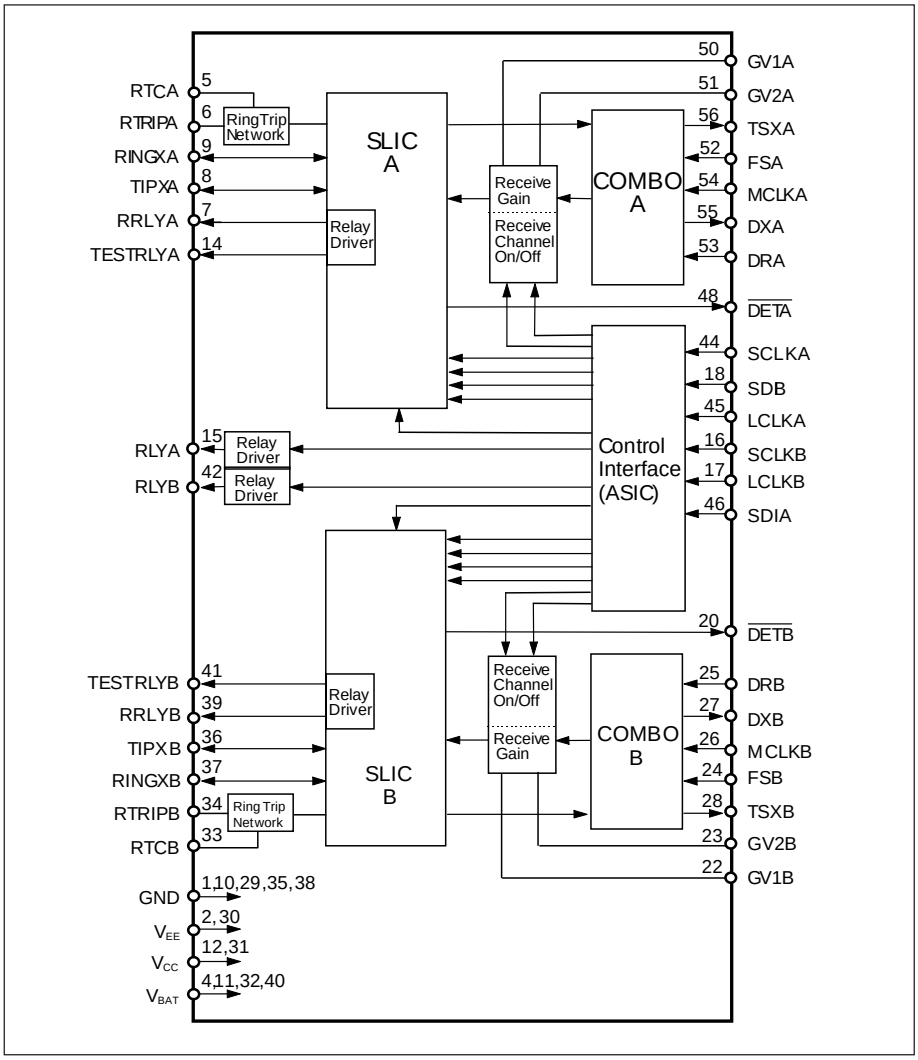

Figure 1: Block Diagram

Key Features

- Constant Current DC performance at V_{BAT}=-40,0 V I_{LDC}=min 17.3 mA at R_{LOOP}=1800 Ω
- Two Software programmable receive gain ranges: (-3.5/-7.0) or (0/-3.5) dBr. Software receive gain range is selectable via hardware wiring
- Simple serial control interface, 8 bit
- Controlled Power-on state: Open circuit, Receive channel off and all realys inactive
- Polarity reversal
- Receive channel can be turned off
- On-Hook Transmission
- Three relay drivers/line; a total of six relay drivers
- Terminating impedance Z_{TR}=200 Ω+ (680 Ω // 100 nF)
- Longitudinal balance; typ 60 dB
- Nominal V_{BAT}= - 48 V
- Few additional external componets needed
- Small physical size: 34.4 x 71.1 mm

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Temperature				
Storage temperature range	T_{stg}	-40	+125	°C
Power Supply				
Positive Supply voltage with respect to Ground (GND)	V_{CC}	-0,4	+6,5	V
Negative Supply voltage with respect to Ground	V_{EE}	-6,5	+0,4	V
Battery voltage with respect to Ground	V_{BAT}	-70	+0,4	V
Ring Relay Driver				
Relay Supply voltage	V_{RRLY}	V_{BAT}	V_{CC}	V
Current	I_{RRLY}		80	mA
Test Relay Driver				
Relay Supply voltage	V_{TRLY}	V_{BAT}	V_{CC}	V
Current	I_{TRLY}		80	mA
Additional Relay Driver				
Relay Supply voltage	V_{RLY}	-30	V_{CC}	V
Current	I_{RLY}		70	mA
TIPX and RINGX terminals				
Voltage (each terminal), Continous (with respect to GND)	V_{TA}, V_{RA}	-70	1	V
Voltage (each terminal), Pulse t_{ON} < 10 ms. t_{REP}>10 s, (Note 1)	V_{TA}, V_{RA}	-70	5	V
Voltage (each terminal), Pulse t_{ON} < 1 µs. t_{REP}>10 s, (Note 1)	V_{TA}, V_{RA}	-90	10	V
Voltage (each terminal), Pulse t_{ON} < 250 ns. t_{REP}>10 s, (Note 1)	V_{TA}, V_{RA}	-120	15	V
Current (each terminal)	I_{DCMET}	-105	105	mA

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Temperature					
Ambient temperature range, Operating	T_{amb}	0		+70	°C
Ambient temperature range, Test	T_{amb}		+23		°C
Power Supply					
Positive Supply voltage with respect to Ground (GND)	V_{CC}	+4,75	+5	+5,25	V
Negative Supply voltage with respect to Ground	V_{EE}	-5,25	-5	-4,75	V
Batteryvoltage with respect to Ground	V_{BAT}	-56	-48	-44	V

Electrical Characteristics

T_{amb} = 0 - 70 °C, V_{CC}= +5 V ± 5 %, V_{EE}=-5 V ± 5 %, V_{BAT}=-44 - -56 V, R_{LDC}= 600 Ω, Z_N=200 Ω+ (680 Ω//100 nF) See also fig 7

Parameter	Condition	Min	Typical	Max	Unit
Battery Feed Characteristics					
Line Current	$R_L \leq 1800\ \Omega$	18,0		28,0	mA
Line Current	R_L = 1800 Ω, V_{BAT}= -40V	17,3			mA
Line Voltage	$R_L = \infty\ \Omega$, V_{BAT}= -48 V	35		39	V
Battery Feed Characteristics, Polarity Reversad					
Line Current	$R_L \leq 1800\ \Omega$	-28,0		-18,0	mA
Line Current	R_L = 1800 Ω, V_{BAT}= -40V			-17,3	mA
Line Voltage	$R_L = \infty\ \Omega$, V_{BAT}= -48 V	-39		-35	V

Electrical Characteristics cont.

Parameter	Condition	Min	Typical	Max	Unit
Loop Current Detector					
Loop Resistance R_L	Active, $\overline{DET}$ output High ("1")	20			kΩ
Loop Resistance R_L	Stand-by, $\overline{DET}$ output High ("1")	20			kΩ
Loop Resistance R_L	Active, $\overline{DET}$ output Low ("0")			2,3	kΩ
Loop Resistance R_L	Stand-by, $\overline{DET}$ output Low ("0")			2,3	kΩ
Off hook Detection delay time	-			100	ms
Dial Pulse Distortion, *(Note 6)*	10 pulses/s, Period 1000 ± 100 ms, *(Note 2)*	-10	0	10	ms
Ring Trip Detector, *(Note 6)*					
Delay time from Off hook ringing to detection. DET from High to Low	R_L = 1800 Ω, U_{RG}= 60 V			150	ms
DET minimum output low, "0" time	-	20	30		ms
Ring Relay Driver					
On-state Voltage	I_{OL}= 25 mA	(V_{CC}-2,0)	(V_{CC}-1,8)		V
Test Relay Driver					
On-state Voltage	I_{OL}= 25 mA	(V_{CC}-2,0)	(V_{CC}-1,8)		V
Additonal Relay Driver					
On-state Voltage	I_{OL}= 25 mA	(V_{CC}-1,0)			V
Power Dissipation per Line	**V_{BAT} = - 48 V**				
Active (Off hook)	R_L= 500 Ω			1300	mW
Active (Off hook)	R_L= 0 Ω			1600	mW
Stand-By (On hook) *(Note 5)*	R_L ≥ 20 kΩ			360	mW
Active (On hook), *(Note 5)*	R_L ≥ 20 kΩ			400	mW
Gain, Absolute					
The absolute reference level at the 2-wire interface, 0 dBm0	P= 1mW, Z_{TR}= 200Ω+(680Ω//100nF) f= 1014 Hz		0,9008		V_{RMS}
Transmit (A-D), Li=0,0 dBr	f= 1014 Hz, Level: -10 dBm0	-0,3	0,0	+0,4	dB
Receive (D-A), Lo= 0,0 dBr	f= 1014 Hz, Level: -10 dBm0	-0,4	0,0	+0,3	dB
Receive (D-A), Lo= -3,5 dBr	f= 1014 Hz, Level: -10 dBm0	-3,9	-3,5	-3,2	dB
Receive (D-A), Lo= -7,0 dBr	f= 1014 Hz, Level: -10 dBm0	-7,4	-7,0	-6,7	dB
Receive (D-A) cancellation	f= 1014 Hz, Level: -10 dBm0			-50	dB
Attenuation / Frequency Distortion					
Transmit connection (A-D) (CCITT Q552 3.1.1.5)	Reference: f = 1014 Hz = 200-300 Hz	-0,3	0,0	-	dB
	f = 300-400 Hz	-0,3	0,0	+1,0	dB
	f = 400-600 Hz	-0,3	0,0	+0,75	dB
	f = 600-2400 Hz	-0,3	0,0	+0,35	dB
	f = 2400-3000 Hz	-0,3	0,0	+0,55	dB
	f = 3000-3400 Hz	-0,3	0,0	+1,5	dB
Receive connection (D-A) (CCITT Q552 3.1.1.5)	Reference: f = 1014 Hz				
	f = 200-400 Hz	-0,3	0,0	+1,0	dB
	f = 400-600 Hz	-0,3	0,0	+0,75	dB
	f = 600-2400 Hz	-0,3	0,0	+0,35	dB
	f = 2400-3000 Hz	-0,3	0,0	+0,55	dB
	f = 3000-3400 Hz	-0,3	0,0	+1,5	dB

Electrical Characteristics cont.

Parameter	Condition	Min	Typical	Max	Unit
Variation of Gain with Input Level, *(Note 7)*					
Transmit (A-D) and	Reference: f = 1014 Hz, Level -10 dBm0				
Receive (D-A) connection	Input level = -55 to -50 dBm0	-1,5	0,0	+1,5	dB
(CCITT Q552 3.1.1.4)	Input level = -50 to -40 dBm0	-0,5	0,0	+0,5	dB
	Input level = -40 to -3 dBm0	-0,3	0,0	+0,3	dB
	Input level = -3 to +3 dBm0	-0,5	0,0	+0,5	dB
	Input level = +3 dBm0,	-2,5	0,0	+2,5	dB
	V_{BAT}= - 44V R_L= 1800Ω				
Signal to Total Distortion, *(Note 7)*					
Transmit (A-D) connection	Li = 0 dBr				
(CCITT Q552 3.3.3)	Input level = -45 dBm0	19,9			dB
	Input level = -40 dBm0	24,9			dB
	Input level = -30 dBm0	32,9			dB
	Input level = -20 dBm0	35,0			dB
	Input level = -10 dBm0	35,0			dB
	Input level = 0 dBm0	35,0			dB
Receive (D-A) connection	Lo = 0 dBr				
(CCITT Q552 3.3.3)	Input level = -45 dBm0	19,9			dB
	Input level = -40 dBm0	24,9			dB
	Input level = -30 dBm0	32,9			dB
	Input level = -20 dBm0	35,0			dB
	Input level = -10 dBm0	35,0			dB
	Input level = 0 dBm0	35,0			dB
Receive (D-A) connection	Lo = -3,5 dBr				
(CCITT Q552 3.3.3)	Input level = -45 dBm0	18,5			dB
	Input level = -40 dBm0	23,2			dB
	Input level = -30 dBm0	31,2			dB
	Input level = -20 dBm0	34,4			dB
	Input level = -10 dBm0	35,0			dB
	Input level = 0 dBm0	35,0			dB
Receive (D-A) connection	Lo = -7,0 dBr				
(CCITT Q552 3.3.3)	Input level = -45 dBm0	14,5			dB
	Input level = -40 dBm0	19,5			dB
	Input level = -30 dBm0	28,8			dB
	Input level = -20 dBm0	33,8			dB
	Input level = -10 dBm0	35,0			dB
	Input level = 0 dBm0	35,0			dB
Idle Channel Noise, (CCITT Q552 3.3.2)*(Note 8)*					
Transmit (A-D) connection	Li = 0 dBr			-66	dBm0p
Receive (D-A) connection	Lo = 0, -3,5 or -7,0 dBr			-70	dBm0p
Power Supply Rejection Ratio (PSRR)					
V_{CC} to Analog Interface	f= 50 to 4000 Hz	35			dB
V_{EE} to Analog Interface	f= 50 to 4000 Hz	10			dB
V_{BAT} to Analog Interface	f= 50 to 4000 Hz	25			dB

Electrical Characteristics cont.

Parameter	Condition	Min	Typical	Max	Unit
Impedance					
Nominal Impedance, Z_{TR}	Z_{TR} = 200 Ω + (680 Ω // 100 nF)				
Return Loss	*Note 3*				
(CCITT Q552 2.1.1.2)	f= 300 Hz	14	30		dB
	f= 500 to 2000 Hz	18	35		dB
	f= 3400 Hz	14	30		dB
Longitudinal Balance, L-T	f= 300 to 600 Hz	40	60		dB
(CCITT Q552 2.2.2)	f= 600 to 3400 Hz	46	60		dB
Terminal Balance Return Loss, TBRL					
(CCITT Q552 3.1.8.1)	*Note 4*				
	f= 300 Hz	16	20		dB
	f= 500 to 2500 Hz	20	30		dB
	f= 3400 Hz	16	20		dB
Stability Balance Return Loss,SBRL					
Only applicable when Lo = -3,5 or -7 dBr	ZN="Worst Terminating condition encountered in normal operation"				
	Open Circuit, f = 200 to 3600 Hz	2,0			dB
	Short Circuit, f = 200 to 3600 Hz	2,0			dB
Outband Signalling					
Transmit (A-D) connection	Input level: -25 dBm0				
(CCITT Q552 3.1.6)	f= 4600 to 72000 Hz				
	In-band signal			-50	dBm0
Receive (D-A) connection, *(Note 7)*	Input level: 0 dBm0				
(CCITT Q552 3.1.7)	f= 300 to 3400 Hz				
	Out-band signal (f= 4600 - 72000 Hz)			-25	dBm0
Intermodulation					
	2nd or 3rd order, 4-tone, A-D			-41	dB
	2nd or 3rd order, 4-tone, D-A			-41	dB
Crosstalk					
Input Crosstalk	CCITT Q552 3.1.4.1 (far-end) FEXT			-70	dBm0
Output Crosstalk	CCITT Q552 3.1.4.2 (far-end) FEXT			-73	dBm0
Digital Inputs					
Input Low voltage	Inputs: SDI, SCLK, LCLK	0,0		0,8	V
	Other Inputs	0,0		0,6	V
Input High voltage	Inputs: SDI, SCLK, LCLK	2,0		V_{CC}	V
	Other Inputs	2,2		V_{CC}	V
Input Low current	Inputs: SDI, SCLK, LCLK	-20		+20	µA
	Other Inputs	-10		+10	µA
Input High current	Inputs: SDI, SCLK, LCLK	-20		+20	µA
	Other Inputs	-10		+10	µA

Electrical Characteristics cont.

Parameter	Ref fig	Symbol	Min	Typical	Max	Unit
Timing Specification						
Frequency of Master Clock, MCLK	2	$1/T_{PM}$	2,037	2,048	2,062	MHz
Width of Master Clock High	2	t_{WMH}	160			ns
Width of Master Clock Low	2	t_{WML}	160			ns
Rise time of Master Clock	2	t_{RM}			50	ns
Fall time of Master Clock	2	t_{FM}			50	ns
Delay time to valid Data from FS or MCLK, whichever comes later and Delay time from FS to Data output disabled	3	t_{DZF}	20		165	ns
Delay time from MCLK High to Data output Disabled	2	t_{DZC}	50		165	ns
Setup time from DR valid to MCLK, Low	3	t_{SDB}	50			ns
Hold time from MCLK Low to DR Invalid	3	t_{HBD}	50			ns
Holding time from BIT Clock Low to the Frame Sync (FS)	3	t_{HBF}	0			ns
Setup time from Frame Sync to BIT Clock	3	t_{SFB}	80			ns
Hold time from 3rd period of BIT Clock Low to Frame Sync (FS)	3	t_{HBFI}	100			ns
Delay time from MCLK High to Data valid	2	t_{DBD}	0		180	ns
Setup time from FS to MCLK Low	2	t_{SF}	80			ns
Hold time from FS Low to MCLK Low	2	t_{HF}	100			ns
Delay time TSX Low	2	t_{XDP}			140	ns
Propagation Delay	4	t_{pLH}			15	ns
Min. Setup time SDI-SCLK	4	t_{SDS}	5			ns
Min. Hold time SCLK-LCLK	4	t_{hSL}	5			ns
Hold time LCLK-SCLK	4	t_{hLS}	5			ns
Min. Hold time, SCLK-SDI	4	t_{hSD}	5		200	ns

Notes

1. Requires DBAT; see Figure 6.
2. Dial Pulse Distortion at the $\overline{DET}$ output. Pulse tone: 8-14 pulses/s, 40 to 77 % duty factor for in-out application of a external resistance (200 - 1800 Ω) on the two-wire terminal.
3. Rising log scale from 14 dB @ 300 Hz up to 18 dB @ 500 Hz and falling log scale from 18 dB @ 2000 Hz down to 14 dB @ 3400 Hz.
4. Rising log scale from 16 dB @ 300 Hz up to 20 dB @ 500 Hz and falling log scale from 20 dB @ 2000 Hz down to 16 dB @ 3400 Hz.
5. Power dissipation is measured for both channels at the same time and divided by two.
6. The state during the pause of the ringing cadence or pulse dialling shall be active.
7. At V_{BAT} = -44 V and R_{LDC} = 1800Ω the SLIC has start to saturate. This will effect some transmission parameters, for high signal levels.(> -10dBm0).
8. The noise increase when the saturation guard becomes active arround RLDC ≥1400 Ω but is still better than CCITT Q552.3.3.2..

Reference Figures

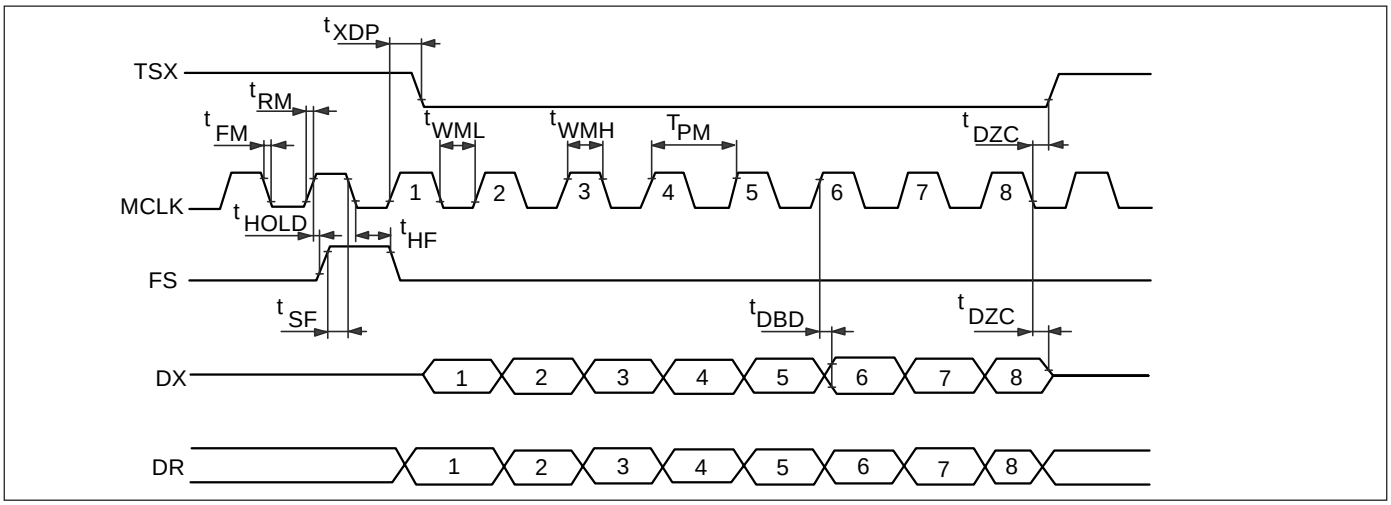

Figure 2. Short Frame Sync Timing diagram.

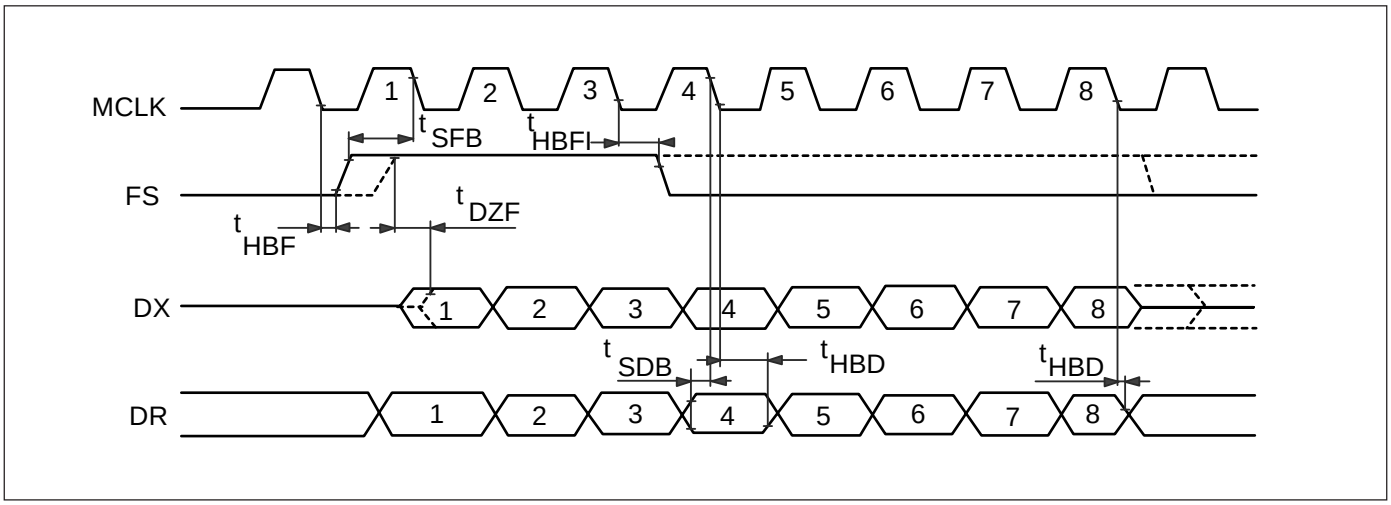

Figure 3. Long Frame Sync Timing diagram.

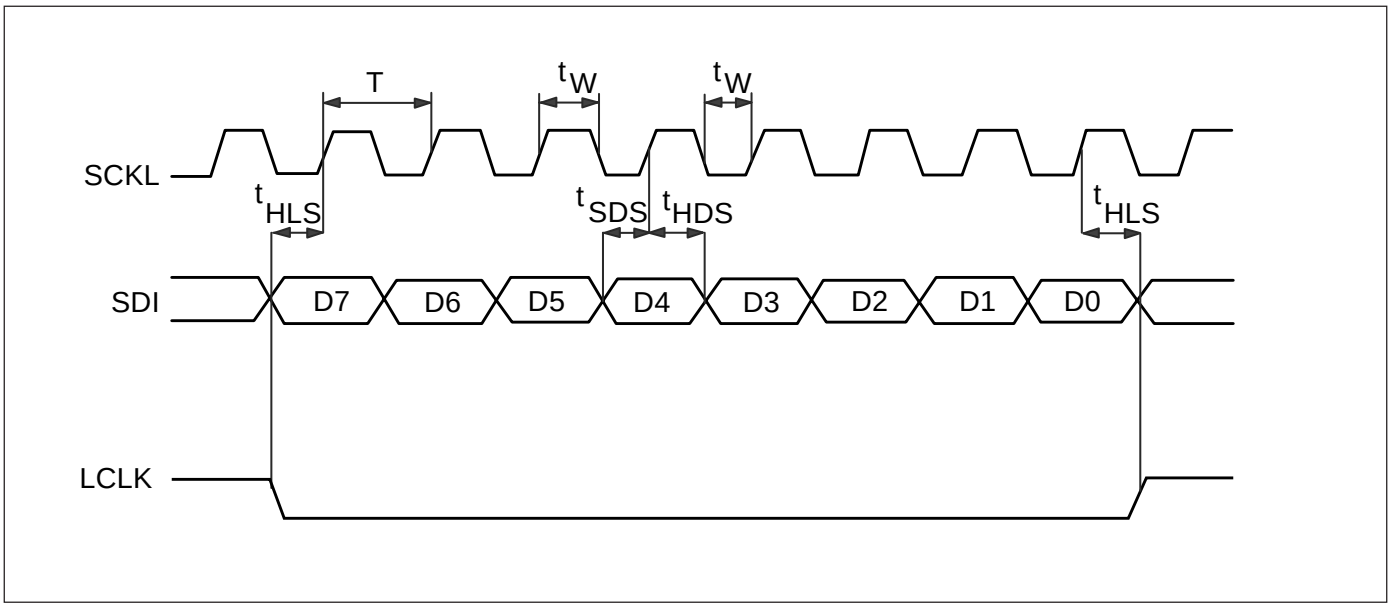

Figure 4. Control Timing diagram.

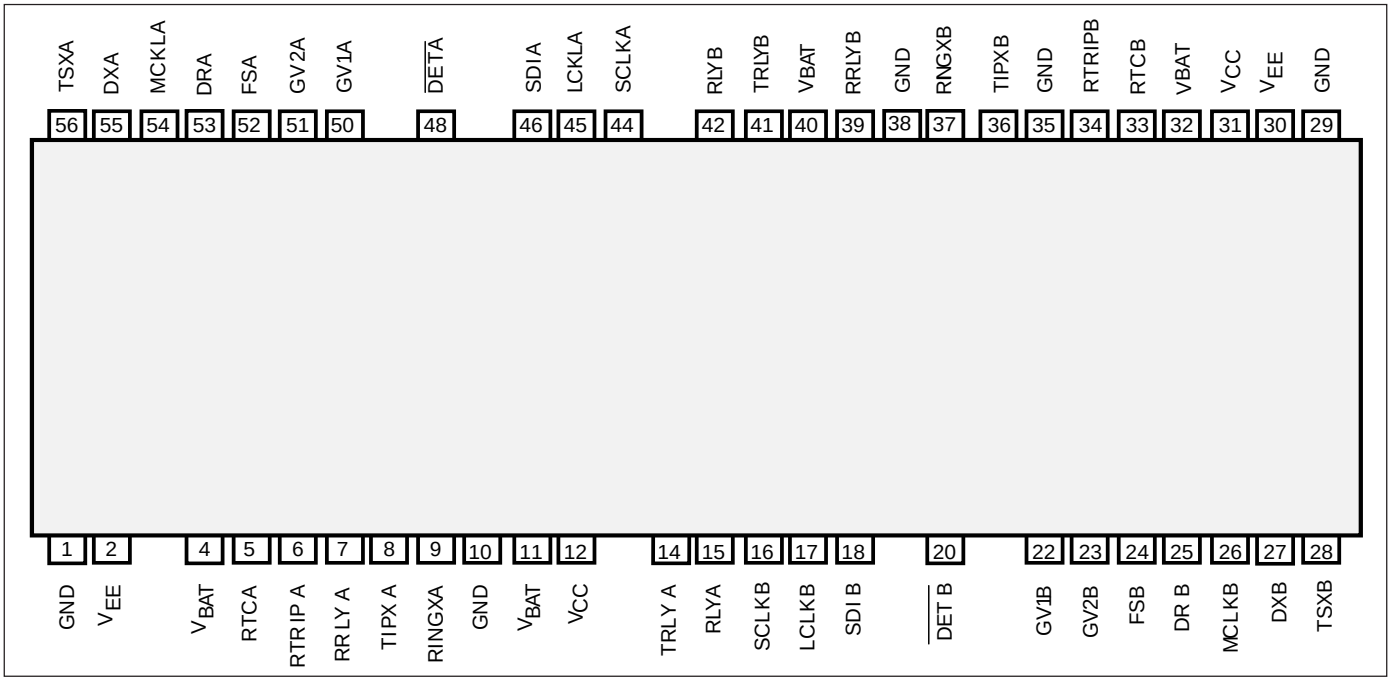

Figure 5. Pin-configuration, 56 pin DIL.

Pin Description

Pin	Symbol	Description
1	GND	Ground.
2	V_{EE}	Negative Supply Voltage, - 5V, for the CLIC.
3		Omitted Pin.
4	V_{BAT}	Battery Voltage, - 48 V to the CLIC.
5	R_{TC}	A ring Trip filter Capacitor input for Channel A. For standard performance of the CLIC, leave the pin open.
6	RTRIP A	Ring Trip network input for Channel A. Connect to the resistor RRT A. The resistor RRT A causes a voltage drop when Off-hook occurs during ringing. The voltage will cause a change of state in $\overline{\text{DET A}}$.
7	RRLY A	Ring Relay driver output for Channel A. The output is Open-collector, with a Kick-back diode included, designed to be connected to a negative voltage.
8	TIPX A	Tip lead input for Channel A to the CLIC from the subscriber line (two-wire).
9	RINGX A	Ring lead input for Channel A to the CLIC from the subscriber line (two-wire).
10	GND	Ground.
11	V_{BAT}	Battery Voltage, - 48 V to the CLIC.
12	V_{CC}	Positive Supply Voltage, + 5V, for the CLIC.
13		Omitted pin.
14	TRLY A	Test Relay driver output for Channel A. The output is Open-collector, with a Kick-back diode included, designed to be connected to a negative voltage.
15	RLY A	Additional Relay driver output for Channel A. The output is Open-collector, with a Kick-back diode included, designed to be connected to a negative voltage.
16	SCLK B	Serial Clock for Channel B. Clocks data into the shift-register on low-to-high transitions (edge)
17	LCLK B	Latch Clock for Channel B. Latches the data in the shift-register out on the eight parallell output bits on low-to-high transition (edge).
18	SDI B	Serial Data Input for Channel B.
19		Omitted pin.
20	$\overline{\text{DET}}$ B	Detector output for Channel B. The output is a Open-collector with internal pull-up resistor to V_{CC}.

Pin Description cont.

Pin	Symbol	Description
21		Omitted pin.
22	GV1 B	Gain Value for Channel B. For a receive gain of 0 to -3,5 dBr, GV1 and GV2 are connected togehter. For a receive gain of -3,5 to -7,0 dBr, GV1 and GV2 shall be left open.
23	GV2 B	see GV1 B.
24	FS B	Frame Sync for Channel B; Transmit and Receive.
25	DR B	PCM Receive Data Input for Channel B.
26	MCLK B	Master Clock for Channel B.
27	DX B	PCM Transmit data Output for Channel B; Tri-state.
28	TSX B	Time Slot for Channel B; Open-drain. Output pulse low during encoding.
29	GND	Ground.
30	V_{EE}	Negative Supply Voltage, - 5V, for the CLIC.
31	V_{CC}	Positive Supply Voltage, + 5V, for the CLIC.
32	V_{BAT}	Battery Voltage, - 48 V to the CLIC.
33	RTC B	Ring Trip filter Capacitor input for Channel B. For standard performance of the CLIC, leave the pin open.
34	RTRIP B	Ring Trip network input for Channel B. Connect to the resistor RRT B. The resistor RRT B causes a voltage drop when Off-hook occurs during ringing. The voltage will cause a change of state in $\overline{\text{DET}}$ B.
35	GND	Ground.
36	TIPX B	Tip lead input for Channel B to the CLIC from the subscriber line (two-wire).
37	RINGX B	Ring lead input for Channel B to the CLIC from the subscriber line (two-wire).
38	GND	Ground.
39	RRLY B	Ring Relay driver output for Channel B. The output is Open-collector, with a Kick-back diode included, designed to be connected to a negative voltage.
40	V_{BAT}	Battery Voltage, - 48 V to the CLIC.
41	TRLY B	Test Relay driver output for Channel B. The output is Open-collector, with a Kick-back diode included, designed to be connected to a negative voltage.
42	RLY B	Additional Relay driver output for Channel B. The output is Open-collector, with a Kick-back diode included, designed to be connected to a negative voltage.
43		Omitted pin.
44	SCLK A	Serial Clock for Channel A. Clocks data into the shift-register on low-to-high transitions (edge).
45	LCLK A	Latch Clock for Channel A. Latches the data in the shift-register out on the eight parallell output bits on low-to-high transition (edge).
46	SDI A	Serial Data Input for Channel A.
47		Omitted pin.
48	$\overline{\text{DET}}$ A	Detector output for Channel A. The output is a Open-collector with internal pull-up resistor to V_{CC}.
49		Omitted pin.
50	GV1 A	Gain Value for Channel A For a receive gain of 0 to -3,5 dBr, GV1 and GV2 are connected togehter. For a receive gain of -3,5 to -7,0 dBr, GV1 and GV2 shall be left open.
51	GV2 A	see GV1 A.
52	FS A	Frame Sync for Channel A Transmit and Receive.
53	DR A	PCM Receive Data Input for Channel A.
54	MCLK A	Master Clock for Channel A.
55	DX A	PCM Transmit data Output for Channel A; Tri-state.
56	TSX A	Time Slot for Channel A; Open-drain. Output pulse low during encoding.

Functional Description and Applications Information

General

The PBA 3357/3 is a Dual Complete Line Interface Circuit. Only a small number of additional external components are required.

In case of a requirement for test of the subscriber line and system, two relays per line will be needed.

In figure 6 they are relay RL1, RL2, RL4 and RL5. One ring relay per channel will be needed to apply the ring signal to the subscriber line (RL3 and RL6).

Ring Trip

The ring trip function has been designed to the following conditions:

- Unbalanced ringing super-imposed on the battery voltage.
- Ring generator data:
  Output typical 75 VRMS
  min 60 VRMS, max 90 VRMS
  Impedance min 20 Ω, max 40 Ω
  Frequency typ 25 ± 3 Hz
- Loop Resistance <1800 Ω
- On-hook impedance @ 25 Hz (Ringing signal) is 7,5 to 18 k Ω

One, two or three POT's (Plain Ordinary Telephone or equal) in parallell on each line.

In order to sense off-hook during ringing, two resistors per line is required; R_{RT} and R_{RG}.

They should be 240 Ω, min 2 W.

Note: R_{RT} and R_{RG} must fulfill CCITT k20. Lightning Surge.

The CLIC state during the pause of the ringing cadence shall be active due to longer stabilization time in stand-by state.

Receive Gain Pins (GV1, GV2)

The receive gain can have three different values; 0, -3,5 or -7,0 dBr.

If the pins GV1 (pin 23, 50) and GV2 (pin 22, 51) are shorted, the low gain equals -3,5 dBr and the high gain equals 0,0 dBr.

If the pins GV1 and GV2 are left open, the gain values are -7,0 dBr and -3,5 dBr respectively. High and low gain is selected with input data to the ASIC.

Over Voltage Protection

The CLIC must be protected against surge voltages and power cross conditions.

In figure 6, the line resistors with fuse function, R_{F1} and R_{F2}, PTC:s, together with the voltage clamping device OVPD form the secondary protection. The PTC acts as a resettable fuse for non destructive power contact.

The protection network in figure 6 is designed to meet requirements in CCITT k20, Table 1.

If overvoltages with a magnitude higher than CCITT k20, Table 1, is expected, a primary protection is required. A Gas Discharge Tube is recommended.

ZBAT protects against overvoltage on VBAT and ensure that the OVP-device can trigger if the -48V should not be connected

The capacitor C_G Between ground and the OVP-device should be as close as possible to the OVP-device.

The OVP-device ground connector should be as close as possible to the CLIC ground connector.

Grounding

The "grounds"; GND's shall be tied together as close as possible; i.e. in one point on the PCB.

The different ground points on the linecard shall also be connected together into one point.

GND should be distributed with a very low impedance as a ground plane or a grid in order to sink the overvoltage current with low voltage drops between the connectors of the component.

Power-up State

At Power-up, the CLIC Control Circuit makes a reset and put the CLIC in its power-up state.The power-up state i Open Circuit and no Relay Drivers activated. The CLIC will remain in this state until programmed else by sending the inverse of the desired command word (see table page 11) followed by the desired command word. Example: To set the CLIC in active state with command word 'C8', the inverse of 'C8', '37', followed by 'C8' has to be sent. Once this two word sequence has been sent the CLIC is enabled to take one-word command.

Since all flip-flops in the circuit is initually set to zero, it is recommended to avoid to start with 'FF', which is the only single word enable to open the circuit.

TTL or CMOS use

The integrated circuits of the interface are LSTTL or CMOS. CMOS use need specific attention during the board insertion under back panel power on condition.

Power-up Sequence

The optimum power-up sequence, in order to avoid any problem, is: Ground, V_{BAT} (-48 V), V_{EE} (- 5 V) and V_{CC} (+ 5 V) in stated order.

If it is not possible to control the power-up sequence , the following design must be used:

1. **6,2 V Zener diode D_{VCC}, D_{VEE2}:**

   The zener diodes will protect all +5 V and -5 V IC´s on the linecard from overvoltage if Ground being connected after V_{CC}/V_{EE} and VBAT.in the power-up sequence.

   This due to the voltage dividing between the decoupling capacitors on the line card.

2. **Schottky diode D_{VEE1}:**

   The schottky diode, with low forward voltage drop, will protect all -5 V IC's on the linecard from reverse voltage if Ground is connected after V_{EE} and V_{BAT}.in the power-up sequence.

   This due to the voltage dividing between the decoupling capacitors on the line card.

3. **Resistor R_{VEE}**:

   The resistor will reduce the charging current into the decoupling capacitors and limit dV/dt.

4. **RC-network R_{BAT} and C_{BAT}:**

   To protect the V_{BAT} - pin from being exposed to a faster dV/dt - rate than 4 V / µs when connecting to V_{BAT}.

   This can be achieved by using a RC-filter with the time constant (τ) formed by a 5,1 Ω resistor (R_{BAT}) and a 0,47 µF capacitor (C_{BAT}).

To ensure a fail-safe function in the system, it is recommended to use resistors with some type of fuse function and a Fuse on V_{CC} connection in series with the power supplies to avoid resulting failures in the system.

1.

Control Data

Each channel of PBA 3357/3 has an ASIC which controls all line functions with a 8 bit serial word

Relay Driver	Test Relay Driver	Detector Select	Gain Control	SLIC Operation			Receive Control	Function	
*	*	*	*	*	*	*	1	Receive Channel Off	
*	*	*	1	*	*	*	0	High Gain	
*	*	*	0	*	*	*	0	Low Gain	
*	0	*	*	*	*	*	*	Test relay driver	Active (On)
*	1	*	*	*	*	*	*	Test relay driver Inactive (Off)	
0	*	*	*	*	*	*	*	Relay driver Active (On)	
1	*	*	*	*	*	*	*	Relay driver Inactive (Off)	
								Operating State	**Active Detector**
*	*	X	*	0	0	0	*	Open Circiut	None
*	*	X	*	0	0	1	*	Ring Relay driver Active (Ringing)	Ring Trip
*	*	0	*	1	0	0	*	Active	Loop Current
*	*	1	*	1	0	0	*	Active	Ground Key
*	*	0	*	1	0	1	*	Stand by	Loop Current
*	*	1	*	1	0	1	*	Stand by	Ground Key
*	*	0	*	0	1	0	*	Tip open	Loop Current
*	*	X	*	0	1	1	*	No Function	None
*	*	0	*	1	1	0	*	Active, Polarity Reversed	Loop Current
*	*	1	*	1	1	0	*	Active, Polarity Reversed	Ground Key
*	*	0	*	1	1	1	*	Stand by, Polarity Reversed	Loop Current
*	*	1	*	1	1	1	*	Stand by, Polarity Reversed	Ground Key
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Sequence of Data Input (SDI)	

Comments: 1) X = Do not care 2) * = Function specified elsewhere in the table.

The CLIC will remain in its power-up state until programmed by sending the inverse of the desired command word followed by the desired command word. *Example:* To set CLIC in active state with command 'C8', the inverse of 'C8', '37', followed by 'C8' has to be sent. To set CLIC in standby state with command 'CA', the inverse of 'CA', '35', followed by 'CA' has to be sent. Once this has been done the CLIC is enabled to take single-word command. The Power-up state is Open Circuit and no Relay Driver activated.

Example on Control Input:

HEX Word	Binary Word	Function
C8	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 1 1 0 0 1 0 0 0 C 8	Relay Driver Off (Bit D_7) Testrelay Driver Off (Bit D_6) Active, Detector = Loop Current (Bit D_3, D_2, D_1 and D_5) Receive Channel On, Low Gain (Bit D_0 and D_4)
D2	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 1 1 0 1 0 0 1 0 D 2	Relay Driver Off (Bit D_7) Testrelay Driver Off (Bit D_6) Ringing, Detector = Ring Trip (Bit D_3, D_2, D_1) Receive Channel On, High Gain (Bit D_0 and D_4)

Note: BIT D_7 is sent first, BIT D_0 is sent last.

Application Reference Figures

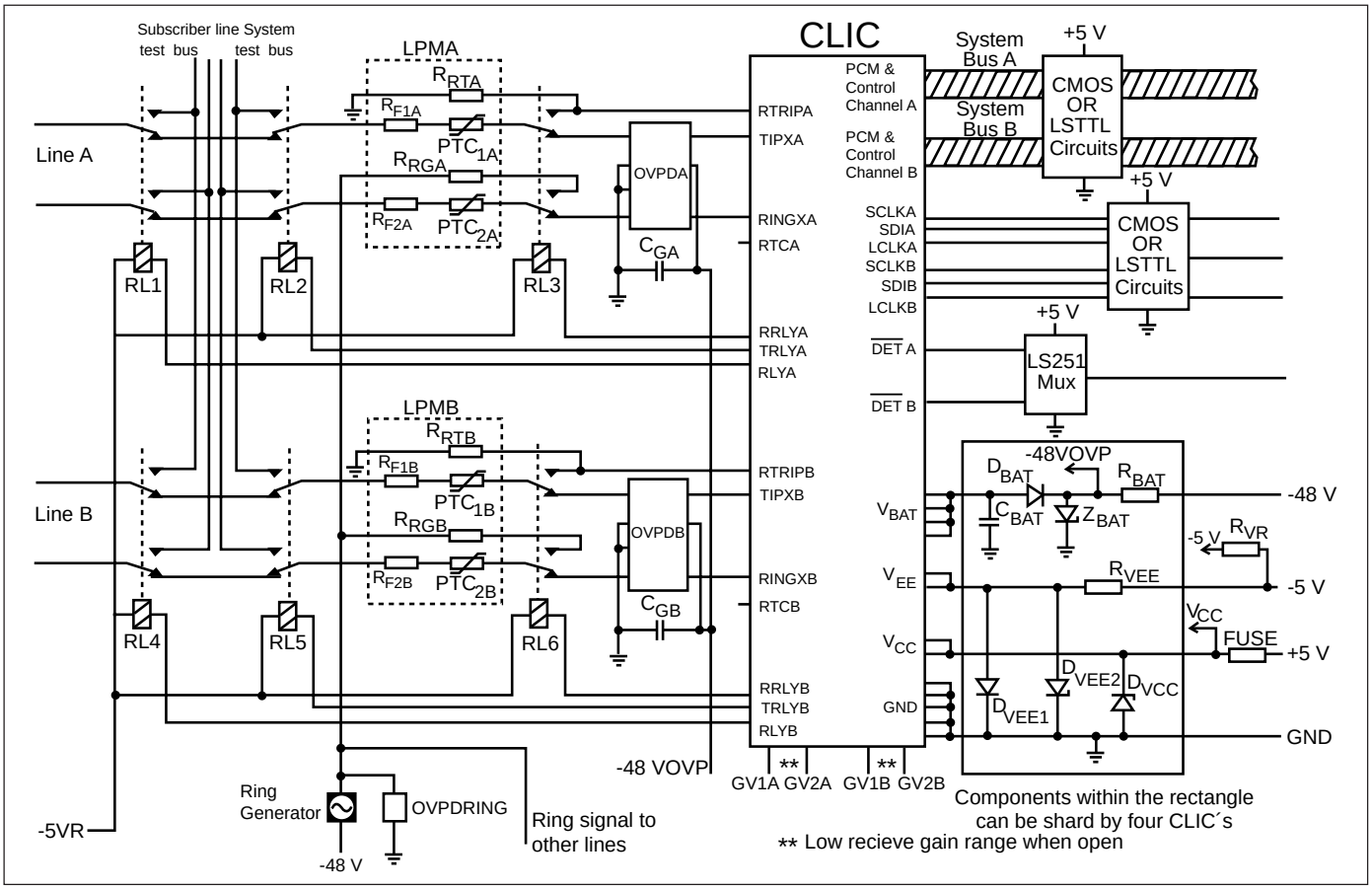

Figure 6. Typical Application for Dual CLIC PBA 3357/3 on a 16 Lines Line Card.

Denotation	Type of Component; requirements, name etc
OVPDA, OVPDB	TISP R3612
OVPDRING	Transient supressor, Zener diode type, 200V
D_{VCC}, D_{VEE2}	Zener diode 6,2 V 1 W; BZX 85 C6V2
D_{VEE1}	Schottky diode 1N5818, 1N5820
D_{BAT}	Diode 1N4004 or similar
Z_{BAT}	Transient supressor, BZW04-58 or SA58A
RL1-RL6	Relay; 9 V type
LPMA, LPMB[1)]	PBR 522 01/1 2 x 40 Ω, matched, Line Resistor with PTC and Two 240 Ω resistors.
R_{VEE}, R_{VR}	1,0 Ω, ± 20 %, 0,25 W (with fuse function)
R_{BAT}	5,1 Ω, ± 20 %, 1 W (with fuse function, max 4 DualCLIC's)
C_{BAT}	0,47 µF, ± 20 %, 100 V. Recommended types: 1. Ceramic, X7R, with low voltage coefficient; max 15 % at 50 V_{DC} 2. Metallized polyester film (stacked MKT); Prefered
C_{GA}, C_{GB}	0,22 µF, ± 20 %, 100 V. Recommended types: same as C_{BAT}
Fuse	Fuse Ω 1A depending on the power supply current Ir the interface circuits

Application Reference Figures cont.

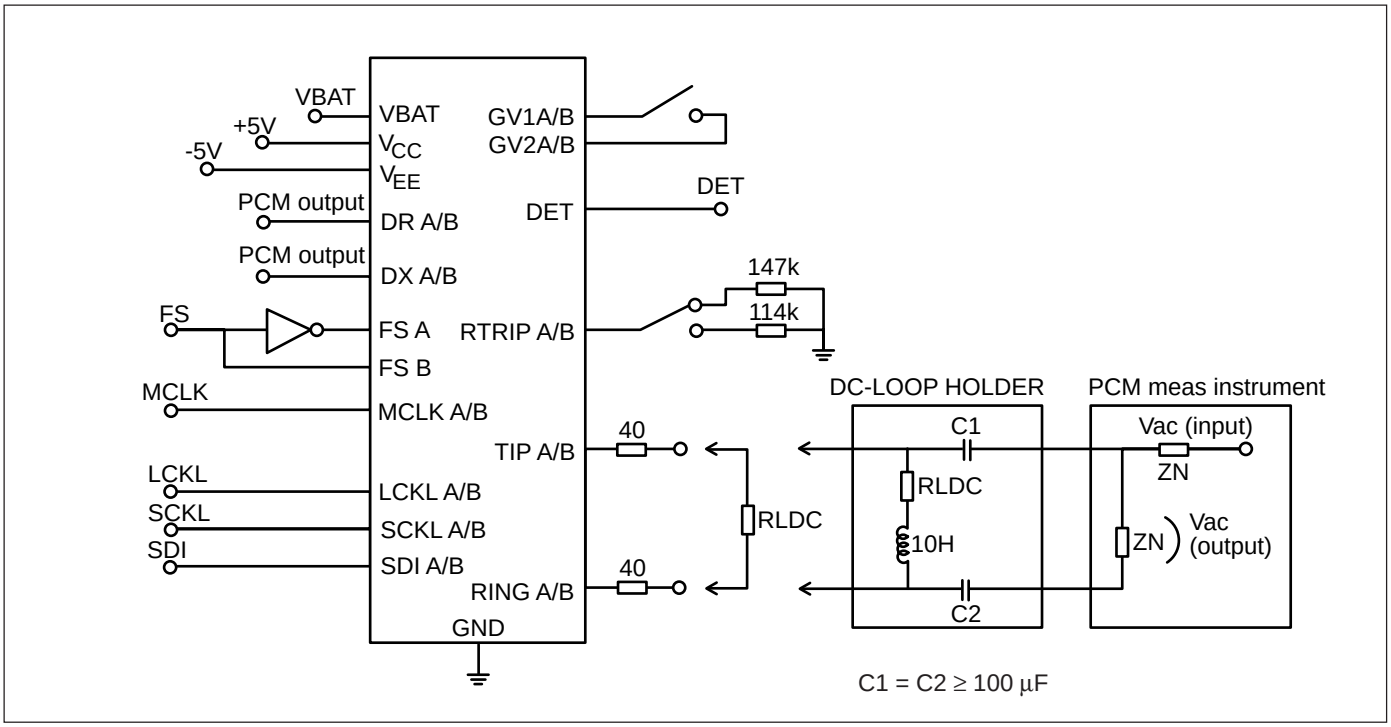

Figure 7. Reference diagram for Transmission Measurement.

Mechanical Outline

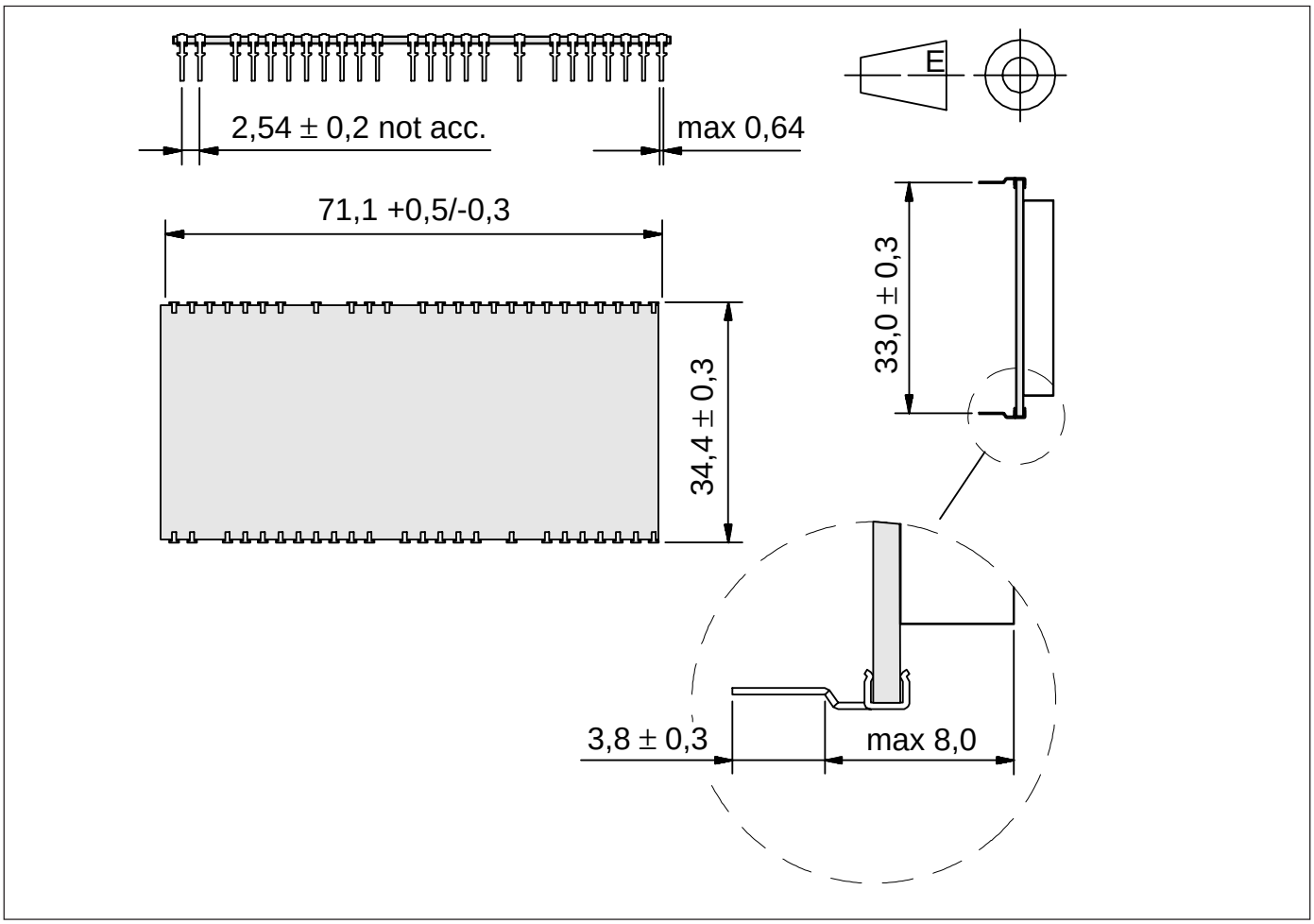

Figure 8. Mechanical outline.

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Ericsson Components AB
S-164 81 Kista-Stockholm, Sweden
Telephone: (08) 757 50 00