Application Note

PBL 3762A Subscriber Line Circuit As DID Trunk Interface

Direct Inward Dialing (DID) is an operational feature available on some private automatic branch exchanges (PABX) that provides for direct dial access to PABX stations from public switched network stations. Direct Inward Dialing requires transmission of address signals from the serving central office to the PABX. The PABX detects central office seizure by application of a dc resistance of maximum 2450 Ω and recognizes idle state as loop resistance exceeding 30 kΩ. The PABX communicates control of incoming address signaling and answer supervision by tip-ring polarity reversals. The reader is referred to Electronic Industries Association standard EIA/TIA-464-A for a description of the One-Way Direct Dialing (DID) Service PBX-CO Trunk Interface.

The PBL 3762A Subscriber Line Interface Circuit can be employed in DID trunk interfaces in addition to its application in On-Premises (ONS) and Off-Premises (OPS) station line interfaces. Applying the same device in these three types of port groups leads to great design commonality, potentially allowing a common printed circuit board design. Further, with the addition of necessary circuitry, the required port type could be configured under software control. This would eliminate the need to manufacture, test, stock, service, etc. three different assemblies. The SLIC design approach reduces required PCB area, reduces weight, decreases component height requirements, reduces the number of components to buy and stock, as well as simplifies the production testing compared to discrete transformer hybrid designs.

Design Example

The following text describes a step by step procedure on how to apply the PBL 3762A SLIC in a DID trunk interface. The design example is for μ-law compatible equipment, but the procedure can easily be modified to suit other applications.

General Specifications

- Applicable parts of EIA/TIA-464-A and FCC part 68

Design Input Data

(For calculation of components surrounding the PBL 3762A SLIC and interface components to the National TP3054 combination CODEC/filter.)

- Battery voltage, V_{Bat}: - 48 V
- Tip-ring short circuit SLIC power dissipation, P_{Sh}: max. 1.5 W
- Two-wire impedance, Z_{TR} (programmed by Z_T): 900 Ω, resistive
- Feed resistance (programmed by R_{DC1} and R_{DC2}): 16.2 mA delivered into a 2265 Ω loop by the PBL 3762A 50 V apparent battery
- Off hook loop current detection level, I_{LThoff}: 10 mA
- Transmit gain, V_O/V_{TR} (two-wire to four-wire gain): 0 dBm0, 1.0 kHz transmit level at the two-wire port is -3.0 dBm or 0.6716 V_{Rms} across 900 Ω. The corresponding output level from the CODEC/filter transmit amplifier, V_O is 1.2276 V_{Rms}.
- Receive gain, V_{TR}/V_{RX} (four-wire to two-wire gain): 0 dBm0, 1.0 kHz receive level at the two-wire port is +3.0 dBm or 1.3401 V_{Rms} across 900 Ω. The corresponding output level from the CODEC/filter (pin 3, VFRO), V_{RX}, is 1.2276 V_{Rms}.
- Balance network, Z_B: design for tip-ring compromise impedance of 900 Ω, resistive.
- Ac-dc separation capacitors C_{DC} and C_{HP}: calculate C_{DC} for a 3 dB breakpoint at 2.3 Hz and C_{HP} for a 3 dB breakpoint at 48 Hz.

Calculations

1. Two-wire Impedance, Z_{TR}

The two-wire impedance presented by the SLIC to the line, Z_{TR}, is calculated for a two-wire line impedance $Z_L = R_L = R_{TR} =$ 900 Ω. From the PBL 3762A data sheet:

$$Z_{TR} = R_{TR} = \frac{R_T}{1000} + 2 \bullet R_F \qquad (1)$$

which yields:

$$R_T = (R_{TR} - 2 \bullet R_F) \bullet 1000$$

where:

$Z_{TR} = R_{TR}$ is the DID interface tip-ring impedance

R_F = the line resistor

R_T = the SLIC two-wire impedance programming resistance

with:

R_F = 40 Ω

R_{TR} = 900 Ω

R_T = 820 kΩ

2. Feed Resistance

In the active state (C1, C2 = 0, 1) the PBL 3762A SLIC emulates a resistive feed circuit with an apparent battery voltage of 50 V according to

$$I_{Ldc} = \frac{50}{R_{Feed} + R_{Ldc} + 2 \bullet R_F} \qquad (2)$$

$$R_{Feed} = \frac{(R_{DC1} + R_{DC2})}{50} \qquad (3)$$

where:

I_{Ldc} is the dc loop current

R_{Ldc} is the dc loop resistance

R_{Feed} is the emulated feed resistance

R_{DC1} and R_{DC2} are the feed bridge programming resistance

R_F is the line resistor

Solving (2) for the feed resistance yields:

$$R_{Feed} = \frac{50}{I_{Ldc}} - R_{Ldc} - 2 \bullet R_F$$

with:

R_{Ldc} = 2265 Ω

I_{Ldc} = 16.2 mA

R_F = 40 Ω

R_{Feed} = 741.4 Ω

This feed resistance would result in a short circuit loop current I_{Lsh} of:

$$I_{Lsh} = \frac{50}{R_{Feed} + 2 \bullet R_F} = 60.9 \text{ mA}$$

The short circuit SLIC power dissipation P_{Sh} can be calculated from:

$$P_{Sh} = I_{Lsh} \bullet (48 - I_{Lsh} \bullet 2 \bullet R_F) + P_{OnAct} \quad (4)$$

which with I_{Lsh} = 60.9 mA and P_{OnAct} = 0.16 W yields:

P_{Sh} = 2.79 W

Maximum allowable SLIC dissipation is 1.5 W which indicates that the short circuit loop current needs to be limited. Calculate the maximum permissible short circuit loop current from (4) with P_{Sh} = 1.5 W. The resulting short circuit current is:

I_{Lsh} = 29.4 mA.

Note that a direct short circuit across the two-wire port is not a normal operating state. Even with near zero wire resistance, the terminating central office equipment adds resistance to the loop. At a loop resistance of e.g. 100 Ω the SLIC power dissipation would be reduced to 1.4 W and at 200 Ω reduced to 1.3 W. If it is desirable to increase the short loop current and thereby the short loop power dissipation, this can be achieved by incorporating a heatsink.

Knowing the required feed resistance from (2) permits the sum of R_{DC1}+R_{DC2} to be calculated from (3):

$$R_{DC1} + R_{DC2} = R_{Feed} \bullet 50 = 741.4 \bullet 50 = 37.07 \text{ k}\Omega$$

The division between R_{DC1} and R_{DC2} is determined by the described power dissipation limit for a short circuited loop. To limit the short circuit loop current I_{Lsh} to 29.4 mA, a diode, D_3, is connected from ground to the junction of R_{DC1} and R_{DC2}. As the voltage at the cathode of the diode becomes increasingly negative with larger loop currents, a point will be reached when the diode starts to conduct and the voltage is clamped to one diode drop, V_d thereby limiting the current flowing out from the summing node, RSN. The loop current is 1000 times the current flowing out of the receive summing node, RSN. Thus, R_{DC1} can be calculated from

$$R_{DC1} = \frac{V_d \bullet 1000}{I_{Lsh}} = 17.00 \text{k}\Omega$$

(select standard 1% value 16.9kΩ) where V_d is the voltage drop across the conducting diode D_3, approximately 0.5 V.

R_{DC2} is then 37.07 kΩ - 17.0 kΩ = 20.07 kΩ (select standard 1% value 20.0 kΩ).

3. Saturation Guard Reference Voltage Programming Resistor, R_{SG}

The PBL 3762A SLIC has a monitoring circuit, which measures the dc voltage between tip and ring. When this voltage reaches a programmable value, V_{SGRef}, the saturation guard is activated and will start to limit the dc loop voltage. With increasing loop resistances the line voltage will continue to increase somewhat beyond V_{SGRef}, but will ultimately be limited to an open circuit voltage, V_{TROpen}, set by R_{SG} according to:

$$V_{TROpen} = 20.4 + \frac{4.29 \bullet 10^5}{R_{SG}}$$

For V_{Bat} = -48 V the tip to ring voltage may be permitted to increase to 40 V without causing a 3.1 V_{Peak} metallic line voltage to be distorted by the SLIC. From the expression above with V_{TROpen} = 40 V, R_{SG} can be calculated to 21.9 kΩ (select standard 22 kΩ ± 5 % resistor).

With the R_{SG} value determined, the loop voltage at which the saturation guard will activate, V_{SGRef}, can be calculated:

$$V_{SGRef} = 15.5 + \frac{5 \bullet 10^5}{R_{SG}} = 38.2 \text{ V}$$

The tip to ring dc voltage at the maximum DID loop resistance is

$$V_{TR} = 2265 \bullet 16.2 \bullet 10^{-3} = 36.7 \text{ V}$$

i.e. the saturation guard will not activate and interfere within the normal DID loop range.

4. Ac - dc separation capacitor C_{DC}

The C_{DC} capacitance value is calculated from

$$C_{DC} \bullet \frac{R_{DC1} \bullet R_{DC2}}{R_{DC1} + R_{DC2}} = T$$

where:

T = 70 ms (f_{DC} = 2.3 Hz)

which yields:

$C_{DC} = 7.5 \bullet 10^{-6}$ µF (select 8.2 µF, 10 V)

5. Off-hook Loop Current Detection Level Programming Resistor, R_D

Resistor R_D programs the loop current detection threshold I_{Lth} according to:

$$R_D = \frac{375}{I_{Lth}}$$

Let $I_L = I_{Lth}$ = 10 mA be the off-hook detection threshold current. Then R_D = 37.5 kΩ (select standard 5% value 36 kΩ).

6. Ac - dc Separation Capacitor C_{HP}

A C_{HP} value of 10 nF will position the low end frequency response 3 dB breakpoint at 48 Hz according to:
$f_{3dB} = 1/(2 \bullet \pi \bullet R \bullet C)$ where R = 330 kΩ.

7. Transmit Gain

At the combination CODEC/filter, TP3054, uncommitted op-amp output, GSX, the 0 dBm0 signal level is 1.2276 V_{Rms} (V_O). The corresponding input tip-ring voltage, V_{TR}, is -3 dBm or 0.6716 V_{Rms} (refer to gain/level plan for µ-law compatible PABX). The two-wire to four-wire gain between these two points is expressed as:

$$\frac{V_O}{V_{TR}} = \frac{R_T \ /1000}{R_T \ /1000 \ + \ 2R_F} \bullet \frac{R_{FB}}{R_{TX}}$$

if R_{TX} is set to 20 kΩ then R_{FB} can be calculated from the above expression to be R_{FB} = 40.12 kΩ (select standard 1% value 40.2 kΩ).

8. Receive Gain

At the combination CODEC/filter output, VFRO, the 0dBm0 signal level is 1.2276

V_{Rms} (V_{RX}). The corresponding output tip-ring voltage, V_{TR}, is +3 dBm or 1.34 V_{Rms} (refer to gain/level plan for μ-law compatible PABX). The four-wire to two-wire gain between these two points is expressed as:

$$\frac{V_{TR}}{V_{RX}} = \frac{R_T}{R_{RX}} \bullet \frac{R_L}{R_T/1000 + 2 \bullet R_F + R_L}$$

where

R_T = 820 kΩ, R_L = 900 Ω, R_F = 40 Ω.

Thus R_{RX} = 375.6 kΩ (select standard 1% value 374 kΩ).

9. Balance Network

$$R_B = R_{TX} \bullet \frac{R_{RX}}{R_T} \bullet \frac{R_T/1000 + 2 \bullet R_F + R_L}{2 \bullet R_F + R_L}$$

from which:

R_B = 16.75 kΩ
(standard 1% value is 16.9 kΩ).

10. Overload Levels at the Two-wire Port (PCM Channel Overload Level)

Note that the overload levels referred to are those imposed by the PCM channel.

Transmit (to PABX) overload level at the two-wire port: + 0.17 dBm or 0.97 V_{Rms} across 900 Ω (+ 3.17 dBm0).

Receive (from PABX) overload level at the two-wire port: + 6.17 dBm or 1.93 V_{Rms} across 900 Ω (2.73 V_{Peak} or +3.17 dBm0).

11. Relay Driver

The ring relay driver in the PBL 3762A is activated only when C2 = 0 and C1 = 1, the ringing state in a station line interface. In this state, the ring trip detector would be activated and the TIPX and RINGX terminals would be set to their high impedance state. Since the loop current detector must be active and since the vf paths must be active in both the normal and the reversed polarity case, the current version of PBL 3762A relay driver cannot be employed in the DID trunk interface. A 2N7000 MOSFET relay driver is suggested as a low cost alternative. Note that the 2N7000 gate voltage should be pulled to > + 4.5 V to operate a + 5 V relay, such as e. g. Aromat DS type (nominal operating power: 400 mW standard or 200 mW sensitive). 5 V HCMOS has adequate output drive to bring the level above + 4.5 V. If interfacing with TTL or LSTTL, take precautions to ensure sufficient drive capability. The inductive kickback protection is provided by a 20 V zener diode for maximum relay operating speed. A diode (e.g. 1N4454) connected with cathode to + 5 V and anode to the 2N7000 drain could alternatively be used, but may somewhat impede relay operating speed. Note that operating the relay will cause current pulsing on the + 5 V line.

V_{TA} , V_{RA}	Voltage range
Continuous voltage	V_{Bat} to +1 V
pulse < 10 ms	t_{Rep} > 10s -70 V to +5 V
pulse < 1 μs, ...	t_{Rep} > 10s -90 V to +10 V
pulse < 0.25 μs,	t_{Rep} > 10s -120 V to +15 V

Proper decoupling and/or trace routing may be required to avoid interference with other devices powered by the + 5 V supply. It may be advantageous to use another supply voltage such as +12 V for relay operation. The DS relay is available in 5 V, 12 V, 24 V, 48 V and other coil voltage ratings.

Figure 1. Example of PBL 3762A loop feed with current limiting.

$P = \frac{T_J - T_A}{Q_{JA}}$ P = Power, T_A = Ambient Temperature

Curve A: T_J = 110°C, Junction Temperature
Q_{JA} = 50°C/W, Junction-to-ambient Thermal Resistance

Curve B: T_J = 140°C, Junction Temperature
Q_{JA} = 50°C/W, Junction-to-ambient Thermal Resistance

Curve C: T_J = 140°C, Junction Temperature
Q_{JA} = 36.5°C/W, Junction-to-ambient Thermal Resistance (heatsink added to PBL3762)

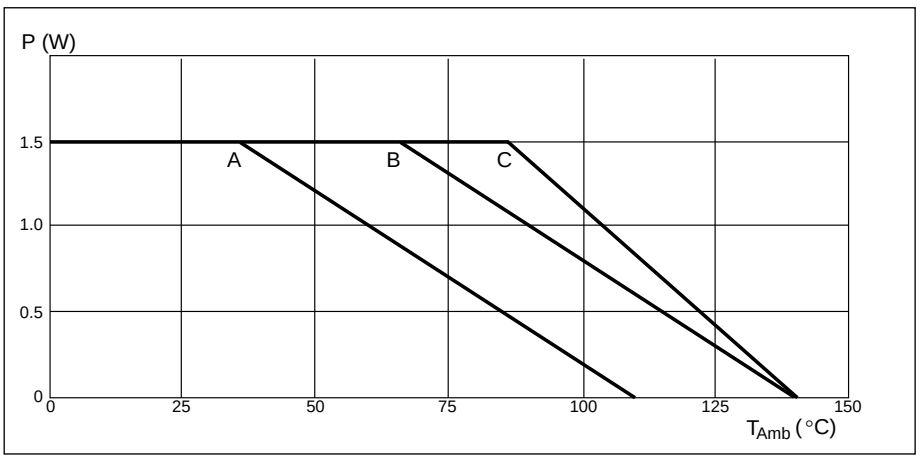
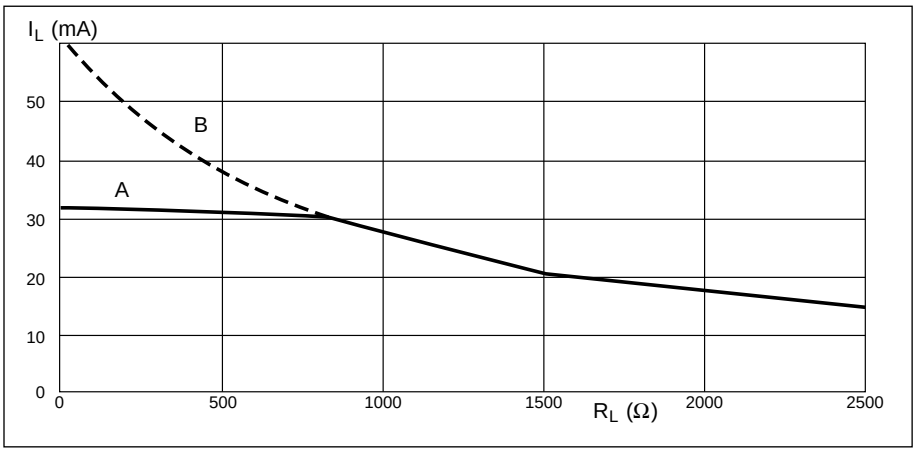
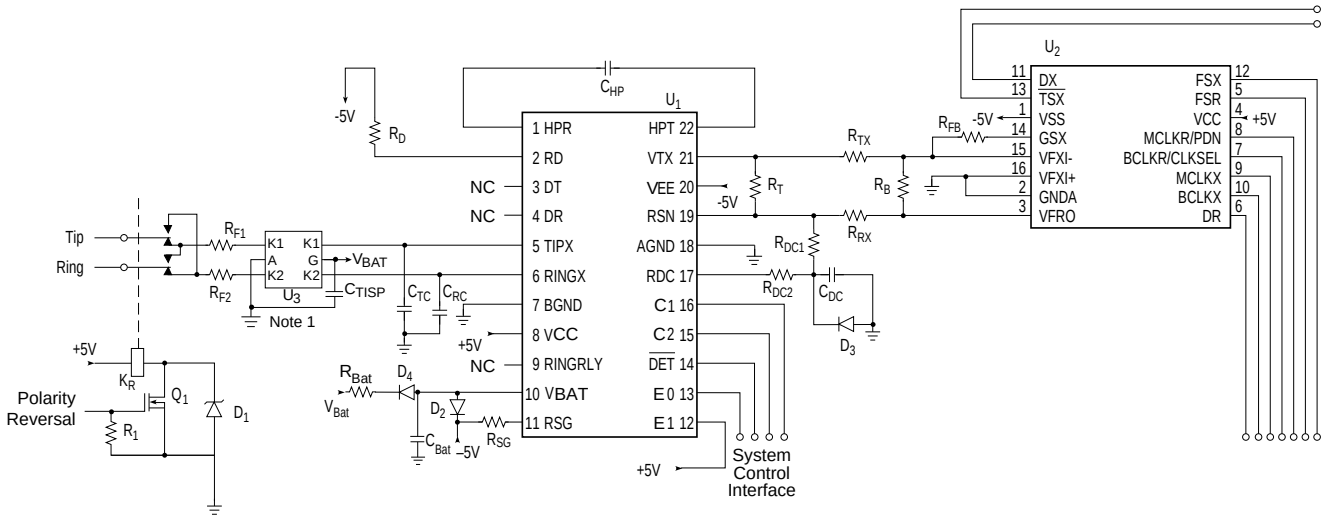


Figure 2. Example of PBL 3762A loop feed with current limiting.

Curve A: 50 V apparent battery voltage
782 Ω + 40 Ω feed resistance
Current limited to 32 mA
V_{SGREF} ≈ 37 V

Curve B: 50 V apparent battery voltage
782 Ω + 40 Ω feed resistance
Current not limited
V_{SGREF} ≈ 37 V





Qty	Reference	Part	Description
1	U_1	PBL 3762A	Ericsson Components SLIC
1	U_2	TP 3054	Combination CODEC/filter
1	U_3	TISP PBL1	Secondery protection (e.g. Texas Instruments)
1	D_2	1N4454	Diode, low cap., 300 mA, 50 V
1	D_1	1N5250A	Diode, zener, 20 V, 10%
2	D_3, D_4	1N4148	Diode
1	R_{Bat}	5,1Ω	Resistor 1/4 W 5 %
2	R_{F1}, R_{F2}	40 Ω	Ericsson Components PBR 510 12/1, 2 x 40 Ω
1	R_T	820 kΩ	Resistor 1/4 W 1% MF
1	R_{TX}	20.0 kΩ	Resistor 1/4 W 1% MF
1	R_{DC1}	16.9 kΩ	Resistor 1/4 W 1% MF
1	R_{DC2}	20.0 kΩ	Resistor 1/4 W 1% MF
1	R_{FB}	40.2 kΩ	Resistor 1/4 W 1% MF
1	R_{RX}	374 kΩ	Resistor 1/4 W 1% MF
1	R_B	16.9 kΩ	Resistor 1/4 W 1% MF
1	R_D	36 kΩ	Resistor 1/4 W 5%
1	R_{SG}	20 kΩ	Resistor 1/4 W 5%
1	R_1	51 kΩ	Resistor 1/4 W 5%
1	C_{Bat}	0.47 µF	Cap., 0.47 µF, 20 %, (V_{Bat}) +20 V
1	C_{DC}	8.2 µF	Cap., tant., 10 V
1	C_{HP}	0.01 µF	Cap., mon. cer., 50 V
2	C_{TC}, C_{RC}	2200 pF	Cap., mon. cer., 100 V
	C_{TISP}	220nF	Cap., 100 V 20%
1	Q_1	2N7000	MOSFET, n-channel, 60 V
1	K_1		Relay DPDT, Aromat DS, 5 V

Note 1. The ground terminals of the secondary protection should be connected to the ground terminal of the SLIC, and to the common ground on the Printed Board Assembly with a track as short and wide as possible, preferable a groundplane.

Figure 3. DID trunk interface with PBL 3762.

12. Application of V_{Bat}

As the line card is plugged into a powered back up plane, V_{Bat} should be applied to the SLICs with low $\partial v/\partial t$. Five ohms in series with the incoming V_{Bat} supply and then decoupled to ground by a 0.47 µF capacitor to ground is sufficient and may be shared by the SLICs on the card.

13. Overvoltage Protection

The PBL 3762A SLIC must be protected against overvoltages on the telephone line caused by lightning, ac power contact and induction. Refer to Maximum Ratings, TIPX and RINGX terminals, for maximum allowable continuous and transient voltages that may be applied to the SLIC. The circuit shown in figure 3 utilizes series resistors together with a programmable overvoltage protector (e g Texas Instrument TISP PBL1), serving as a secondary protection.

The protection network in figure 3 is designed to meet requirements in ITU-T K20, Table 1.

The TISP PBL1 is a dual forward-conducting buffered p-gate overvoltage protector. The protector gate references the protection (clamping) voltage to negative supply voltage (i.e. the battery voltage,V_{Bat}). As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clamped to ground by an internal diode. Negative overvoltages are initially clamped close to the SLIC negative supply rail voltage. If sufficient current is available from the overvoltage, then the protector will crowbar into a low voltage on-state condition, clamping the overvoltage close to ground.

A gate decoupling capacitor, C_{TISP} is needed to carry enough charge to supply a high enough current to quickly turn on the thyristor in the protector. Without the capacitor even the low inductance in the track to the V_{Bat} supply will limit the current and delay the activation of the thyristor clamp.

The fuse resistors R_F serve the dual purposes of being non- destructive energy dissipators, when transients are clamped and of being fuses, when the line is exposed to a power cross.

Ericsson Components AB offers a series of thick film resistors networks (e g PBR 51- series and PBR 53-series) designed for this application.

Also devices with a built in resetable fuse function is offered (e g PBR 52-series) including positive temperature coefficient (PTC) resistors, working as resetable fuses, in series with thick film resistors. Note that it is important to always use PTC´s in series with resistors not sensitive to temperature, as the PTC will act as a capacitance for fast transients and therefore the ability to protect the SLIC will be reduced.

If there is a risk of overvoltages on the V_{Bat} terminal on the SLIC, then this terminal should also be protected.

14. Un-used Inputs/Outputs

DT (pin 3) and DR (pin 4): leave open if not used.

C1 (pin 16), C2 (pin 15), E0 (pin 13), E1 (pin 12): these inputs must never be left open - connect to ground or + 5 V.

RINGRLY (pin 9): leave open if not used.

15. PCB Layout

Care in PCB layout is essential for proper PBL 3762A function. The components connecting to the RSN pin (19) should be in close proximity to that pin such that no interference is injected into the RSN terminal. Ground plane surrounding the RSN pin is advisable.

Specifications subject to change
without notice.
LZT 153 24 PBL 3762A Uen Rev. A

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