Application Note

PBL 3860A/6 Ring Through SLIC

The Ring Through SLIC (RTS) application is a method to allow a low voltage ring-signal to be amplified in the SLIC and transferred to the subscriber. There are several advantages with this application compared to a traditional solution. First of all no high voltage ring-generator is needed. Furthermore, since the ring-signal is connected to the line, in the same way as an ordinary voice signal, no ring relay is required either. The ordinary internal SLIC ring-trip detector is not used in this application. Therefore the ordinary ring-trip network is omitted.

With a battery voltage, VBat, of -80V during ringing, a balanced sine wave ring-signal of minimum 40Vrms is guaranteed across a 5REN load at the end of a 100Ω wire resistance loop.

Programming of the SLIC

For the programming of the battery feed characteristics and loop detector level, refer to the Telecommunication Circuits Databook. Those parts that are affected in the RTS application will be explained in this application note.

Output Impedance

The two-wire impedance, ZTR , presented by the SLIC to the line in active mode (except during the ring-burst) is calculated as:

$$Z_{TR} = \frac{Z_T}{1000} + 2\,(R_F + R_P)$$

Thus with Z_{TR} and R_F known:

$$Z_T = 1000 \bullet (Z_{TR} - 2 \bullet (R_F + R_P)$$

where Z_{TR} = the SLIC's two-wire (tip-ring) interface impedance.

R_F = the line resistor, R_P = SLIC protection resistor. Z_T = the SLIC two-wire impedance programming impedance.

Chose R_F=40Ω, R_P=40Ω.

R_{TR}=600Ω yields R_T=442kΩ.

Transmit Gain

The two-wire to four-wire gain between the TIPX - RINGX input and the VTX - ground output is calculated as

$$G_{2\text{-}4} = \frac{Z_T/1000}{Z_T/1000 + 2 \bullet (R_F + R_P)}$$

Receive Gain

The four-wire to two-wire gain between the TIPX - RINGX output and the V_{RX} to ground input is calculated in the active state, as:

$$G_{4\text{-}2} = \frac{-Z_T}{Z_{RX}} \bullet \frac{Z_L}{Z_T/1000 + 2 \bullet (R_F + R_P) + Z_L}$$

If R_T = 442 kΩ, R_F = R_P = 40 Ω, V_{TR}/V_{RX} =1 and Z_L = 600 Ω this yields R_{RX}=221 kΩ.

Balance Network

$$R_B = R_{TX} \bullet \frac{Z_{RX}}{Z_T} \bullet \frac{Z_T/100\ 0 + 2 \bullet (R_F + R_P) + Z_L}{2 \bullet (R_F + R_P) + Z_L}$$

from which, with our suggested component values, RB=15.8 kΩ

Ring-Signal Connection

The ring-signal can be generated in a CODEC with assistance from the device processor, which may send the appropriate stream of bytes to the CODEC. With this approach any desired ring-signal shape can be generated, maximising output amplitude and minimising EMI. The R_{SIN} and V_{RX} nodes are both connected to the CODEC, and the ring-signal is injected in the same way as an ordinary voice signal.

Operation of the Ring Loop

During ringing the line voltage is monitored by the differential stage, consisting of an operational amplifier and resistors R_{DT1}, R_{DR1}, R_{DT2} and R_{DR2}. This stage decreases the amplitude of the signal 39 times and relates it to ground. Due to the fact that we don't want leakage from the line to ground the resistors need to be high impedance, therefore the values are:

R_{DT1}, R_{DR1} = 10kΩ, R_{DT2}, R_{DR2} = 390kΩ

As the RSN input on the SLIC is a current input this pin can be used to mix the signal from the ring-loop and the signal source. The output voltage from the ring-loop is fed to a switch, which in its turn is connected to the RSN pin, by the RRS resistor. In the same way the signal source is connected to this point via the RRG resistor. When the switch is turned on, these resistors acts as voltage to current converters.

The resulting current that flows into the RSN input, IS, can be calculated as follows:

$$I_S(t) = \frac{Vg(t)}{R_{RG}} + \frac{\beta \bullet V_{TR}(t)}{R_{RS}}$$

where Vg(t) is the signal from the signal source.

$\beta = R_{Dx1} / R_{Dx2}$ =1/39, x = TIP / RING.

The ring-signal from the SLIC will be balanced about V_{Bat} / 2.

The Ring Loop Switch

To connect the ring-loop when ringing there must be an external switch between the RSN input and the R_{RS} and R_{RG} resistor. Normally, when not in ring-mode, this switch should be open.

This switch could be implemented in different ways, see fig 1. The best performance is achieved using an

analogue multiplexer like the 74HC4053 or similar, this device includes three switches. The second best choice is to use the 4066/-16, this device is suitable for two lines.

The 4066/-16 device needs a level shifter since the low state must equal VEE , due to the internal design. The noise from the ring loop and ring signal source will be lower in the case of using the 4053. Since this is a double pole switch the signal will be fed to ground when not in ring mode.

Control Inputs

To be able to use the SLIC as a ring-signal amplifier it must be put in the active state during the ring-burst and NOT in the ring-mode, this is because the internal output stage has to be used.

To be able to switch the ring-loop on and off there is an additional control signal: C0. This signal is connected to the switch described in the previous part.

state:	C0 I	C0 II	C1	C2
Open circuit	1	0	0	0
Active	1	0	0	1
Ringing	0	1	0	1
Stand-by	1	0	1	1

For the different types of switches C0 is configured as follows, se fig. 1:

I: applies to 4016 and 4066.
4053 can be used in both modes.

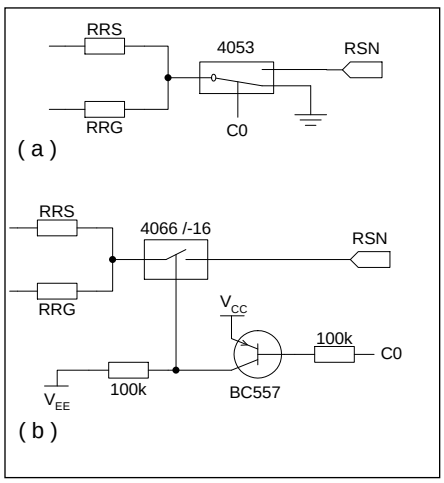


Fig. 1 Ring loop switches.

Application of V_{Bat}

The battery should be switched to -80V, to be able to fulfil the Bellcore requirements of min 40Vrms over a 5REN load with a sine wave. The battery switching can be solved in one of two ways, either using switching of a dual VBat supply (of -48V and -80V e.g.), or by using a programmable DC/DC converter.

In order to minimise the power dissipation in the SLIC the maximum VBat current shall be limited to 70mA when using a voltage below -60V.

A suggestion of a VBat switch is presented in the figure 5, where $|V_{BAT2}| > |V_{BAT1}|$.

Ring Trip Detection

As the SLIC's internal ring-trip detector can't be used in this application, ring trip must be arranged in another way.

In the case of up to 5REN load connected to a short line (of up to 100Ω) the SLIC loop detector can be used to detect off-hook during ringing with the help of one extra resistor and a switch, see fig 2.

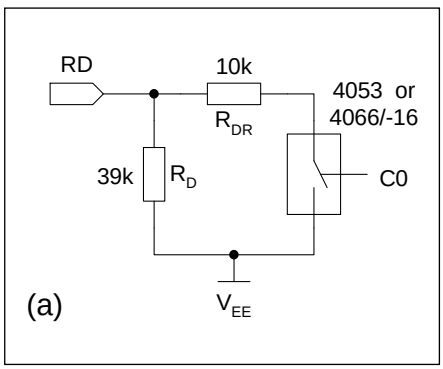


Fig. 2 Ring trip components.

The RD resistor is calculated as follows

$$R_{DR} = \frac{385 \bullet R_D}{R_D \bullet I_L - 375}$$

Where IL is the peak line current threshold when ringing. For a 5REN load and a V_{BAT2} of -80V, I_L is 48mA. This results in a RDR resistor of 10kΩ.

This can be achieved because of the change in impedance when the phone goes off-hook. During ringing the impedance is larger than 1,4kΩ, even for 5REN, and when a phone goes off-hook it will decrease to less than 500Ω.

This solution minimises the number of external components.

There might be a need for software filtering of the detector signal because it will ripple, but in most cases this will not be necessary. See fig 3 for the behaviour of the states at the DET pin and voltage at the RD pin.

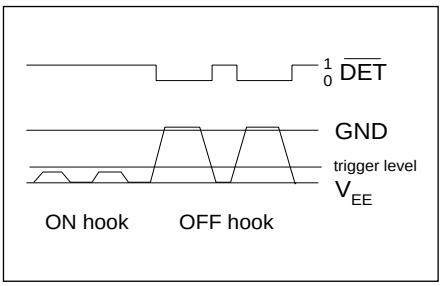


Fig. 3 Ring-trip detector behaviour.

For other cases and methods, please do not hesitate to contact Ericsson Components for assistance.

Over-Voltage Protection

When using the SLIC as a ring generator the over-voltage protection (OVP) must be carefully considered in order to meet the requirements of the SLIC with the higher than usual voltages supplied to the line.

As the line voltage, depending of VBat, can be over 60V a programmable transient voltage suppressor must be used. We recommend Texas Instruments TISP PBL1, TISP61CAP3 or TISP61089 which all can handle 80V.

Make sure that V_{Bat} is connected to the SLIC and the gate of the OVP in the proper way:
The SLIC and the OVP ground should be tied together on the PCB.

A capacitor of min 220nF should be connected close to the gate of the OVP, to decouple the VBat voltage when the OVP starts to conduct. This can be done by placing the CBat capacitor close to the gate of the transient protector.

The R_F resistors limits the transient currents and R_P limits the currents to the SLIC while the OVP conducts. R_P is very important in this application to prevent the output-stages TIPX and RINGX from being damaged, if the OVP conducts during ringing.

Power cross protection is provided by the R_F resistors in conjunction with the OVP. For the R_F resistors, we recommend Ericsson Components' thickfilm resistors PBR510 12/1 (2•40Ω),

which are designed to fail open circuit without catching fire when exposed to electrical overload.

Power Dissipation

The short circuit SLIC power dissipation PShTot is:

$$P_{ShTot} = I_{LSh} \bullet (|Vbat| - I_{LSh} \bullet 2 \bullet (R_F + R_P)) + P_3$$

where VBat is the battery voltage connected to the SLIC at pin V_{BAt}.

$$I_{LSh} = \frac{2.5 \bullet 1000}{RDC1 + RDC2}$$

is the constant loop current. P3 is on-hook active state power dissipation (typ 200mW; VBat = -48V). Note that a short circuited loop is not a normal operational condition. The terminating equipment will add some dc resistance (150 to 300 Ω) even if the wire resistance is close to 0Ω.

During ringing the highest power dissipation occurs when the line is 0Ω and maximum number of bells are connected (5REN). With the suggested values given in this note the maximum line current ILmax will be 47 mA. The power drawn from the supply is then with class-B amplifiers:

$$P_S = \frac{2 \bullet 80 \bullet 47}{\pi} + P_{idle} \approx 2.6W$$

The output power from the SLIC is:

$$P_{out} = I_{lrms}^2 \bullet (Z_{bell} + 2 \bullet (R_F + R_P)) \approx 1.7W$$

This means that the power dissipation in the SLIC is about 0.9W during ringing, which is within the limit for maximum ratings.

Unused Inputs / Outputs

DT (pin 3), DR (pin 4) and RINGRLY (pin 9) are not used in this application: leave open.

PCB Layout

Care in PCB layout is essential for proper PBL3860A/6 function. The components connected to the RSN input (pin 16 for PLCC) should be in close proximity to that pin such that no noise is injected into the RSN terminal. Ground plane surrounding the RSN pin is advisable.

The track between the gate of the OVP and the CGO capacitor must be short and wide.

The SLIC and the OVP ground should be tied together on the PCB.

Ring Voltage

First we define: Crest factor $\triangleq \frac{\hat{V}}{V_{rms}}$

The following two tables define the voltage over the bell under different conditions. First the load voltage as a function of line length, number of bells and shape of the ring signal when VBat = -80V, RSIN = 2.0V peak.

Load #REN	RL	Crest factor	Load voltage
1	0	1.41; sin	52.2
3	100	1.41; sin	47.2
5	100	1.41; sin	43.5
1	0	1.20	62.9
3	100	1.20	57.0
5	100	1.20	52.6
1	0	1.05	72.0
3	100	1.05	65.2
5	100	1.05	60.2

In the next table the required VBat to achieve a specific voltage over the bell (40 or 50 V) is presented, the load is fixed at 3 or 5REN with 100Ω wire resistance. RSIN as above.

Load voltage	Crest factor	Vbat [V] 3REN	5REN
40	1.41; sin	67.2	73.0
40	1.20	56.4	61.2
50	1.20	70.5	76.1
40	1.05	49.4	53.2
50	1.05	61.3	66.8

Ring Signal Generator

There are different ways of generating the low voltage ring signal.

One is to use the CODEC as a oscillator, this can be done if access to the PCM bus is provided. The micro controller feeds the CODEC with a stream of bytes to generate the desired frequency and amplitude.

Another choice is to use a D/A converter connected to the micro controller.

Then there are different kinds of oscillator circuits.

In this application note we have used an Wien bridge sine wave oscillator. The circuit uses two resistors and one diode to stabilise the amplitude, se fig 4.

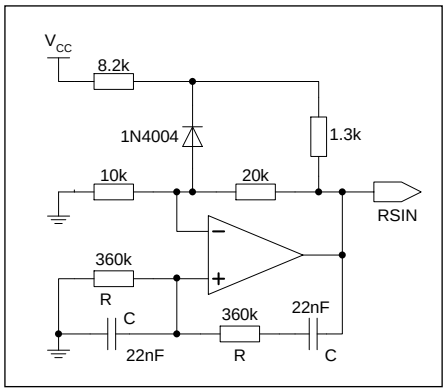
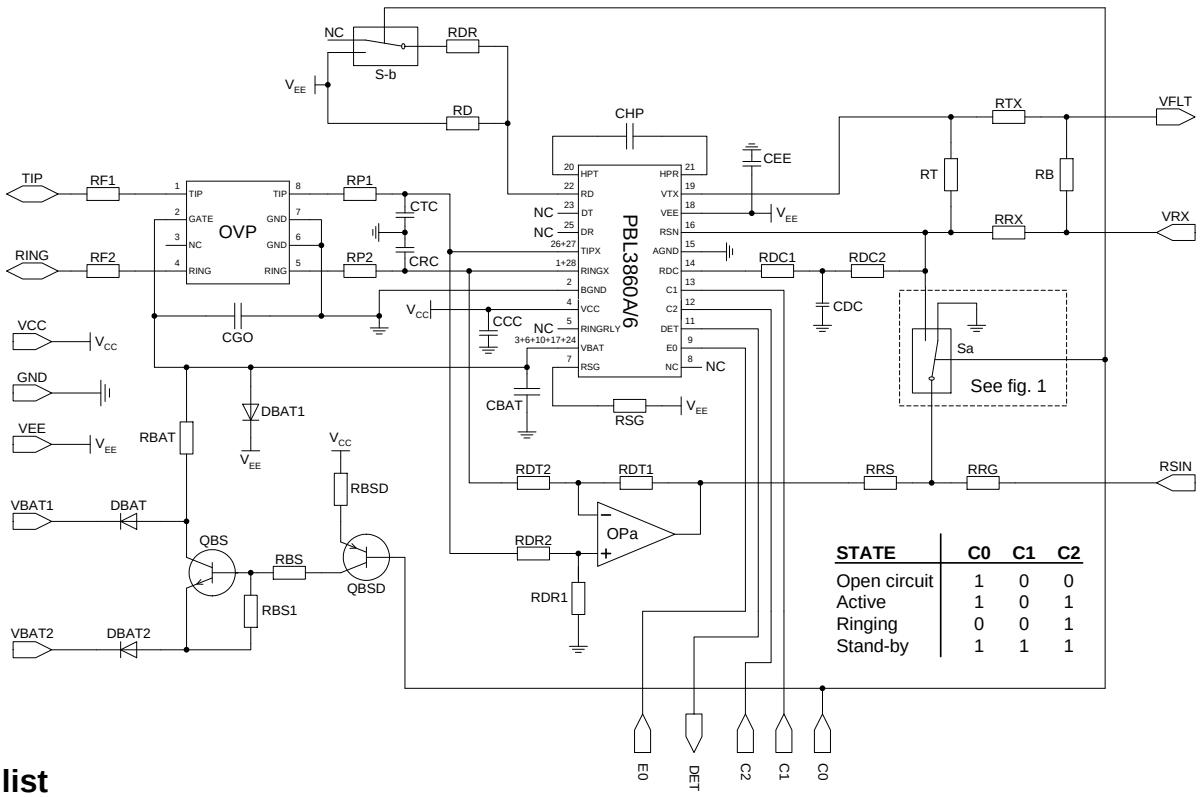


Fig. 4 Wien bridge sine wave oscillator.

With components values shown, the RSIN output will be an 1.4Vrms sine wave with a frequency of 20Hz.
The frequency is determined by Resistor R and capacitor C according to

$$f = \frac{1}{2 \bullet \pi R \bullet C}$$

There is no need to use one oscillator for each line, depending on the amplifiers current capability. So if the current driving capability of the amplifier is high enough, only one oscillator is required per line card, regardless of the number of lines.



STATE	C0	C1	C2
Open circuit	1	0	0
Active	1	0	1
Ringing	0	0	1
Stand-by	1	1	1

Part list

SLIC	PBL3860A/6
OVP	TISP 61CAP3
OPa	LM324
Sa, b	74HC4053
QBS	MPSA42
QBSD	MPSA92
DBAT	1N4004
DBAT1	10MQ090
DBAT2	1N4004
RF1, 2	PBR510 12/1 2*40Ω
RP1, 2	39Ω ≥1/4 W
RBAT	5.1Ω 5% ≥1/4 W
RSG	*
RDC1, 2	51k*
RD	39k*
RDR	10k*
RT	442k*
RRX	221k*
RTX	20k*
RB	15.8k*
RDT1, RDR1	10k
RDT2, RDR2	390k
RRS, RRG	2k
RBS	22k
RBS1	10k
RBSD	2k
CBAT	0.22µF100V
CGO	0.22µF100V
CTC, CRC	2.2nF 100V
CHP	10nF 100V
CDC	1µF
CCC, CEE	220nF

All resistors are 1%

*Fig. 5 Components marked with * are application dependent, see this note and Telecomunication Circuits Databook for more information.*

LZT Over-voltage protection Uen Rev. A

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