National Semiconductor

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PC87782 CompactRISC Intelligent System Management Controller

General Description

The PC87782 CompactRISC™ 16-bit Embedded Controller is a highly integrated microcontroller designed for power management applications in desktop Personal Computers (PCs). The device is optimized for ACPI Power Management, including multi-pattern Wake-up on LAN scanning; and System Environment monitoring, including fan speed, supply voltages, temperature and chassis intrusion. The PC87782 incorporates National's CR16A CPU core (a high-performance 16-bit RISC core), on-chip memories, and system support functions.

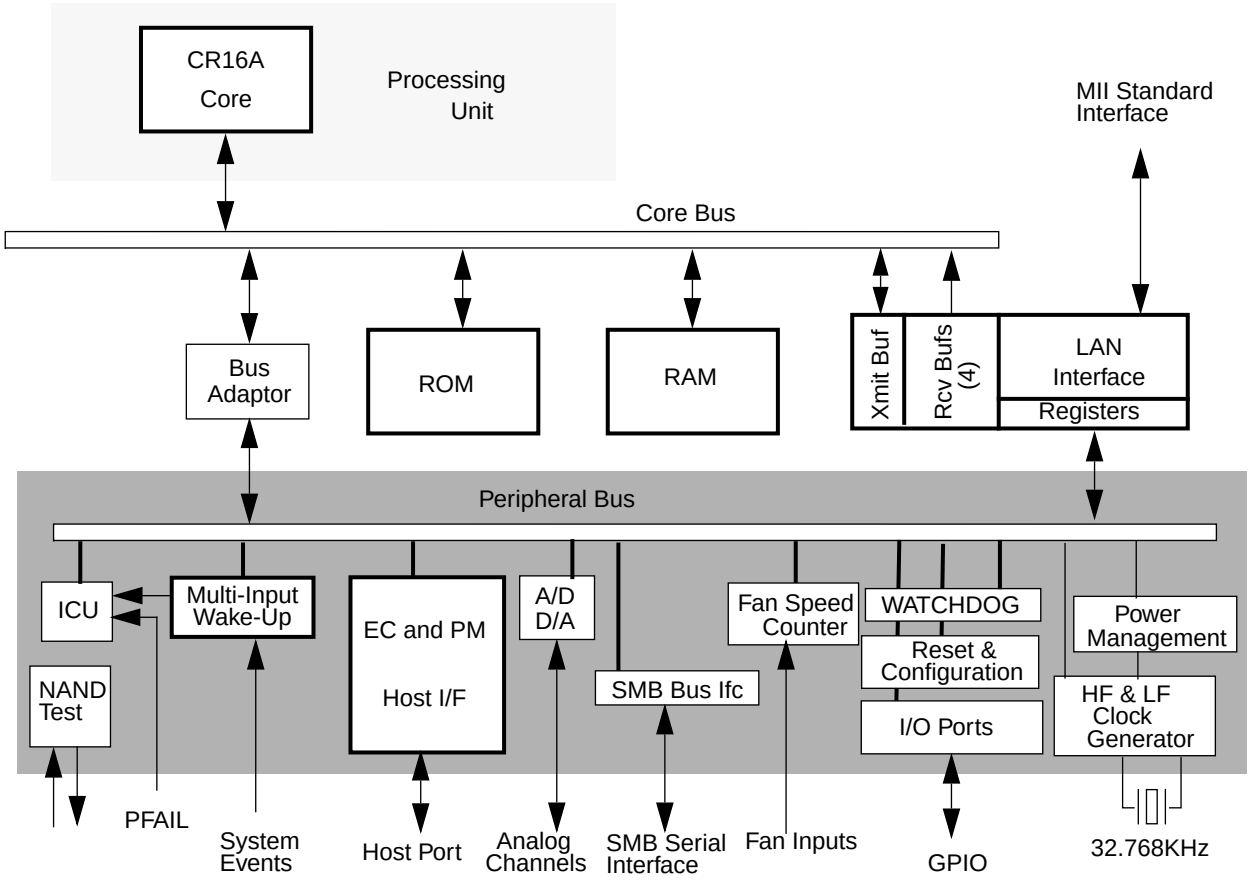
The CR16A core offers the high performance of a RISC architecture while retaining the advantages of a traditional Complex Instruction Set Computer (CISC): compact code, on-chip memory and I/O, and low cost. The CPU uses a three-stage instruction pipeline that allows execution of up to one instruction per clock cycle, or up to 20 million instructions per second (MIPS) at the maximum clock rate of 20 MHz.

Patent Pending.

Features

- CPU Features
  - — Fully static core, capable of operating at any rate from 4 MHz to 20 MHz
  - — On-chip high-speed clock generator
  - — Multi-source vectored interrupts (internal, external, and on-chip peripheral)
  - — On-chip power-on reset
- On-Chip Memory
  - — 32K mask-programmed ROM program memory
  - — 2,784 bytes of static RAM data memory
- On-Chip Peripherals
  - — Host Interface to PC (ISA and ACPI 1.0 compatible)
  - — 10/100 LAN Interface to monitor network traffic for PC wake-up on LAN activity
  - — Fan-Speed Timer to monitor cooling fans
  - — System Management (ACCESS.bus) Interface, a 2-wire serial interface compatible with Intel's SMBus and Phillips' I^2C bus
  - — 8-channel, 8-bit Analog-to-Digital (A/D) converter
  - — 8-bit Digital-to-Analog (D/A) converter
  - — Integrated WATCHDOG™ logic

System Diagram



General Description (continued)

Each PC87782 device has 16 kbytes of mask-programmed ROM, 2,784 bytes of on-chip static RAM, a Host Interface, a LAN Interface, a System Management (Access.bus) Interface, a fan-speed timer, an A/D converter, a D/A converter, WATCHDOG protection, and a set of general-purpose I/O pins.

The PC87782 is available in 100-pin and 160-pin PQFP packages. The 160-pin device provides development support and offers the additional ability to use off-chip memory and I/O.

The PC87782 device is driven by a slow (32.768 kHz) oscillator. An on-chip clock circuit generates a high-speed clock to drive the device for normal operation, at a programmable rate ranging from 4 MHz to 20 MHz. The device supports a power save mode called the Idle mode, which is combined with multi-source interrupt and wake-up capabilities.

Features (continued)

- I/O Features
  - — Up to 40 general-purpose I/O pins (shared with on-chip peripheral I/O pins)
  - — Programmable I/O pin characteristics: TRI-STATE® output, push-pull output, weak pull-up input, high-impedance input
  - — Schmitt trigger inputs on all I/O ports
  - — External memory and I/O support in 160-pin device
- Power Supply
  - — 4.5V to 5.5V single-supply operation
- Temperature Range
  - — -40°C to +85°C extended temperature range
- Package Types
  - — 160-pin PQFP
  - — 100-pin PQFP
- Development Support
  - — Real-time emulation and full program debug capabilities supported by 160-pin device
  - — CompactRISC tool set provides C programming and debugging support

Device Overview

The PC87782 is a microcontroller with all system interfaces, interrupt logic, program memory, data memory, and I/O ports included on-chip, making it well-suited to PC monitoring applications. The block diagram on the page 1 of the data sheet shows the major on-chip components of the PC87782. Figure 1 shows a connection diagram of the PC87782 to the PC system.

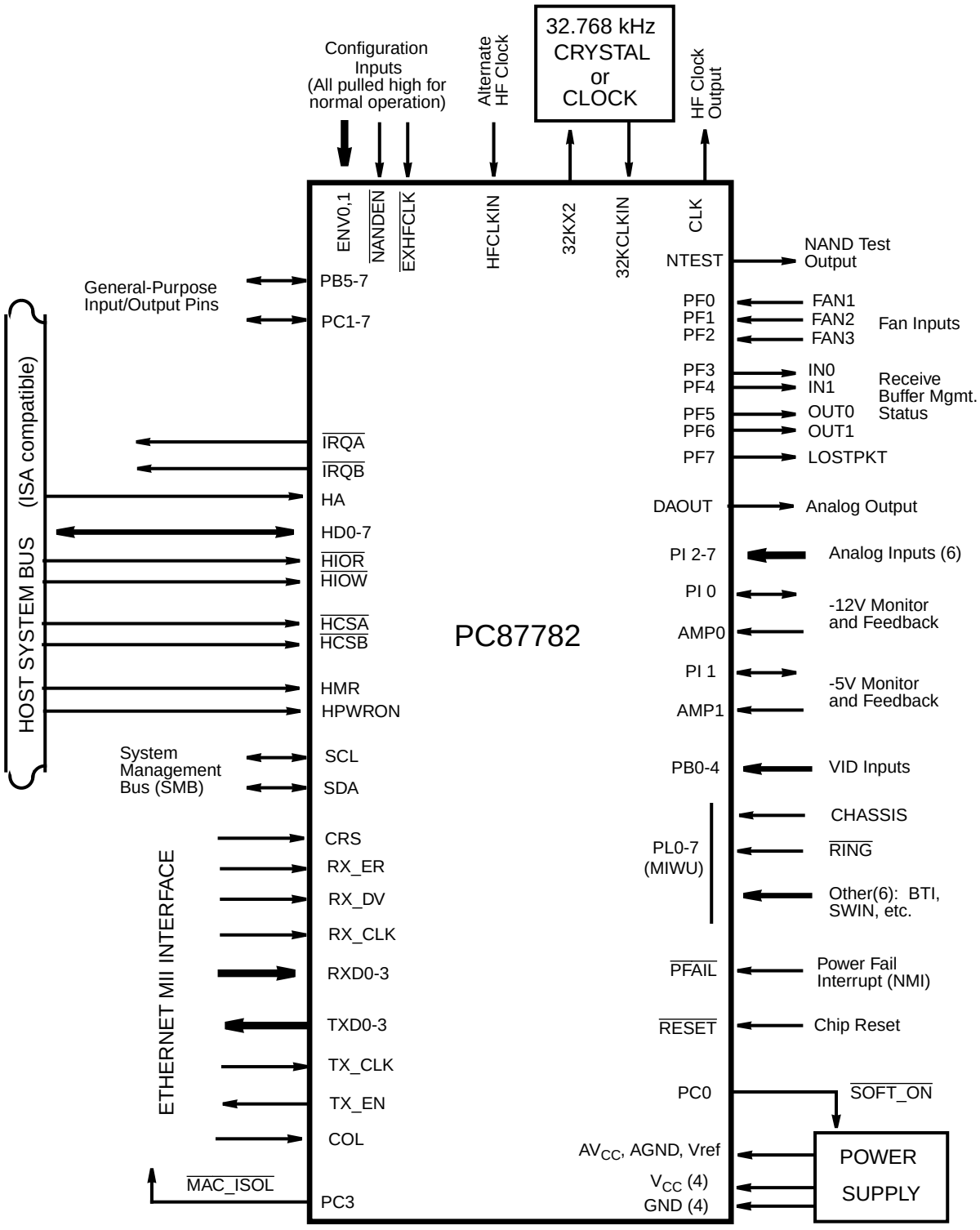


Figure 1. PC87782 Stand-Alone System Connection

CR16A CPU Core

The PC87782 uses a CR16A CPU core module. This is the same core used in other CompactRISC family members. The core's Reduced Instruction Set Computer (RISC) architecture is similar to that used in high-performance workstations. The PC87782 RISC processor takes advantage of this architecture while maintaining the on-chip features and low cost of an embedded controller.

The high performance of the CPU core results from the implementation of a pipelined architecture with a two-bytes-per-cycle pipelined system bus. As a result, the CPU can support a peak execution rate of one instruction per clock cycle.

Compared with conventional RISC processors, the PC87782 differs in the following ways:

- The CPU core uses on-chip rather than external memory. This eliminates the need for large and complex bus interface units.
- All opcodes are 16 bits, so all basic instructions are just two bytes long. (Additional bytes are sometimes required for immediate values, so instructions can be two, four, or six bytes long.)
- Non-aligned access of multiple bytes is allowed. Each instruction can operate on 8-bit, 16-bit, or 32-bit data.
- The device is designed to operate with a clock rate in the 10 to 20 MHz range rather than 100 MHz or more. Most embedded systems face EMI and noise constraints that limit clock speed to these lower ranges. A lower clock speed means a simpler, less costly silicon implementation.
- The instruction pipeline uses three stages rather than the usual five or more used in workstation processors. A smaller pipeline eliminates the need for costly branch prediction mechanisms and bypass registers, while maintaining adequate performance for typical embedded controller applications.

Memory

The CompactRISC architecture supports a uniform linear address space of 256K bytes. The PC87782 implementation of this architecture uses only the lowest 64K bytes of address space. Three types of on-chip memory occupy specific intervals within this address space: 32K bytes of ROM program memory and 2,784 bytes of static RAM memory.

The 32K bytes of ROM program memory are used to store the application program. For prototype work, the 160-pin device supports the use of external memory in place of the on-chip ROM.

The 2,784 bytes of static RAM are used for temporary storage of data and for the program and interrupt stacks. Read and write operations can be byte-wide or word-wide, depending on the instruction executed by the CPU. Each memory access requires one clock cycle; no wait cycles or hold cycles are required.

Input/Output Ports

Each device has 40 software-configurable I/O pins, organized into six 8-pin ports called Port B, Port C, Port F, Port L, and Port I. Each pin can be configured to operate as a general-purpose input or general-purpose output. In addition, many I/O pins can be configured to operate as a designated input or output for an on-chip peripheral module.

The I/O pin characteristics are fully programmable. Each pin can be configured to operate as a TRI-STATE output, push-pull output, weak pull-up input, or high-impedance input. All input pins are equipped with Schmitt triggers for noise resistance.

Bus Interface Unit

The Bus Interface Unit (BIU) controls the interface between the on-chip modules to the internal core bus (and to off-chip memory or I/O, if used). It determines the configured parameters for bus access (such as the number of wait states for memory access) and issues the appropriate bus signals for each requested access.

The BIU uses a set of control registers to determine how many wait states and hold states are to be used when accessing different types of memory. Upon start-up of the device, these registers must be programmed with appropriate values so that the minimum allowable number states is used.

Interrupts

The Interrupt Control Unit (ICU) receives interrupt requests from internal and external sources and generates interrupts to the CPU. An interrupt is an event that temporarily stops the normal flow of program execution and causes a separate interrupt service routine to be executed. After the interrupt is serviced, CPU execution continues with the next instruction in the program following the point of interruption.

Interrupts from the on-chip peripherals and interface modules are all maskable interrupts; they can be enabled or disabled by the software. There are 16 of these interrupts, organized into 16 predetermined levels of priority.

The highest-priority interrupt is the Non-Maskable Interrupt (NMI), which is generated by a signal received on the $\overline{\text{PFAIL}}$ input pin.

Multi-Input Wake-Up

The Multi-Input Wake-up (MIWU) modules can be used for either of two purposes: to wake up (exit from) from the Idle mode upon the occurrence of specified events; or to provide general-purpose edge-triggered maskable interrupts from external sources. One eight-channel MIWU module generates a combined interrupt to the CPU based on the signals received on its eight input channels, which are alternate functions of Port L. Channels can be individually enabled or disabled, and programmed to respond to positive or negative edges. Another MIWU module generates a combined interrupt to the CPU based on internal events: a Timer T0 event, a Host Bus read or write, or an SMB wake-up event.

Clock Generator

The Clock Generator module generates a high-speed main system clock (4 to 20 MHz) based on a slow (32.768 kHz) clock signal or crystal network. An on-chip oscillator generates the high-speed clock and locks on to the programmed rate, using the low-speed clock as a reference.

The slow clock is also used for operating the device in Idle mode. During Idle mode, the fast clock oscillator continues to operate but is disconnected from the rest of the device to reduce power consumption.

Power Management

The Power Management Module (PMM) improves the efficiency of the PC87782 device by changing the operating mode (and therefore the power consumption) according to the current level of activity. There are two power modes, called Active and Idle. The Active mode is the normal operating mode. In the Idle mode, the device is inactive except for the Power Management Module and Timing and Watchdog Module, which continue to operate using the slow clock.

Host Interface

The Host Interface module is an interface to the host PC. It consists of two channels. One channel is intended for System Environment Monitoring functions, similar to those provided by the LM78. The second channel is intended for Power Management functions as defined for ACPI 1.0.

The PC87782 can generate Host Interface interrupt requests: the SMI and SCI special interrupts, and two maskable interrupts to manage transfers on the two host interface channels. This allows the PC87782 to be used with polling or interrupt driven schemes. The hardware is designed to allow a race-free interface between the host and PC87782.

SMB (ACCESS.bus) Interface

The System Management Bus (SMB) is a two-wire serial interface compatible to the Intel SMB physical layer. It is also compatible with ACCESS.bus and Phillips' I^2C. SMB may serve as a bus master or a bus slave and perform both transmit and receive operations.

LAN Interface

The Local Area Network (LAN) interface module provides the ability to monitor Ethernet network traffic. It is designed for the purpose of determining when to wake up a sleeping host system. It can operate at 10 or 100 Mbps using the MII Standard Interface.

Fan-Speed Timer

The Fan-Speed Timer contains a single 8-bit timer with a digital input-glitch filter, designed to count the revolutions of a cooling fan according to the tachometer pulses received from the fan. The module has an input multiplexer, allowing up to three different fans to be monitored.

NAND Test

The NAND Test circuit provides the ability to test the input pins of the device. When the $\overline{\text{NANDEN}}$ input is pulled low, the tested pins float and become inputs, and are logically NANDED to an output pin, NTEST.

Real-Time Clock and Watchdog

The Timing and Watchdog Module (TWM) generates the clocks and interrupts used for timing periodic functions in the system. It also provides Watchdog protection against software errors. The module operates on the slow (32.768 KHz) clock.

The real-time clock generates a periodic interrupt to the CPU at a software-programmed interval. This can be used for real-time functions such as a time-of-day clock.

The Watchdog is designed to detect program execution errors such as an infinite loop or a "runaway" program. Once Watchdog operation is initiated, the application program must periodically write a specific value to a Watchdog register, within specific time intervals. If the software fails to do so, a Watchdog error is triggered, which resets the device.

A/D and D/A Converters

The A/D Converter (ADC) module is an 8-channel multiplexed-input analog-to-digital converter. The A/D Converter receives an analog voltage signal on an input pin and converts the analog signal into an 8-bit digital value using successive approximation. The CPU can then read the result from a memory-mapped register. The module supports four automated operating modes, providing single-channel or scanned 4-channel operation in single or continuous mode. Reading negative voltages is supported on two channels by activating a set of on-chip op-amps.

The D/A Converter (DAC) module is a single-channel analog-to-digital converter. The CPU writes a digital value to a register and the D/A converter generates an analog voltage proportional to the programmed value.

Reset and Configuration

The Reset and Configuration module controls the setting of the environment and resets the device in response to power up detection, WATCHDOG error, a rising edge on the host reset signal (HMR), a low level on the $\overline{\text{NANDEN}}$ pin, or a low level on the $\overline{\text{RESET}}$ pin.

Operating Modes

The PC87782 is designed to operate in one of three modes: Internal ROM Enabled (IRE), Internal ROM Disabled (IRD), or Development. The 100-pin device can operate only in the IRE mode, whereas the 160-pin device can operate in any of the three modes. The IRD mode uses off-chip memory instead of the on-chip ROM, which is useful for prototype work. The Development mode is useful for Application Development Boards and In-System Emulators.

External Interface

The PC87782 interfaces with the following external devices:

- the Host processor, via the ISA interface and/or the SMB (I^2C) interface,
- an Ethernet LAN Physical interface device, sharing the MII interface with a standard MAC device
- one or more LM75-series temperature monitors and/or other serial devices, via the SMB interface

In a Development environment, the device also interfaces with the ROM and RAM of the development system and the development system peripherals.

Table 1 is a list of the PC87782's signals in alphabetical order, together with a brief description of each signal. Only the pins in the 100-pin package are listed in this table. The 160-pin device has additional pins to support its additional functions.

Table 1 PC87782 Signals (100-Pin Package)

Signal Name	Type	Function
32KCLKIN	Input	32.768 KHz Oscillator Clock Input
32KX2	Oscillator	32.768 KHz Crystal Oscillator Interface
AMP0	Analog In	Negative Voltage to Port I0 A/D op-amp
AMP1	Analog In	Negative Voltage to Port I1 A/D op-amp
CLK	Output	CPU Clock Output
COL	Input	MII Interface: Collision Detect
CRS	Input	MII Interface: Carrier Sense
DAOUT	Analog Out	D/A Converter Output
ENV0-1	Input	Environment select strap inputs
FAN1	Input	Fan Speed Timer Input 1
FAN2	Input	Fan Speed Timer Input 2
FAN3	Input	Fan Speed Timer Input 3
HA	Input	Host Address line: Distinguishes Commands from Data bytes.
HCSA	Input	Chip Select for Host Interface A
HCSB	Input	Chip Select for Host Interface B
HD0-7	I/O	Bidirectional Data bus used to interface the PC87782 to the peripheral data bus of a host.
EXHFCLK	Input	For factory test purposes only. Must be pulled permanently high in end applications.
$\overline{\text{HIOR}}$	Input	Host I/O Read. Active-low input to signal data read by the host processor.
$\overline{\text{HIOW}}$	Input	Host I/O Write signal which enables a write operation to the PC87782 through HD0-7.
HMR	Input	Host Master Reset. Indicates state of Host system.
HPWRON	Input	Host Power On Indication.
IN0-1	Output	LAN Receiver Buffer Management: IN pointer
$\overline{\text{IRQA}}$	Output	Interrupt A. Signals an interrupt on host channel A.
$\overline{\text{IRQB}}$	Output	Interrupt B. Signals an interrupt on host channel B.
LOSTPKT	Output	LAN Receiver: Buffer Overflow
$\overline{\text{MAC\_ISOL}}$	Output	Isolates MII from standard LAN MAC when low.
$\overline{\text{NANDEN}}$	Input	NAND Test Enable / ISE TRI-STATE Control
NTEST	Output	NAND Test Output
OUT0-1	Output	LAN Receiver Buffer Management: OUT pointer
PB0-7	I/O	Port B, bits 0 through 7
PC0-7	I/O	Port C, bits 0 through 7
PF0-7	I/O	Port F, bits 0 through 7
$\overline{\text{PFAIL}}$	Input	Power Fail (Non-Maskable Interrupt) Input
PI0-7	Analog I/O	Port I A/D converter Analog Inputs. PI0 and PI1 can be configured as analog feedback outputs for inputs AMP0 and AMP1, respectively.
PL0-7	!/O	General-purpose Wake-Up inputs for $\overline{\text{RING}}$, CHASSIS, SWIN, $\overline{\text{BTI}}$ and other events.
$\overline{\text{RESET}}$	Input	Master Reset to PC87782 device
RXD0-3	Input	MII Interface: Received Data nibble
RX_CLK	Input	MII Interface: Receiver Clock
RX_DV	Input	MII Interface: Receiver Data Valid
RX_ER	Input	MII Interface: Received Error

Table 1 PC87782 Signals (100-Pin Package)

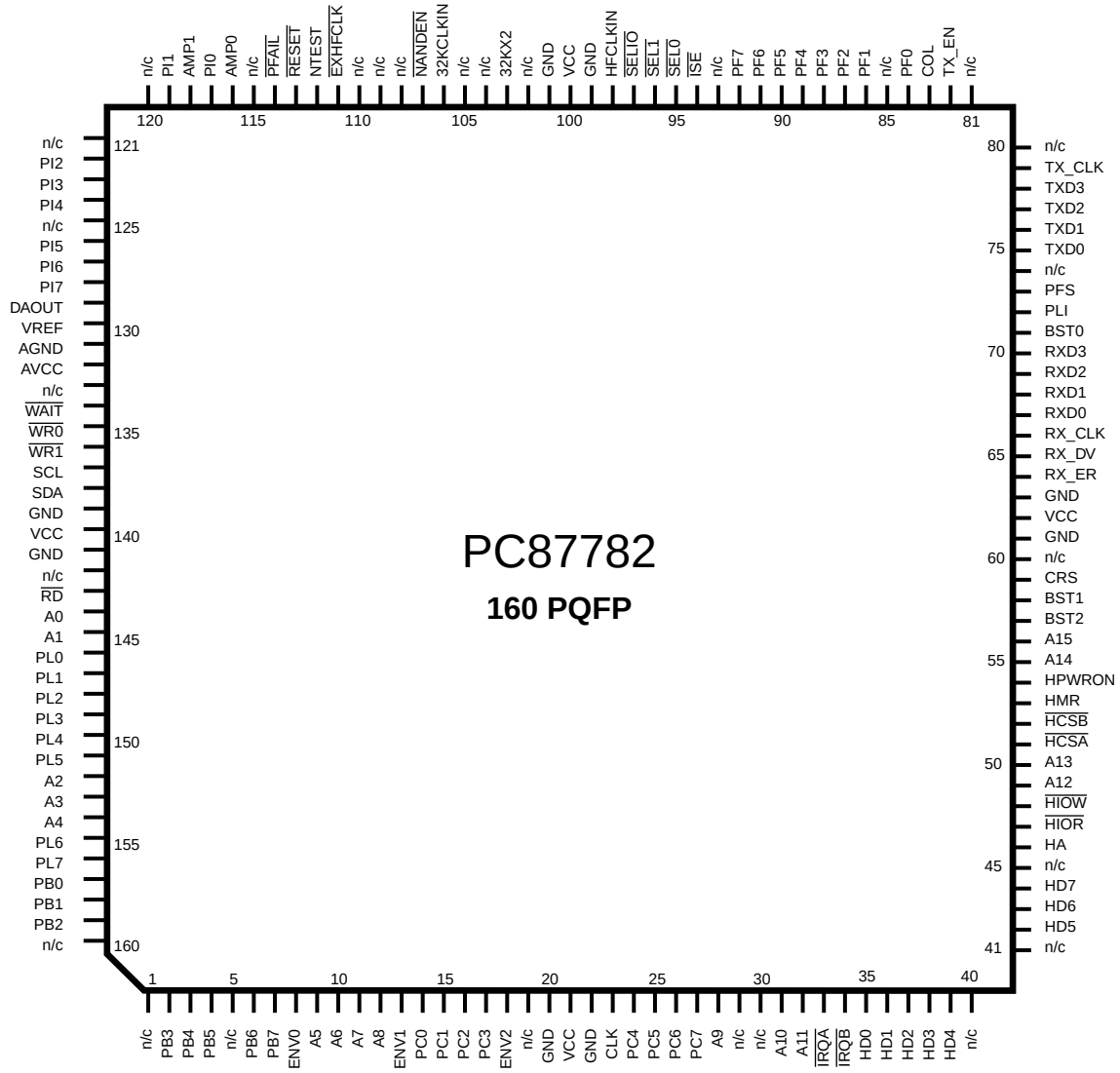
Signal Name	Type	Function
SCL	I/O	SMB clock signal
SDA	I/O	SMB data signal
$\overline{\text{SOFT\_ON}}$	Output	Software Control to Power Supply
TXD0-3	Output	MII Interface: Transmit Data nibble
TX_CLK	Input	MII Interface: Transmit Clock
TX_EN	Output	MII Interface: Transmit Enable
$\overline{\text{VID0-4}}$	Input	Voltage Identifier Strap Inputs
VREF	Analog Input	A/D Reference Voltage.
AV_{CC}	Power	Analog Supply for the on-chip A/D and D/A
V_{CC}	Power (4)	Power Supply. +5 Volt supply
AGND	Power	Analog Ground for the on-chip A/D and D/A
GND	Power (4)	Ground for on-chip logic and output drivers

Device Pinouts

The PC87782 is available in 160-pin and a 100-pin packages. Figure 2 and Figure 3 show the pin assignments for the two package sizes, and Table 1, “PC87782 Signals (100-Pin Package),” on page 6, shows the pin assignments for all package types.

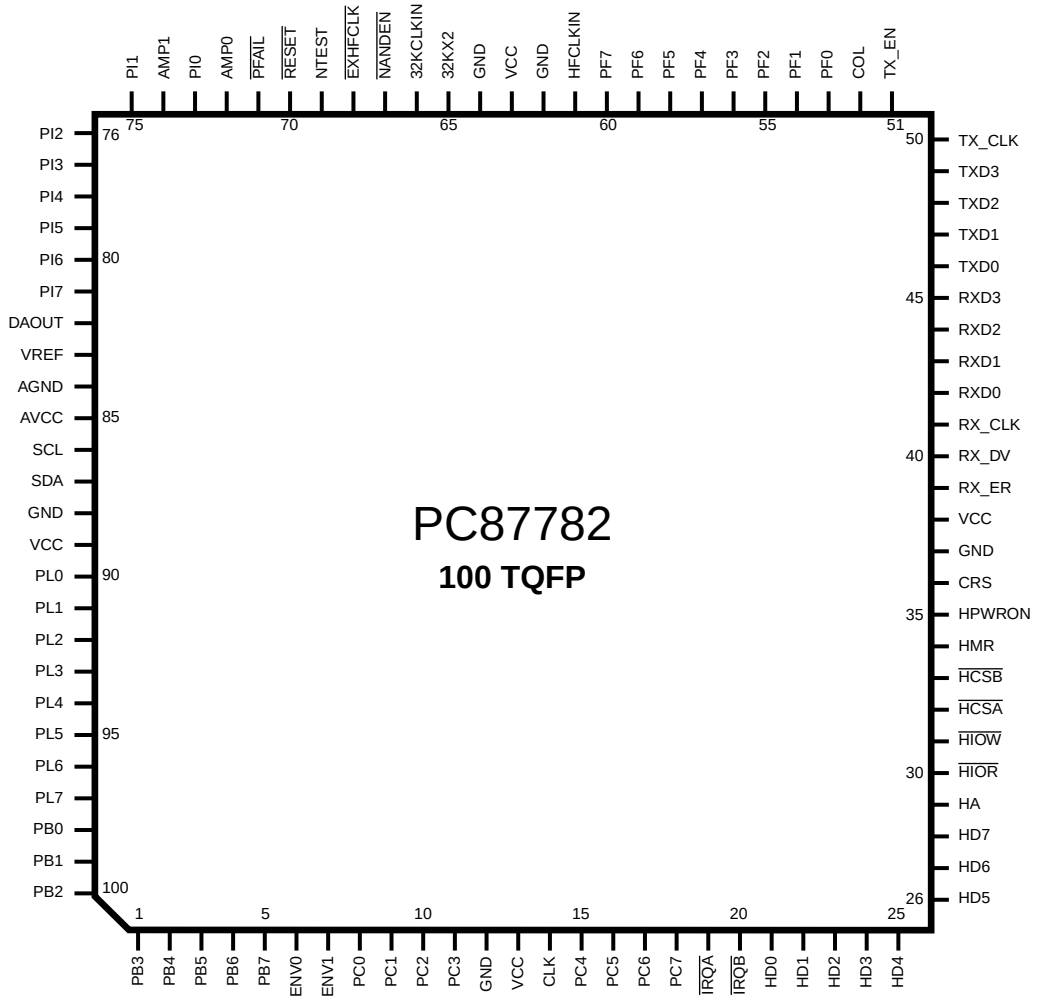
Pin Descriptions

The following tables describe the input pins, output pins, bi-directional input/output pins, and power supply pins of the PC87782. n these pin description tables, the following abbreviations are used to describe the pin types:



Order Number PC87782VUL
See NS Package VUL160A

Figure 2. Pin Assignments for PC87782 160-Pin Packages



Order Number PC87782VJG
See NS Package VJG100A

Figure 3. Pin Assignments for PC87782 100-Pin Packages

Table 2 Pin Descriptions

Signal Type	Input Parameters	Output Parameters	Buffer Description
TTL	V_{IH} V_{IL}		TTL Input Levels
Schmitt	V_{CHh}, V_{CHl}, V_{hys}		CMOS Input Levels with Hysteresis
CM		V_{OH}, V_{OL}	CMOS Output Buffer
CMHD2		V_{OHhd2}, V_{OLhd2}	CMOS Output Buffer with High Drive type 2
CM-TTL	V_{IH}, V_{IL}	V_{OH}, V_{OL}	CMOS Output buffer. Input TTL Characteristics
OD		V_{OL}	Open Drain Output
OD-TTL	V_{IH}, V_{IL}	V_{OL}	OD Output Buffer. Input TTL Characteristics
PU		R_{pu}, V_{OHpu}	Weak Pull Up Capability.
STRAP	V_{CHh}, V_{CHl}, V_{hys}	R_{pu}	An input with “Schmitt” characteristics and an internal PU resistor. This type of input is typically used for strap signals.
OSCIN			Oscillator Input [not characterized]

Table 2 Pin Descriptions

Signal Type	Input Parameters	Output Parameters	Buffer Description
OSCOUT			Oscillator Output [not characterized]
Analog in			A/D Analog Input signal
Analog out			D/A Analog output signal
Analog I/O			A/D Analog input/output signal
Analog FB			A/D Op-Amp Feedback
MII In	V_{IH} V_{IL} (TTL) V_{TRH} V_{TRL}		Ethernet IEEE 802.3u compliant input
MII Out		V_{OHm} V_{OLm}	Ethernet IEEE 802.3u compliant output

Table 3 Input Pins

Signal	Type	Pin Number		No. of Sig Pins	Function
		100-pin	160-pin		
32KCLKIN	TTL			1	32.768 KHz Oscillator Clock Input.
AMP(1,0)	Analog In			2	Analog Inputs to Op-Amps
ENV(1,0)	STRAP			2	Environment select strap pins. These pins define the device environment. They are sampled on all resets except HMR. ENV2 is permanently high in the 100-pin package.
ENV2	STRAP	N/A		1	
HA	TTL			1	Host Address line used in conjunction with the chip-select inputs to address registers on the Host Interface.
$\overline{\text{HIOR}}$	TTL			1	Host I/O Read. Active-low input that signals an I/O data read by the host processor.
$\overline{\text{HIOW}}$	TTL			1	Host I/O Write. Active-low input that signals an I/O data write by the host processor.
$\overline{\text{HCSA}}$	TTL			1	Host Chip Select A. Active-low input that indicates an access to Channel A by the host processor.
$\overline{\text{HCSB}}$	TTL			1	Host Chip Select B. Active-low input that indicates an access to Channel B by the host processor.
HMR	Schmitt			1	Host Master Reset
HPWRON	Schmitt			1	Host Power On. Indicates that the host power supply is on, and the host bus interface signals are valid. While HPWRON is low, the host inputs are ignored, and all outputs float.
$\overline{\text{NANDEN}}$	Schmitt			1	NAND Test Mode / ISE TRI-STATE Mode
$\overline{\text{PFAIL}}$	Schmitt			1	Power Fail Detected Input
$\overline{\text{RESET}}$	Schmitt			1	Master Reset. A low level resets the controller and inhibits HFCG frequency locking.
RXD0-3	MII In			4	MII Input data.
RX_CLK	MII In			1	MII Receive Clock
RX_DV	MII In			1	MII Receive Data Valid
RX_ER	MII In			1	MII Receive Error
COL	MII In			1	MII Collision Detect
CRS	MII In			1	MII Carrier Sense
TX_CLK	MII In			1	Transmit Clock Input
ISE	Schmitt	N/A		1	ISE Interrupt. reserved for use by the development system.

Table 3 Input Pins

Signal	Type	Pin Number		No. of Sig Pins	Function
		100-pin	160-pin		
VREF	Analog Input			1	Reference Voltage for the on-chip A/D and D/A circuits. An External Reference voltage should be connected to this input.
WAIT	TTL	N/A		1	WAIT signal for inserting Wait states into accesses to slow off-chip memories or peripherals.

Table 4 Output Pins

Signal	Type	Pin Number		No. of Sig Pins	Function
		100-pin	160-pin		
32KX2	OSCOUT			1	32.768 KHz Crystal Oscillator Interface output to crystal
CLK	CM			1	Processor System Clock
DAOUT	Analog out			1	Digital to Analog Converter Output.
IRQA, IRQB	CM			2	Interrupts from Host Interface channels A and B.
NTEST	CM			1	NAND Test Output.
TXD0-3	MII Out			4	MII Output data.
TX_EN	MII Out			1	MII Transmit Enable
A0-15	CM	N/A		16	Address A0 through A15. CR16A address to memory.
BST(2,1,0)	CM	N/A		3	Bus Status bits 0 through 2
PFS	CM	N/A		1	Pipe Flow Status.
PLI	CM	N/A		1	Pipe Long Instruction Status.
RD	CM	N/A		1	Output Enable.
SEL0	CM	N/A		1	Zone Select 0. Chip-select signal for the External Memory.
SEL1	CM	N/A		1	Zone Select 1. Used to select the off-chip Base Memory.
SELIO	CM	N/A		1	Chip-select signal for the I/O Expansion.
WR(1,0)	CM	N/A		2	Write control for bytes 0 and 1

Table 5 Input/Output Pins

Signal	Type	Pin Number		No. of Sig Pins	Function
		100-pin	160-pin		
HD0-7	CMHD2-TTL			8	Bi-directional Data bus used to interface the PC87782 to the peripheral data bus of a host.
PB0-7	CM-PU-Schmitt			8	Port B, bits 0 through 7.
PC0-7	CM-PU-Schmitt			8	Port C, bits 0 through 7.
PF0-7	CM-PU-TTL			8	Port F, bits 0 through 7
PI0-7	Analog I/O CM-PU-Schmitt			8	Analog inputs to the A/D converter. PI0 and PI1 can be analog feedback outputs from the Op-Amps. All Port I pins can be digital inputs or outputs.
PL0-7	CM-PU-Schmitt			8	Port L, bits 0 through 7

Table 5 Input/Output Pins

Signal	Type	Pin Number		No. of Sig Pins	Function
		100-pin	160-pin		
SCL	OD-TTL			1	ACCESS.bus Serial Clock signal
SDA	OD-TTL			1	ACCESS.bus data signal

Table 6 Power Supply

Signal	Pin Number		No. of Sig Pins	Function
	100-pin	160-pin		
AV_{CC}			1	Analog 5V power supply.
V_{CC}			4	Digital 5V power supply.
AGND			1	Analog ground, for A/D and D/A.
GND			4	Ground for on-chip logic and output drivers.
V_{CC}	N/A		2	Digital 5V power supply.
GND	N/A		8	Ground for on-chip logic and output drivers.

Memory Map

The CompactRISC architecture supports a uniform linear address space of 256K bytes. The PC87782 implementation of this architecture uses only the lowest 128K bytes of address space, ranging from 00000 to 1FFFF hex. The remaining 128K bytes (20000 to 3FFFF hex) are not used by the device.

Table 7 is a memory map showing the types of memory and peripherals that occupy this memory space. Address ranges not listed in the table are reserved and should not be read or written.

Table 7 PC87782 Memory Map

Address (hex)	Size	Description	BIU Zone
00000 – 07FFF	32K	Base Memory	Zone 0
08000 – 0DFFF	24K	Reserved	
0E000 – 0E1FF	512	LAN Receive Buffer RAM	N/A
0EA90 – 0F56F	2784	System RAM	
0F800 – 0F87F	128	LAN Transmit Buffer RAM	
0F900 – 0F98F		BIU Registers	
0FB00 – 0FBFF	256	I/O Expansion	
0FC00 – 0FFFF		On-chip module registers	
10000 – 1FFFF	64K	Off-Chip Memory	Zone1 (IRD mode only)
20000 – 3FFFF	120K	Reserved	Zones 2-3

Table 8 is a detailed memory map showing the specific memory address of the memory, I/O ports, and registers. The table shows the starting address, the size, and a brief description of each memory block and register. For detailed information on using these memory locations, see the applicable sections in the data sheet.

All addresses not listed in the table are reserved and should not be read or written. An attempt to access an unlisted address will have unpredictable results.

Each byte-wide register occupies a single address and can be accessed only in a byte-wide transaction. Each word-wide register occupies two consecutive memory addresses and can be accessed only in a word-wide transaction. Both the byte-wide and word-wide registers reside at word boundaries (even addresses). Thus, each byte-wide register uses only the lowest eight bits of the internal data bus.

Most PC87782 registers are read/write registers. However, some registers are read-only or write-only, as indicated in the table. An attempt to read a write-only register or to write a read-only register will have unpredictable results.

When the software writes to a register in which one or more bits are reserved, it must write a zero to each reserved bit unless indicated otherwise in the description of the register. Reading a reserved bit returns an undefined value.

Table 8 PC87782 Detailed Memory Map (Sheet 1 of 3)

Starting Address (hex)	Size	Contents
0000	32K	Base Memory (ROM and/or RAM, depending on environment)
8000	24K	Reserved
E000	512	LAN Receive Buffer RAM
EA90	2784	System RAM (EA90-F56F hex)
F800	128	LAN Transmit Buffer RAM
F900	byte	BCFG, BIU Configuration Register
F902	word	I/O Configuration Register
F904	word	SZCFG0, Static Zone 0 Configuration Register
F906	word	SZCFG1, Static Zone 1 Configuration Register
F910	byte	MCFG, Module Configuration Register
F912	byte	DBGCFG, Debug Configuration Register
F914	byte	MSTAT, Module Status Register (read-only register)
F918	byte	DBGFRZEN, Debug Freeze Enable Register
FB00	byte	PBDIR, Port B Direction Register
FB02	byte	PBDIN, Port B Data Input Register
FB04	byte	PBDOUT, Port B Data Output Register
FB06	byte	PBWKPU, Port B Weak Pull-Up Register
FB10	byte	PCDIR, Port C Direction Register
FB12	byte	PCDIN, Port C Data Input Register
FB14	byte	PCDOUT, Port C Data Output Register
FB16	byte	PCWKPU, Port C Weak Pull-Up Register
FC00	word	LNIFCTL, LAN Interface Control Register
FC02	word	LNRBFCTL, LAN Receive Buffer Control Register
FC02	word	LNRXCTL, LAN Receive Control Register
FC04	word	LNTXCTL, LAN Transmitter Control Register
FC08	word	LNRFCR, LAN Receiver Filter Control Register
FC0A	word	LNRFDR, LAN Receiver Filter Data Register
FC0C	word	LNTXSTAT, LAN Transmitter Status Register
FC10	word	LNIPND, LAN Interrupt Pending Register
FC12	word	LNIEN, LAN Interrupt Enable Register
FC14	word	LNICL, LAN Interrupt Clear Register
FC20	word	LNMSGLEN0, LAN Message Length Register 0
FC22	word	LNMSGSTAT0, LAN Message Status Register 0
FC24	word	LNMSGLEN1, LAN Message Length Register 1
FC26	word	LNMSGSTAT1, LAN Message Status Register 1
FC28	word	LNMSGLEN2, LAN Message Length Register 2
FC2A	word	LNMSGSTAT2, LAN Message Status Register 2
FC2C	word	LNMSGLEN3, LAN Message Length Register 3
FC2E	word	LNMSGSTAT3, LAN Message Status Register 3
FC40	byte	RSTSTAT, Reset Status Register
FC60	byte	PMCSR, Power Management Control/Status Register
FC80	byte	WKEDG1, Wake-Up Edge Detection Register 1

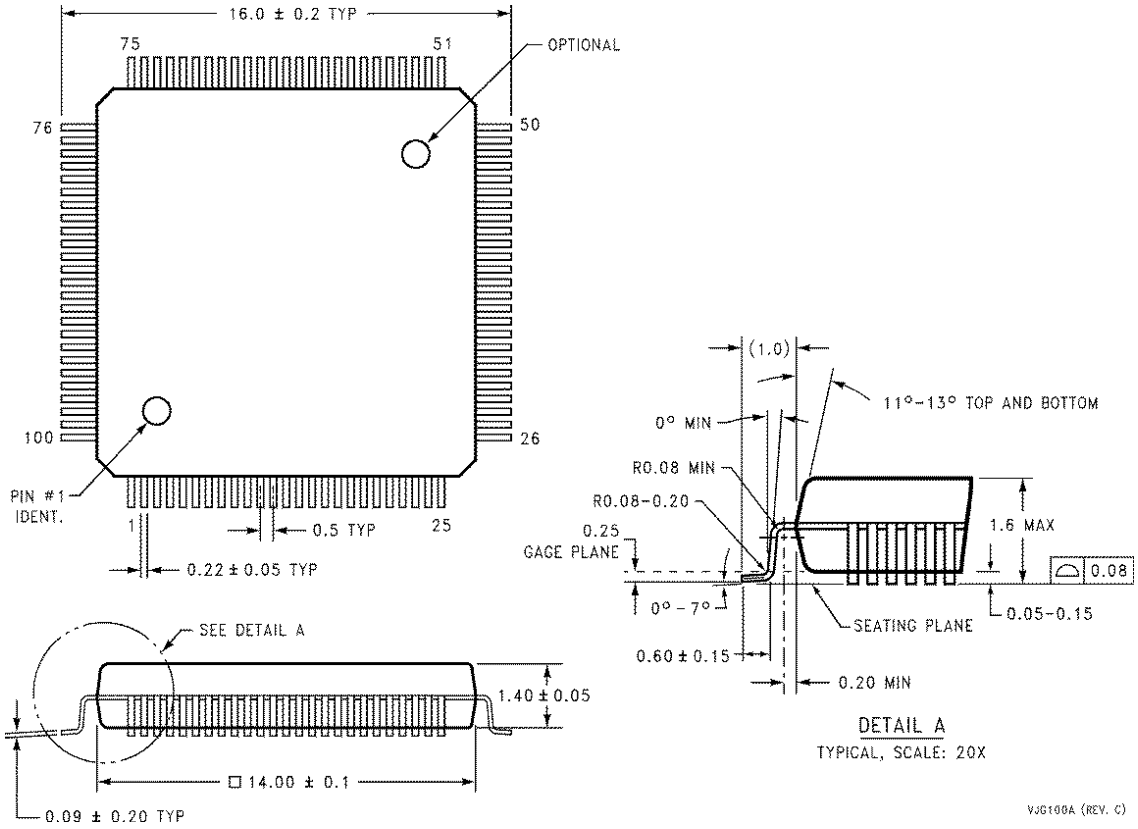
Table 8 PC87782 Detailed Memory Map (Sheet 2 of 3)

Starting Address (hex)	Size	Contents
FC82	byte	WKENA1, Wake-Up Enable Register 1
FC86	byte	WKPND1, Wake-Up Pending Register 1 (read/set register)
FC88	byte	WKCL1, Wake-Up Pending Clear Register 1 (write-only register)
FCA0	byte	WKEDG2, Wake-Up Edge Detection Register 2
FCA2	byte	WKENA2, Wake-Up Enable Register 2
FCA6	byte	WKPND2, Wake-Up Pending Register 2 (read/set register)
FCA8	byte	WKCL2, Wake-Up Pending Clear Register 2 (write-only register)
FD00	byte	FSCNTL, Fan-Speed Control Register
FD02	byte	FSCNTR, Fan-Speed Counter Register
FD04	byte	FSDBG, Fan-Speed Debug Register
FD20	byte	PFALT, Port F Alternate Function Register
FD22	byte	PFDIR, Port F Direction Register
FD24	byte	PFDIN, Port F Data Input Register
FD26	byte	PFOUT, Port F Data Output Register
FD28	byte	PFWKPU, Port F Weak Pull-Up Register
FE00	byte	IVCT, Interrupt Vector Register (read-only)
FE02	byte	NMISTAT, NMI Status Register (read-only)
FE04	byte	EXNMI, External NMI Control/Status Register
FE0A	byte	ISTAT0, Interrupt Status Register 0 (read-only)
FE0C	byte	ISTAT1, Interrupt Status Register 1 (read-only)
FE0E	byte	IENAM0, Interrupt Enable and Mask Register 0
FE10	byte	IENAM1, Interrupt Enable and Mask Register 1
FEA0	byte	HICTRL, Host Interface Control Register
FEA2	byte	HIIRQC, Host Interface IRQ Control Register
FEA4	byte	HISEST, Host Interface System Environment Status Register
FEA6	byte	HISEDO Host Interface System Environment Data Out Buffer (write-only)
FEAA	byte	HISEDI, Host Interface System Environment Data In Buffer (read-only)
FEAC	byte	HIPMST, Host Interface Power Management Port Status Register
FEAE	byte	HIPMDO, Host Interface Power Management Data Out Buffer (write-only)
FEB0	byte	HIPMDI, Host Interface Power Management Data In Buffer (read-only)
FEC0	byte	ACBSDA, ACB Serial Data Register
FEC2	byte	ACBST, ACB Status Register (read-only)
FEC4	byte	ACBCST, ACB Control Status Register
FEC6	byte	ACBCTL1, ACB Control 1 Register
FEC8	byte	ACBADDR, ACB Own Address Register
FECA	byte	ACBCTL2, ACB Control 2 Register
FEE2	byte	PIDIR, Port I Direction Register
FEE4	byte	PIDIN, Port I Data Input Register
FEE6	byte	PIOUT, Port I Data Output Register
FEE8	byte	PIWKPU, Port I Weak Pull-Up Register
FF00	byte	PLALT, Port L Alternate Function Register
FF02	byte	PLDIR, Port L Direction Register

Table 8 PC87782 Detailed Memory Map (Sheet 3 of 3)

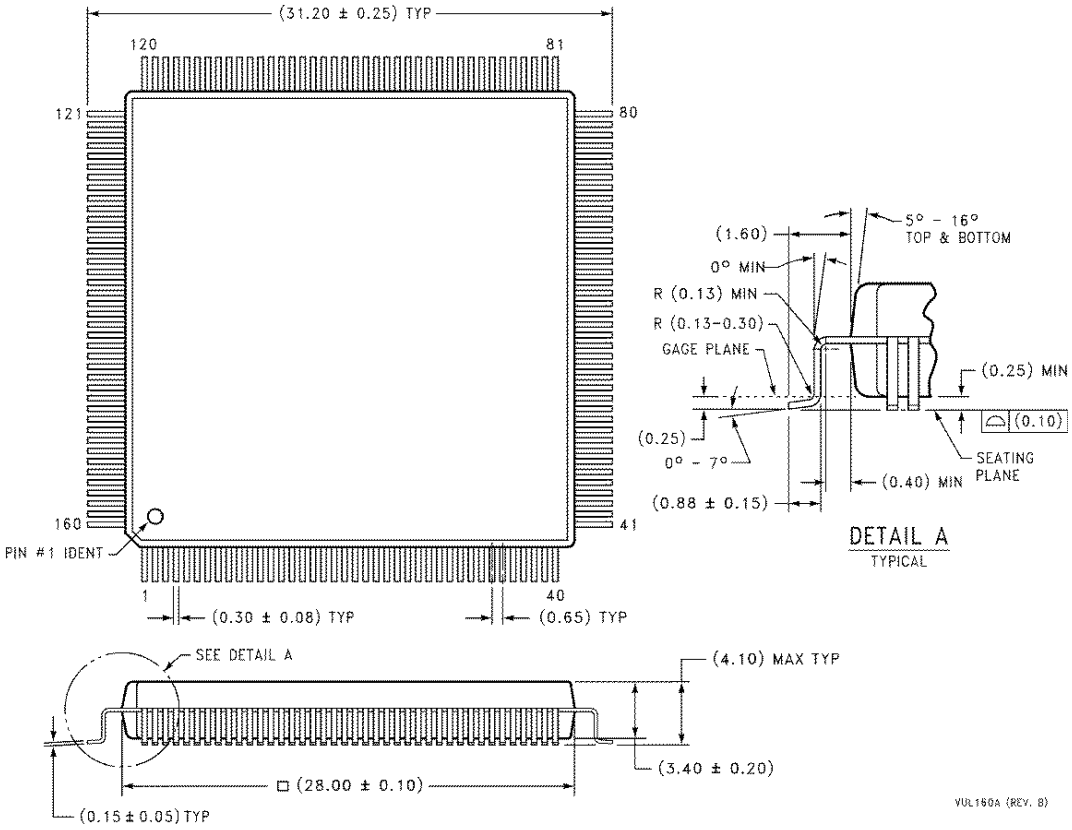
Starting Address (hex)	Size	Contents
FF04	byte	PLDIN, Port L Data Input Register
FF06	byte	PLOUT, Port L Data Output Register
FF08	byte	PLWKPU, Port L Weak Pull-Up Register
FF20	byte	TWCFG, Timer and Watchdog Configuration Register
FF22	byte	TWCP, Timer and Watchdog Clock Prescaler Register
FF24	word	TWMT0, TWM Timer 0 Register
FF26	byte	T0CSR, TWMT0 Control and Status Register
FF28	byte	WDCNT, Watchdog Count Register (write-only)
FF2A	byte	WDSDM, Watchdog Service Data Match Register (write-only)
FF40	byte	DACCTRL, D/A Converter Control Register
FF42	byte	DACDATA, D/A Converter Data Register
FFA0	byte	HFCGCTRL, High-Frequency Clock Generator (HFCG) Control Register
FFA2	byte	HFCGML, HFCG M Value Low Register
FFA4	byte	HFCGMH, HFCG M Value High Register
FFA6	byte	HFCGN, HFCG N Value Register
FFA8	byte	HFCGIL, HFCG I Value Low Register
FFAA	byte	HFCGIH, HFCG I Value High Register
FFC0	byte	ADCST, A/D Converter Status Register
FFC2	byte	ADCCNT1, A/D Converter Control 1 Register
FFC4	byte	ADCCNT2, A/D Converter Control 2 Register
FFC6	byte	ADCCNT3, A/D Converter Control 3 Register
FFCA	byte	ADDATA0, A/D Converter Data 0 Register (read-only)
FFCC	byte	ADDATA1, A/D Converter Data 1 Register (read-only)
FFCE	byte	ADDATA2, A/D Converter Data 2 Register (read-only)
FFD0	byte	ADDATA3, A/D Converter Data 3 Register (read-only)

Physical Dimensions inches (millimeters) unless otherwise noted



100-Lead (14 x 14 mm) Molded Plastic QFP: VJG100A
Order Number PC87782VJG
See NS Package VJG100A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



160-Lead (28 x 28 mm) Molded Plastic QFP: VUL160A
Order Number PC87782VUL
See NS Package VUL160A

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