ADPCM codec for digital cordless telephone PCD5032

The PCD5032 is a CMOS device designed for use in Digital European Cordless Telephone systems (DECT) but it is also suited for other cordless telephony applications (e.g., CT2). The PCD5032 performs A/D and D/A conversion, ADPCM encoding and decoding compliant to CCITT recommendation G.721 (blue book 1988). The PCD5032 allows direct connection to external microphone and earpiece. The device can be used in both handset and base–station designs.

This objective specification contains advance information and is subject to change without notice.

FEATURES

- G.721 compliant ADPCM encoding and decoding
- 'Bitstream' A/D and D/A conversion
- On–chip receive and transmit filter
- On–chip ringer and tone generator
- Programmable gain of receive and transmit path
- Serial ADPCM interface with independent timing for maximum flexibility
- Linear PCM data accessible for digital echo cancelling
- Programmable via I^2C interface
- Fast receiver mute input via pin
- On–chip voltage reference
- On–chip symmetrical supply for electret microphone
- Few external components; direct connection to microphone and earpiece
- Low power consumption in standby mode
- Low supply voltage (single supply 2.7 V up to 5.5 V)
- CMOS technology
- Minimized EMC on digital outputs

APPLICATIONS

- Digital European Cordless Telephony (DECT)
- CT2 cordless
- Speech compression

PACKAGE OUTLINE

S028 (SOT136A) QFP44S14 (SOT205AG)

1.0 BLOCK DIAGRAM

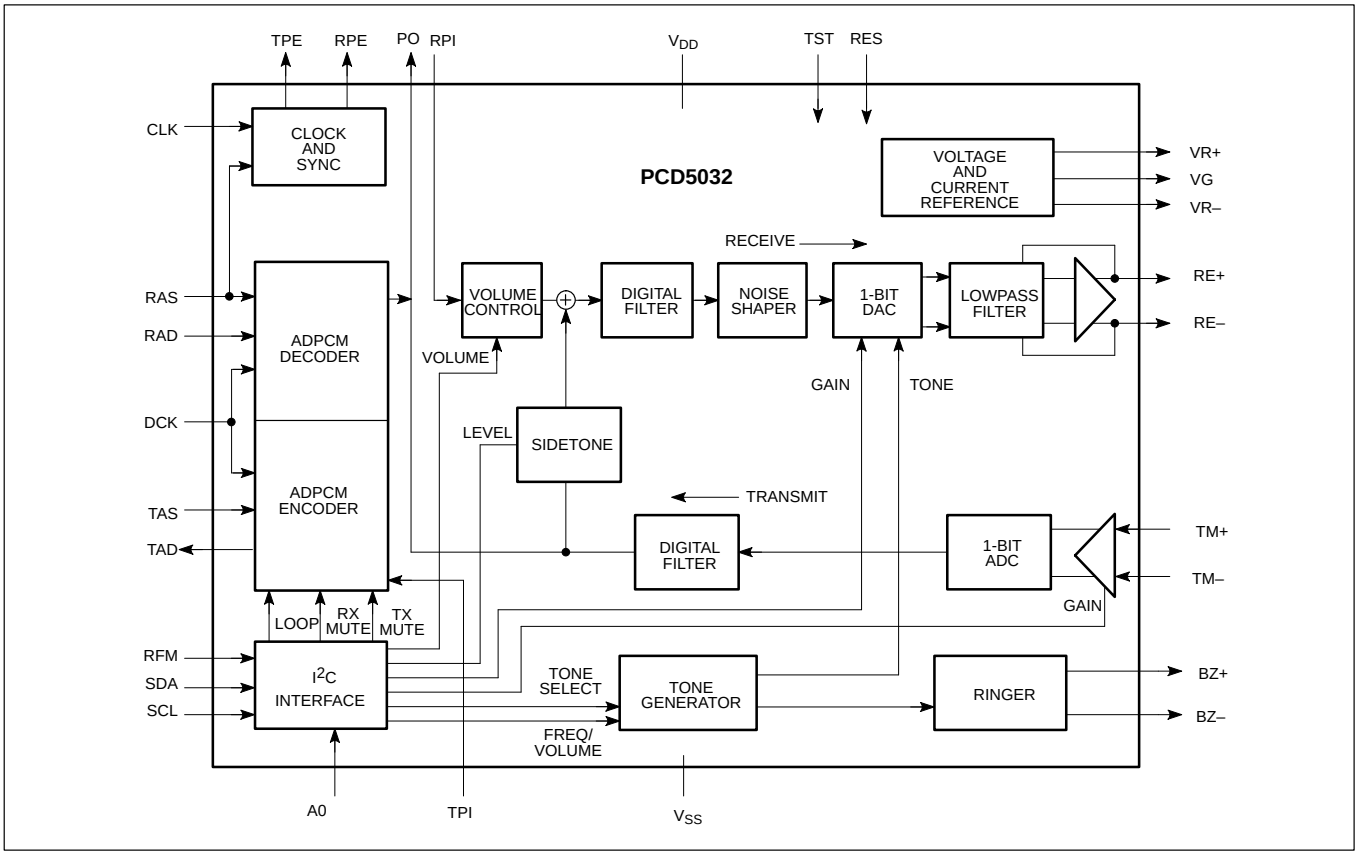

Figure 1. Block Diagram

2.0 PINNING

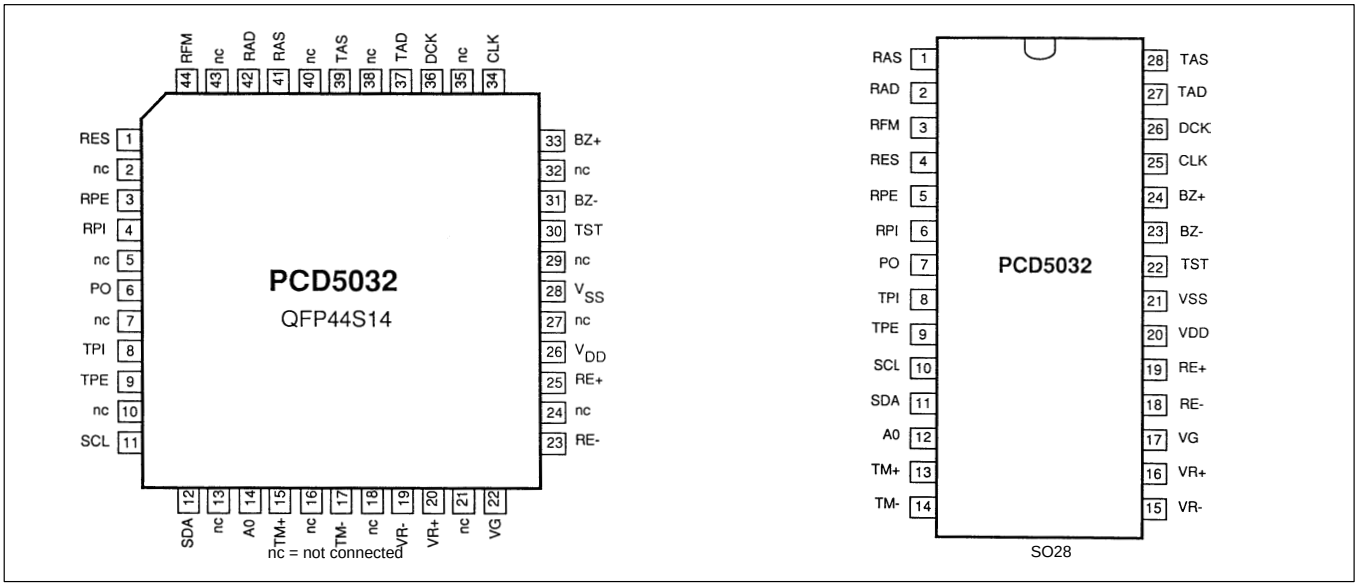

Figure 2. Pin Configuration

2.1 Pin Description

Pin	Name	I/O	Description
General			
26	V_{DD}	–	Positive power supply (2.7V – 5.5V)
28	V_{SS}	–	Negative power supply (0V)
22	VG	O	Analog signal ground
20	VR+	O	Positive reference voltage (1)
19	VR–	O	Negative reference voltage (1)
Digital			
34	CLK	I	Clock input
36	DCK	I	Data clock (ADPCM)
41	RAS	I	Receiver ADPCM sync (2)
42	RAD	I	Receiver ADPCM data input (2)
4	RPI	I	ReceiverPCM input (2)
3	RPE	O	Receiver PCM output enable (2)
44	RFM	I	Receiver fast mute (2)
39	TAS	I	TransmitterADPCM sync (2)
37	TAD	O	Transmitter ADPCM data output (2)
8	TPI	I	Transmitter PCM input (2)
9	TPE	O	Transmitter PCM output enable (2)
6	PO	O	PCM data output
12	SDA	I/O	I^2C serial data input / acknowledge
11	SCL	I	I^2C clock input
14	A0	I	I^2C address select pin
1	RES	I	Reset input (active high)
30	TST	I	Test mode (3)
Analog			
33	BZ+	O	Ringer output
31	BZ–	O	Ringer output
15	TM+	I	Transmitter audio input (microphone)
17	TM–	I	Transmitter audio input (microphone)
25	RE+	O	Receiveraudio output (earpiece)
23	RE–	O	Receiver audio output (earpiece)

NOTES:
1. Internally generated, intended for electret microphone supply.
2. Definition: Receiver= direction from ADPCM interface to earpiece; Transmitter = direction from microphone to ADPCM interface.
3. To be connected to Vss in normal application.

3.0 FUNCTIONAL DESCRIPTION

3.1 Digital interfaces (see Fig.1 Block diagram)

3.1.1 ADPCM interface

The ADPCM interface pins (RAD, TAD) carry 4 bits of serial data. Transmit and receiver data both are controlled by separate synchronization pins (RAS, TAS).

Upon detection of a high RAS signal (with rising DCK edge), the receiver will read 4 ADPCM bits on the next 4 high–to–low transitions of the DCK data clock. Likewise, upon reception of a high TAS signal, the transmitter will output 4 ADPCM bits on the next 4 low–to–high transitions of DCK. Figure 5 shows the timing diagram. During the time that the ADPCM data output (TAD) is not activated, it will be in a high impedance state, enabling a bus structure to be used in multi–line base stations. Input RAD has an internal pull–down resistor.

The minimum frequency on the DCK input is $f_{CLK}/54$. the maximum value equals the clock frequency, and any frequency in between may be chosen. The RAS signal controls the start of each conversion in a frame at an 8 kHz rate. The master clock ‘CLK’ must be locked to the frequency of ‘RAS’, with a ratio $f_{CLK} = 432 \times f_{RAS}$.

3.1.2 PCM Interface

To enable additional data processing in a base station both transmit and receive linear PCM data paths are accessible.

For the receive direction the PCM data is output on pin PO and read from pin RPI. For the transmit direction the PCM data is output on pin PO and read from pin TPI. To enable bus structures to be used in base stations the PCM output PO is in high impedance state when not active. Inputs TPI/RPI have internal pull–down.

In a typical (handset) application pin PO is directly connected to RPI and TPI. If additional data processing is required (e.g., echo cancellation in a base–station), then a data processing unit may be placed between PO and RPI or PO and TPI.

The data format is serial, 2’s complement, MSB first. PO outputs 16 bits (14 data bits followed by 2 zeroes). TPI/RPI read 14 data bits. The bit frequency is 3456 kHz (CLK). Data output PO changes on the falling edge of CLK. Data inputs TPI/RPI are read on the rising edge of CLK (Figures 7,8).

For interfacing to digital signal processors signals TPE and RPE (both active low) mark the position of the transmit and receive PCM data on pin PO (Figure 6). TPE/RPE change on the rising edge of CLK.

Outputs RPE and TPE have low impedance only from half a CLK cycle before to half a CLK cycle after the active state. The rest of the time they are in high impedance state. Thus a wired–OR configuration can be made when only one DSP serial input port is used for reading both transmit and receive data. An external pull–up is required.

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3.1.3 I²C Interface

The Philips I2C interface is used for programming gain and mode of operation.

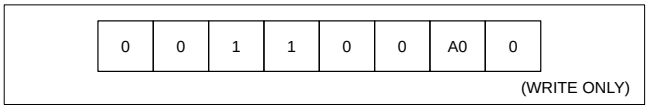

Figure 3. I²C Address

With the address select pin A0 it is possible to have two independently programmed ADPCM codecs in a base station (two outside lines). If more codecs are used in one base station then the address pin can be used as a 'select' signal. For timing of the I²C bus, see Philips Semiconductors' brochure "The I²C–bus and How to Use It".

Each function can be accessed by writing one 8–bit data word to the ADPCM codec. For this reason the 8–bit word is divided into two fields:

bit7, bit6 : function

bit5 to bit0 : value/setting.

Table 1. Overview of the I²C Programming Possibilities

Function	b7	b6	b5	b4	b3	b2	b1	b0
Operation Mode	0	0	–	–	TONE	PON	T1	T0
Receiver Control	0	1	RV2	RV1	RV0	RG2	RG1	RG0
Transmitter Control	1	0	ST1	ST0	MUTE	TG2	TG1	TG0
Ringer	1	1	BF2	BF1	BF0	BV2	BV1	BV0

Definitions

TONE : 'tone/ringer' section for tone generator output; tones can be sent to ringer or receiver DAC
PON : power-on (active)
T1-T0 : test loops
RG2-RG0 : receiver gain
TG2-TG0 : transmitter gain
RV2-RV0 : receiver volume
BV2-BV0 : tone volume
BF2-BF0 : tone frequency
ST1-ST0 : sidetone level

Programming the ADPCM codec is possible in active mode as well as in standby mode. A reset clears all I²C registers.

3.1.4 Fast Mute

The RFM (Receiver Fast Mute) pin enables fast muting of the received signal if erroneous data is present on the ADPCM interface.

Muting is done in the same manner as the receiver mute via I²C bus. The input data of the ADPCM decoder is blanked, so that the ADPCM decoder output signal goes to zero. To ensure immediate silence on the analog outputs RE+/RE–, the linear PCM input data of the receive filter is set to zero as well.

If the mute signal is switched off again, then the ADPCM decoder output settles gradually from zero to the appropriate PCM signal level. No audible clicks will occur.

The sidetone level is not affected by the mute function.

3.2 Analog Parts and I²C Programming

3.2.1 Input/Output

The analog input pins (TM+, TM–) can be connected directly to a microphone. For electret microphones capacitive coupling is required (Figure 11). The earpiece must be a low ohmic device (>100Ω differential).

The microphone and earpiece amplifiers have the possibility of gain control via the I²C interface. Further the sending and receiving direction can be muted separately. Analog gain control for the receive path can be set in steps of 1 dB. Digital volume control can be set in 6 dB steps. The following table gives an overview of the programming possibilities.

Table 2. Overview of Gain Control Options

Function	I²C-code	Description	Note
Receiver gain (relative)	01xxx101	-3dB	
	01xxx110	-2dB	
	01xxx111	-1dB	
	01xxx000	0dB	default
	01xxx001	+1dB	
	01xxx010	+2dB	
	01xxx011	+3dB	
	01xxx100	+4dB	
Receiver volume	01000xxx	0dB	defaults
	01001xxx	-6dB	
	01010xxx	-12dB	
	01011xxx	-18dB	
	01100xxx	-24dB	
	01101xxx	-30dB	
	01110xxx	-36dB	
	01111xxx	RX MUTE	
Transmitter gain (relative)	10xxx101	-3dB	
	10xxx110	-2dB	
	10xxx111	-1dB	
	10xxx000	0dB	default
	10xxx001	+1dB	
	10xxx010	+2dB	
	10xxx011	+3dB	
	10xxx100	+4dB	
Transmitter mute	10xx1xxx	TX MUTE	default off

3.2.2 Sidetone

With the I²C interface the (local) sidetone Level can be set to –12, –18, –24 dB, or switched off. See Table 3. The sidetone level is independent of the receiver volume control setting.

Table 3. Sidetone Level Options

Function	I²C-code	Description	Note
Sidetone	1000xxxx	No local sidetone	default
	1001xxxx	Level = -12 dB	
	1010xxxx	Level = -18 dB	
	1011xxxx	Level = -24 dB	

3.2.3 Tone Generator and Ringer

The PCD5032 contains a programmable tone generator which can be used for generating ringer tones (BZ+, BZ–) or local information tones in the receive path (RE+, RE–).

By setting the TONE bit (b3) in the operation mode register the tone output will be directed to the receiver DAC, otherwise the tones will be sent to the ringer output stage. Table 4 shows the possible frequency and volume settings.

Table 4. Tone Output Frequency/Volume Options

Function	I²C-code	Description	Note
Volume (rel)	11xxx000	Signal off	default
	11xxx001	-29 dB	sine wave
	11xxx010	-23 dB	sine wave
	11xxx011	-17 dB	sine wave
	11xxx100	-11 dB	sine wave
	11xxx101	-5 dB	sine wave
	11xxx110	0 dB	sine wave
	11xxx111	+4 dB	squarewave
Frequency	11000xxx	400 Hz	
	11001xxx	421 Hz	
	11010xxx	444 Hz	
	11011xxx	800 Hz	
	11100xxx	1000 Hz	
	11101xxx	1067 Hz	
	11110xxx	1333 Hz	
	11111xxx	2000Hz	

The ringer output (BZ) is differential and is intended for low ohmic devices. If the ringer is switched off then both outputs are low. The output signal is a pulse density modulated block wave (on a 32 kHz basic pulse rate) to generate a sinewave–like output signal, see Figure 4. Volume is controlled by changing the pulse width of each pulse. In the square wave mode a full square wave is generated and results in the maximum volume. The volume settings (in dB) are given for the first harmonic signal component.

3.3 Modes of Operation

The ADPCM codec has three modes of operation, a normal mode and two loop modes. See the table below for details on setting these modes. Also the standby and active mode are set via the I²C bus.

Table 5. Modes of Operation

Function	I²C-code	Description	Note
Standby mode	00xxx0xx	Power down	default
Active mode	00xxx1xx	Active	
Set Normal mode	00xxxx01	Normal operation	default
Set Loop 1	00xxxx01	Loopback on ADPCM side and on PCM side without using ADPCM transcoder	
Set Loop 2	00xxxx10	Loopback on TM+/TM– to RE+/RE– through ADPCM transcoder	

3.3.1 Standby Mode

After a reset the ADPCM codec will by default be in standby mode. All I²C settings will be cleared. PON=O sets the codec in standby

mode. In standby mode all circuits are switched off, except for the I^2C interface. Before going to standby mode the PCD5032 performs a reset of the ADPCM transcoder, digital filters and auxiliary logic functions. The I^2C interface registers are not cleared.

3.3.2 Active Mode

PON=1 in the operation mode register sets the codec in active mode. In active mode the ADPCM codec can be operated either in normal mode or one of the two test loops may be selected.

3.3.3 Test Loops

Both test loops can be used for test or evaluation purposes.

Loop 1 is intended for testing the audio path and A/D, D/A converters, the ADPCM transcoder is not addressed in this mode. The ADPCM data is directly looped back towards the radio interface. The PCM data is looped from transmit filter output to receive filter input.

Loop 2 is intended for testing the complete audio path including ADPCM encoding and decoding.

3.3.4 Reset (input RES)

After an external reset pulse the circuit will perform an internal reset procedure. The reset pulse must be active during at least 10 CLK cycles. 125 μs (one 8kHz period) after RES has gone low, the internal reset is completed and the PCD5032 goes into standby mode. At that moment the ADPCM codec is ready to be programmed.

A reset clears all I^2C registers and resets the ADPCM transcoder, digital filters and auxiliary logic functions.

4.0 CHARACTERISTICS

4.1 MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	RATING	UNITS
Supply voltage $V_{DD} - V_{SS}$	-0.5 to +6.5	V
Voltage at any pin except V_{DD}	V_{SS} -0.5 to V_{DD} +0.5	V
DC current through pin: V_{DD}, V_{SS} BZ+, BZ–, RE+, RE– other pins	 150 150 50 10	mA
Total power dissipation	500	mW
Operating ambient temperature	–25 to +70	°C
Storage temperature	–65 to +150	°C

Handling

Inputs and outputs are protected against electrostatic discharge in normal handling. ESD protection according to Human Body Model is guaranteed up to 800 V. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see‘Handling MOS Devices’).

4.2 ELECTRICAL CHARACTERISTICS

V_{DD} = 3.0 V, CLK = 3456 kHz

PARAMETER	LIMITS			UNITS
	MIN	TYP	MAX	
General				
Operating temperature	-25	25	70	°C
Supply voltage	2.7	3.0	5.5	V
Supply current (T_{amb} = 25°C)[1] Active (no load) Standby	 – –	 7 20	 14 100	 mA µA
Leakage current inputs	–	–	1	µA
Analog ground	0.48	0.5	0.52	xV_{DD}
Reference voltage VR+[2]	0.8	1.0	1.2	V
Reference voltage VR–[2]	–0.8	–1.0	–1.2	V
Digital I/O				
V_{IH}[3]	0.7	–	1.0	xV_{DD}
V_{IL}[3]	0	–	0.3	xV_{DD}
V_{OL}[3]	–	–	0.4	V
V_{OH}[3]	V_{DD} – 0.4		V_{DD}	V
Pull-down resistor[3]	–	150	–	kΩ
DCK frequency[4]	f_{CLK}/54 = 64	–	f_{CLK}	kHz
RAS, TAS frequency[4]	–	8	–	kHz
I^2C Bus Timing				
SCL clock frequency	–	–	100	kHz
Tolerable spike width	–	–	50	ns
Bus free time	4.7	–	–	µs
Start condition set–up time	4.7	–	–	µs
Start condition hold time	4.0	–	–	µs
SCL LOW time	4.7	–	–	µs
SCL H IGH time	4.0	–	–	µs
SCL and SDA rise time	–	–	1.0	µs
SCL and SDA fall time	–	–	0.3	µs
Data set–up time	250	–	–	ns
Data hold time	0	–	–	ns
Stop condition set–up time	4.0	–	–	µs
Analog Inputs[5]				
TM+ / TM– input impedance[6]	–	125	–	kΩ
Nominal input level[7]	–	12	–	mV_{RMS}
Maximum input signal[8]	–	56	–	mV_{RMS}
Min. voltage gain	–4	–3	–2	dB
Max. voltage gain	+3	+4	+5	dB
Stepsize voltage gain	–	1	–	dB
TX harmonic distortion[9]	–	–	–40	dB

ELECTRICAL CHARACTERISTICS (conitnued)

PARAMETER	LIMITS			UNITS
	MIN	TYP	MAX	
Analog Outputs				
Receiver audio output:				
output impedance[6]		10		Ω
signal level at 0 dBm0[10]		550		mV_{RMS}
signal level at 3.14 dBm0[11]		1250		mV_{RMS}
min. gain	–4	–3	–2	dB
max. gain	+3	+4	+5	dB
gain step size	–	1	–	dB
volume control range	–36	–	0	dB
volume stepsize	–	6.0	–	dB
RX harmonic distortion[12]	–	–	–40	dB
Ringer output:[5,13]				
output impedance	–	14	29	Ω
volume control range	–29	–	+4	dB

FILTER CHARACTERISTICS

PARAMETER	LIMITS			UNITS
	MIN	TYP	MAX	
Transmitter				
Passband ripple (300–3000Hz)	–	–	0.5	dB
Frequency response				
f = 50 Hz	–35			
f = 3400 Hz			–2	dB
f = 4600 Hz	–35			
f = 8000 Hz	–60			
Analog-to-Digital Converter				
Signal-to-noise ratio (Figure 12)[6,14]		35		dB
Digital-to-Analog Converter				
Signal-to-noise ratio (Figure 12)[6,14]		35		dB
Group Delay				
Transmitter[15]			400	µs
Receiver[15]			525	µs
Group Delay Distortion				
See Figure 9				

NOTES: +3.14 dBm0 is the maximum signal level on the PCM interface. Specifications are valid in active mode (except standby current).

1. I_{DD} active measured with all inputs to V_{SS}, except CLK, DCK connected to 3.456 MHz, and RAS, TAS connected to 8 kHz. I_{DD} standby measured with all inputs connected to V_{SS}, except TMP, TMM left open. All outputs left open for both cases.
2. The ref. voltage is available on VR+ and VR– and is measured with respect to VG. The voltage outputs are intended for electret microphone supply, and can deliver 400 µA.
3. Digital inputs and outputs are CMOS–levels compatible. The outputs can sink or source 1 mA. Pull–down resistors are present at pins RPI, TPI, TST, RAD.
4. Any frequency between min and max is allowed for DCK. The signals CLK and RAS/TAS must be frequency–locked. and wilt have a ratio $f_{CLK} / f_{RAS} = 432$.
5. All analog input/output voltages and impedances are measured differentially. The circuit is designed for use with an electret microphone.
6. Frequency band is 300 Hz – 3400 Hz. Maximum load capacitance = 100 pF differentially, or 200 pF each pin.
7. Nominal signal level gives –10 dBm0 on the PCM interface (G.71 1/G.712). Value given for TX gain setting 0 dB.
8. Maximum signal level gives +3.14 dBm0 on the PCM interface, with larger input signals the digital output signal will be saturated. Value given for TX gain setting 0dB.
9. TX gain setting = 0 dB and input signal level 40 mV_{RMS} (will generate 0 dBm0 signal level on PCM interface according to G.711).
10. PCM signal level is 0 dBm0 and RX gain setting 0 dB. With a load of 300 Ω between RE+ and RE– the given signal level results in an output power of 1 mW. The maximum output current is 10 mA.
11. PCM signal level is +3.14 dBm0 and RX gain setting +4 dB. The maximum output current is 10 mA.
12. PCM signal level is 0dBm0 (G.711).
13. For maximum output power the load resistance should equal the typical output impedance (specified at I_{LOAD} – 20 mA). The minimum load resistance is limited by the “Maximum Ratings”.
14. Measured with psophometric filter (CCITT G.223). Only fulfilled at V_{DD} noise level smaller than 40 mV_P (0 – 20 kHz). Measured on sample basis at V_{DD} = 3.0 V, temperature = 25°C, compliant with G.712. Signal level is –40 dBm0 on PCM interface (0.4 mV_{RMS} on analog input). Gain setting is 0 dB.
15. Group delay includes ADPCM / PCM conversion; signal frequency = 1.5 kHz. Figure is given for RAS/TAS signals at the same moment.

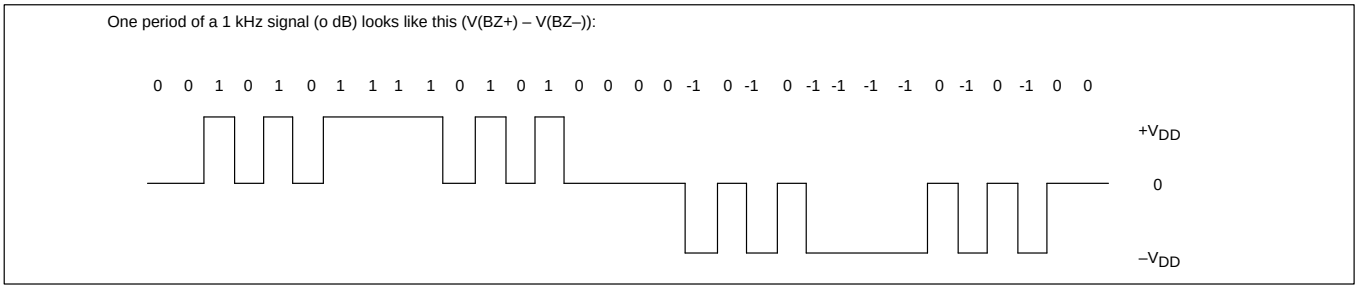

Figure 4. Tone Output Example

TIMING DIAGRAMS

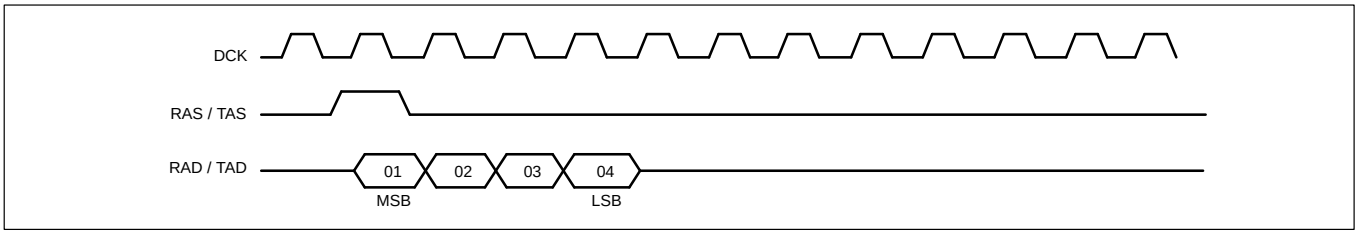

Figure 5. ADPCM Timing

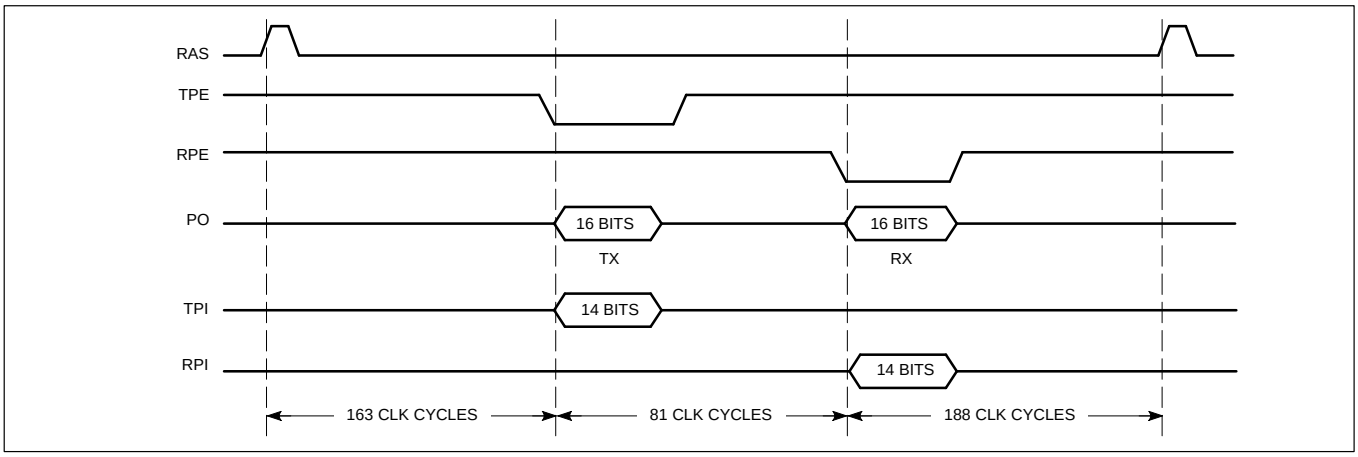

Figure 6. PCM Timing

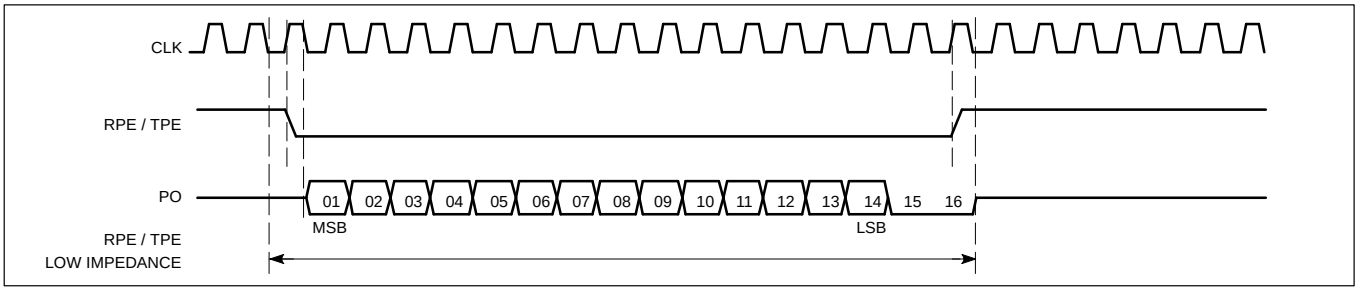

Figure 7. PCM Output Timing

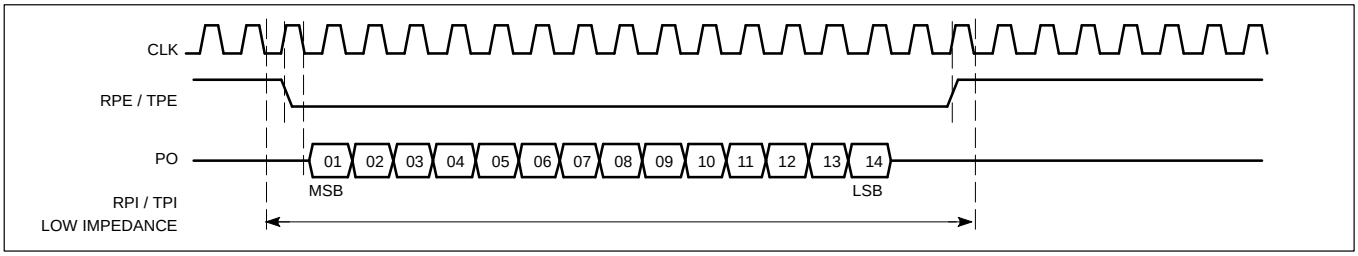

Figure 8. PCM Input Timing

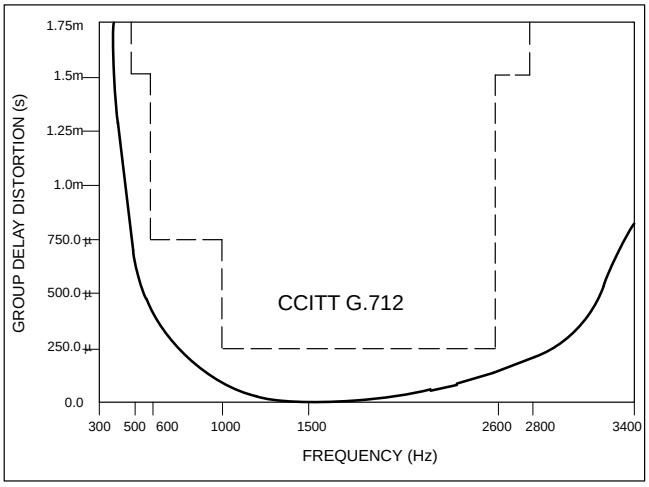

Figure 9. Group Delay Distortion Transmit + Receive (Loop Measurement)

APPLICATION INFORMATION

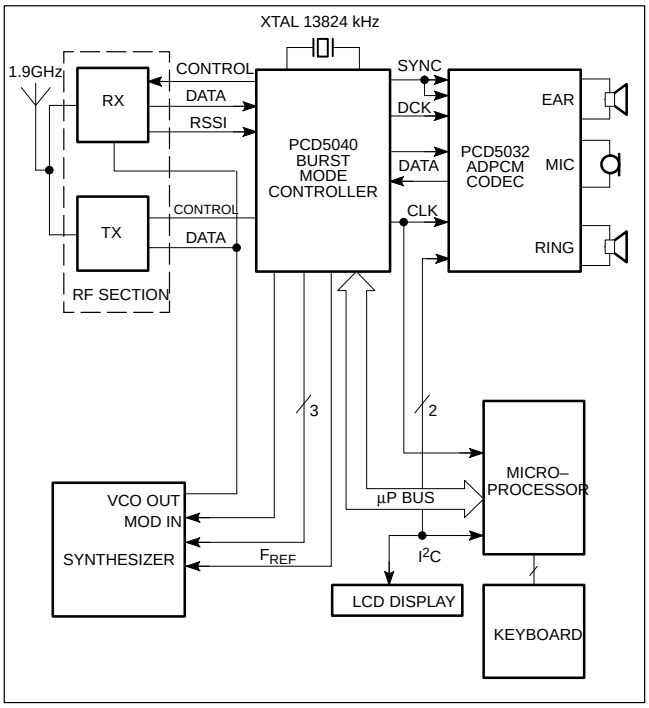

Figure 10. Typical Block Diagram for a DECT Handset

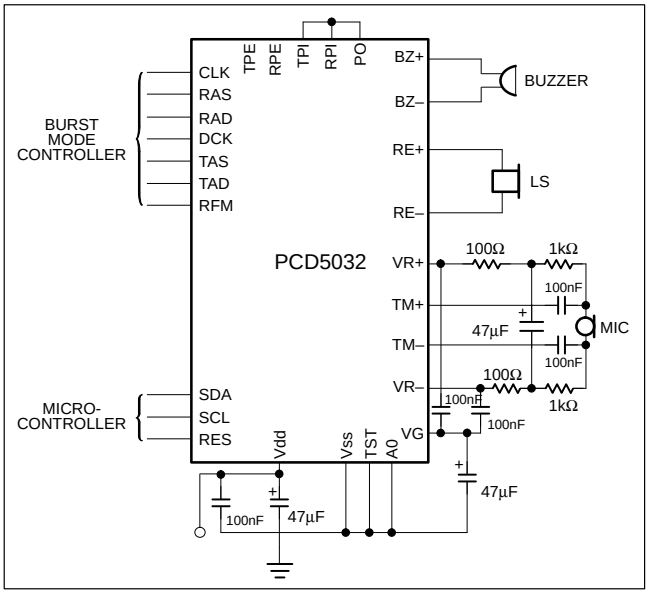

Figure 11. Typical Handset Application Diagram for the PCD5032

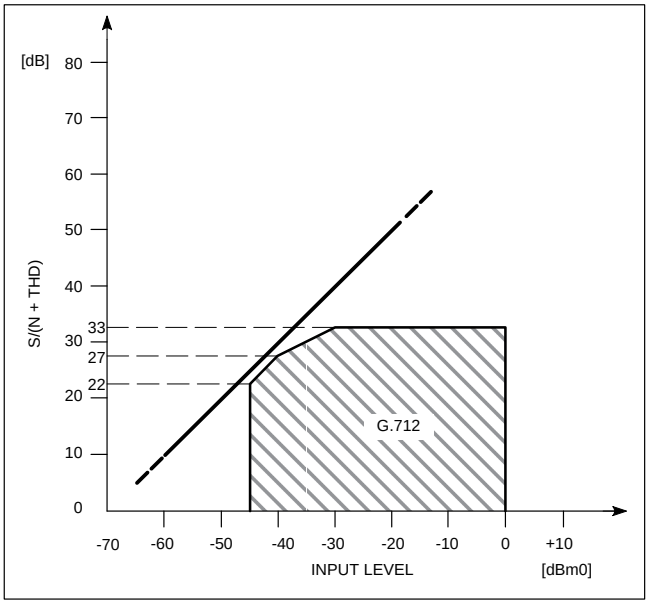

Figure 12. Typical Performance of AD and DA in Cascade (Loop 1)