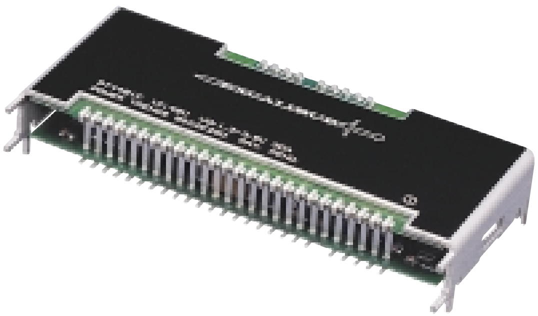


Features

- Dual 15-A Outputs *(Independantly Regulated)*
- Power-up/Down Sequencing
- Input Voltage Range: 36 V to 75 V
- 1500 VDC Isolation
- Temp Range: –40 to 100 °C
- High Efficiency: 88 %
- Fixed Frequency Operation
- Over-Current Protection *(Both Outputs)*
- Dual Logic On/Off Control
- Over-Temperature Shutdown
- Over-Voltage Protection *(Coordinated Shutdown)*
- Under-Voltage Lockout
- Input Differential EMI Filter
- IPC Lead Free 2
- Safety Approvals:
  UL1950
  CSA 22.2 950

Description

The PT4660 Excalibur™ Series is a 30-A rated, dual-output isolated DC/DC converter that combines state-of-the-art power conversion technology with unparalleled flexibility. These modules operate from a standard telecom (–48 V) central office (CO) supply to produce two independantly regulated outputs.

The PT4660 series is characterized with high efficiencies and ultra-fast transient response, and incorporates many features to facilitate system integration. These include a flexible “On/Off” enable control, output current limit, over-temperature protection, and an input under-voltage lockout (UVLO). In addition, both output voltages are designed to meet the power-up/power-down sequencing requirements of popular DSPs.

The PT4660 series is housed in space-saving solderable copper case. The package does not require a heatsink and is available in both vertical and horizontal configurations, including surface mount. The ‘N’ configuration occupies less than 2 in² of PCB area.

Ordering Information

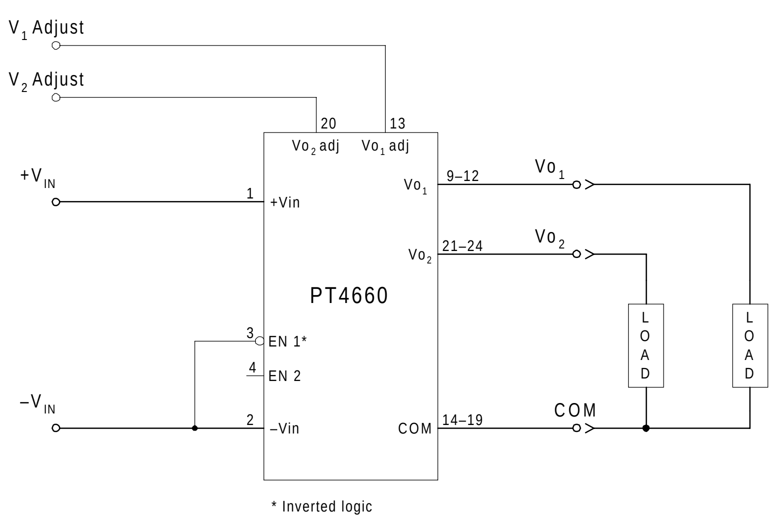
Pt. No.	Vo1/Vo2
PT4661❑	= 5.0/3.3 Volts
PT4662❑	= 3.3/2.5 Volts
PT4663❑	= 3.3/1.8 Volts
PT4665❑	= 3.3/1.5 Volts
PT4666❑	= 2.5/1.8 Volts
PT4667❑	= 5.0/1.8 Volts
PT4668❑	= 3.3/1.2 Volts

PT Series Suffix (PT1234 x)

Case/Pin Configuration	Order Suffix	Package Code
Vertical	N	(EKD)
Horizontal	A	(EKA)
SMD	C	(EKC)

(Reference the applicable package code drawing for the dimensions and PC board layout)

Typical Application



* Inverted logic

Pin-Out Information

Pin	Function	Pin	Function	Pin	Function
1	$+V_{in}$	10	$+Vo_1$	19	COM
2	$-V_{in}$	11	$+Vo_1$	20	Vo_2 Adjust
3	EN 1	12	$+Vo_1$	21	$+Vo_2$
4	EN 2	13	Vo_1 Adjust	22	$+Vo_2$
5	TEMP	14	COM	23	$+Vo_2$
6	AUX	15	COM	24	$+Vo_2$
7	Do Not Connect	16	COM	25	Do Not Connect
8	Do Not Connect	17	COM	26	Do Not Connect
9	$+Vo_1$	18	COM		

Note: *Shaded functions indicate signals that are referenced to the input (-Vin) potential.*

On/Off Logic

Pin 3	Pin 4	Output Status
1	×	Off
0	1	On
×	0	Off

Notes:
Logic 1 =Open collector
Logic 0 = –Vin (pin 2) potential

For positive Enable function, connect pin 3 to pin 2 and use pin 4.

For negative Enable function, leave pin 4 open and use pin 3.

Pin Descriptions

+Vin: The positive input supply for the module with respect to $-V_{in}$. When powering the module from a –48 V telecom central office supply, this input is connected to the primary system ground.

–Vin: The negative input supply for the module, and the 0 VDC reference for the *EN 1*, *EN 2*, *TEMP*, and *AUX* signals. When the module is powered from a +48-V supply, this input is connected to the 48-V Return.

EN 1: This an open-collector (open-drain) negative logic input that enables the module output. This pin is TTL compatible and referenced to $-V_{in}$. A logic '0' at this pin enables the module's outputs, and a logic '1' or high impedance disables the module's outputs. If not used, the pin must be connected to $-V_{in}$.

EN 2: An open-collector (open-drain) positive logic input that enables the module output. This pin is TTL compatible and referenced to $-V_{in}$. A logic '1' or high impedance enables the module's outputs. If not used, the pin should be left open circuit.

AUX: Produces a regulated output voltage of 11.6 V ±5 %, which is referenced to $-V_{in}$. The current drawn from the pin must be limited to 10mA. The voltage may be used to indicate the output status of the module to a primary referenced circuit, or power a low-current amplifer.

TEMP: This is the output voltage produced by the module's internal temperature sensor. The voltage at this pin is referenced to $-V_{in}$ and rises approximately 10 mV/°C from an intital value of 0.1 VDC at –40 °C.

$$V_{temp} = 0.5 + 0.01 \cdot T_{sense}$$

The signal is available whenever the module is supplied with a valid input voltage, and is independant of the enable logic status. (**Note:** *A load impedance of less than 1 MΩ will adversly affect the module's over-temperature shutdown threshold. Use a high-impedance input when monitoring this signal.)*

Vo_1: The higher regulated output voltage, which is referenced to the *COM* node.

Vo_2: The lower regulated output voltage, which is referenced to the *COM* node.

COM: The secondary return reference for the module's two regulated output voltages. It is dc isolated from the input supply pins.

Vo_1 Adjust: Using a single resistor, this pin allows Vo_1 to be adjusted higher or lower than the preset value. If not used, this pin should be left open circuit.

Vo_2 Adjust: Using a single resistor, this pin allows Vo_2 to be adjusted higher or lower than the preset value. If not used, this pin should be left open circuit.

Specifications (Unless otherwise stated, T_a =25 °C, V_{in} =48 V, & Io_1=Io_2=10 A)

Characteristics	Symbols	Conditions	PT4660 SERIES Min	Typ	Max	Units
Output Current	Io_1, Io_2	Vo_1 — Vo_1 ≤3.3 V Vo_1 =5.0 V	0 0	— —	15 10	A
		Vo_2 — All voltages	0	—	15	A
	Io_1+Io_2	Total (both outputs) — Vo_1 ≤3.3 V Vo_1 =5.0 V	0 0	— —	30 25	A
Input Voltage Range	V_{in}		36	48	75	V
Set Point Voltage Tolerance	$V_o$tol		—	±1	±2	%V_o
Temperature Variation	ΔReg_{temp}	–40 to +100 °C Case, Io_1 =Io_2 =0 A	—	±0.5	—	%V_o
Line Regulation	ΔReg_{line}	Over V_{in} range with Io_1=Io_2=5 A	—	±5	±10	mV
Load Regulation	ΔReg_{load}	1 A ≤Io_1 ≤Io_1max, Io_2 =1 A — ΔVo_1 1 A ≤Io_2 ≤Io_1max, Io_1 =1 A — ΔVo_2	— —	±2 ±2	±10 ±10	mV
Cross Regulation	ΔReg_{cross}	1 A ≤Io_2 ≤Io_1max, Io_1 =1 A — ΔVo_1 1 A ≤Io_1 ≤Io_1max, Io_2 =1 A — ΔVo_2	— —	±2 ±2	±10 ±5	mV
Total Output Variation	ΔV_otol	Includes set-point, line load, –40 °C to +100 °C case — ΔVo_1 ΔVo_2	— —	±2 ±2	±3 ±3	%V_o
Efficiency	η	PT4661 PT4662 PT4663 PT4665 PT4666 PT4667 PT4668	— — — — — — —	88 87 86 86 85 88 86	— — — — — — —	%
V_o Ripple (pk-pk)	V_r	Io_1=Io_2=5 A, 20 MHz bandwidth — V_o =5 V V_o <5 V	— —	— —	75 50	mV_{pp}
Transient Response	t_{tr}	1 A/µs load step from 50 % to 100 % $I_o$max (either output)	— —	25 6.0	100 —	µSec %V_o
Current Limit	I_{LIM}	Each output with other unloaded	15.5	18	—	A
Output Rise Time	t_{on}	At turn-on to within 90 % of V_o	—	5	10	mSec
Output Over-Voltage Protection	OVP	Either output; shutdown and latch off	—	125 (1)	—	%V_o
Output Voltage Adjustment	ΔV_oadj	Vo_1, Vo_2	—	±10	—	%V_o
Switching Frequency	f_s		270	—	330	kHz
Under-Voltage-Lockout	UVLO	Rising Falling	— 30	34 32	36 —	V
Internal Input Capacitance	C_{in}		—	2	—	µF
Enable Control Inputs Input High Voltage Input Low Voltage	 V_{IH} V_{IL}	Referenced to $-V_{in}$	 3.5 0	 — —	 — 0.8 (2)	V
Input Low Current	I_{IL}		—	0.5	—	mA
Standby Current	I_{in} standby	Pins 2, 3, & 4 connected	—	3	5	mA
External Output Capacitance	C_{out}	Per each output	0	—	5,000	µF
Primary/Secondary Isolation	V_{iso} C_{iso} R_{iso}		1500 — 10	— 1500 —	— — —	V pF MΩ
Temperature Sense	V_{temp}	Output voltage at temperatures:- — –40 °C 100 °C	— —	0.1 (3) 1.5 (3)	— —	V
Operating Temperature Range	T_a	Over V_{in} range	–40	—	85 (4)	°C
Over-Temperature Protection	OTP	Case temperature (auto restart)	100	—	—	°C
Solder Reflow Temperature	T_{reflow}	Surface temperature of module pins or case	—	—	215 (5)	°C
Storage Temperature	T_s	—	–40	—	125	°C
Mechanical Shock	—	Per Mil-STD-883D, Method 2002.3	—	500	—	G's
Mechanical Vibration	—	Per Mil-STD-883D, Method 2007.2, 20–2,000 Hz — Suffix N Suffixes A, C	— —	10 (6) 20 (6)	— —	G's
Weight	—	—	—	90	—	grams
Flammability	—	Materials meet UL 94V-0				

Notes: (1) *This is a fixed parameter. Adjusting Vo_1 or Vo_2 higher will increase the module's sensitivity to over-voltage detection. For more information, see the application note on output voltage adjustment.*

(2) *The EN_1 and EN_2 control inputs (pins 3 & 4) have internal pull-ups and may be controlled with an open-collector (or open-drain) transistor. Both inputs are diode protected and can be connected to $+V_{in}$. The maximum open-circuit voltage is 5.4 V.*

(3) *Voltage output at "TEMP" pin is defined by the equation:- $V_{TEMP} = 0.5 + 0.01 \cdot T$, where T is in °C. See pin descriptions for more information.*

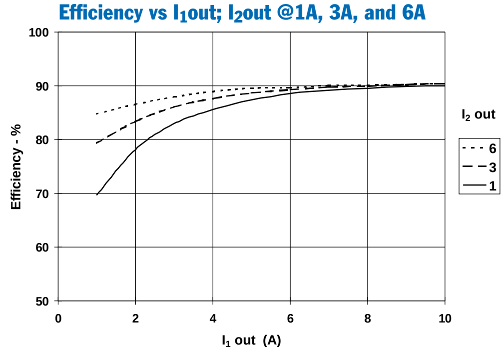
(4) *See SOA curves or consult the factory for the appropriate derating.*

(5) *During solder reflow of SMD package version do not elevate the module case, pins, or internal component temperatures above a peak of 215 °C. For further guidance refer to the application note, "Reflow Soldering Requirements for Plug-in Power Surface Mount Products," (SLTA051).*

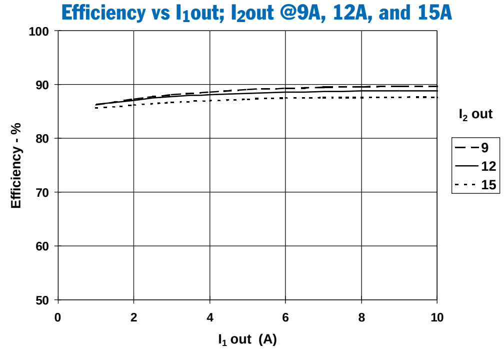
(6) *The case pins on the through-holed package types (suffixes N & A) must be soldered. For more information see the applicable package outline drawing.*

PT4661 (V_1/V_2 =5.0V/3.3V); V_{in} =48V (See Notes A & B)

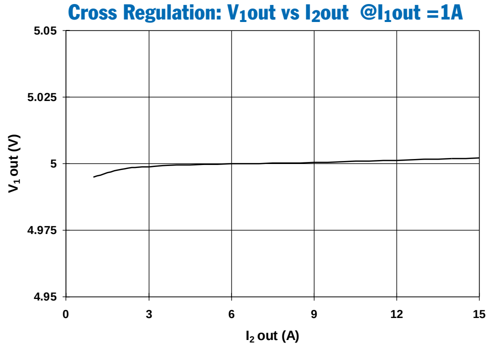
Efficiency vs I_1out; I_2out @1A, 3A, and 6A



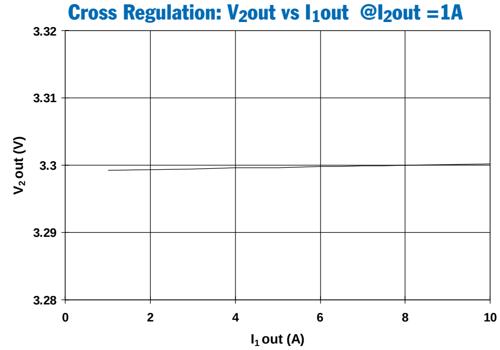
Efficiency vs I_1out; I_2out @9A, 12A, and 15A



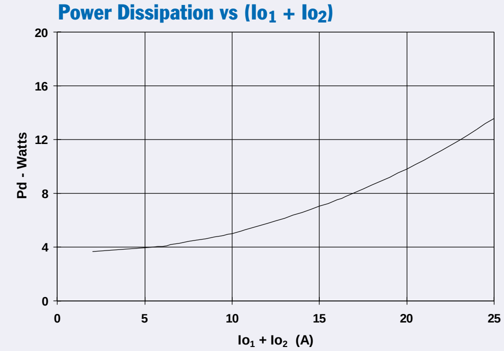
Cross Regulation: V_1out vs I_2out @I_1out =1A



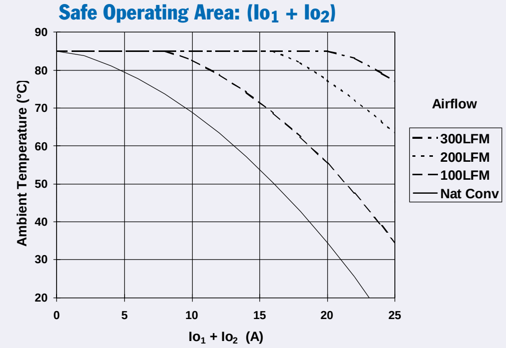
Cross Regulation: V_2out vs I_1out @I_2out =1A



Power Dissipation vs (Io_1 + Io_2)



Safe Operating Area: (Io_1 + Io_2)



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the converter.*
Note B: *SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.*

Typical Characteristics

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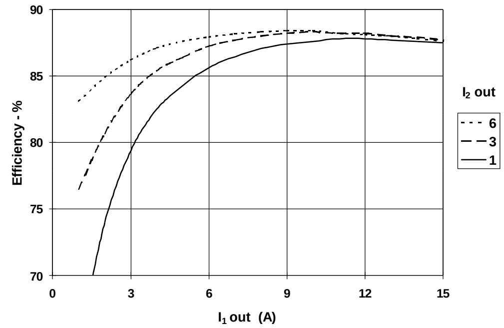
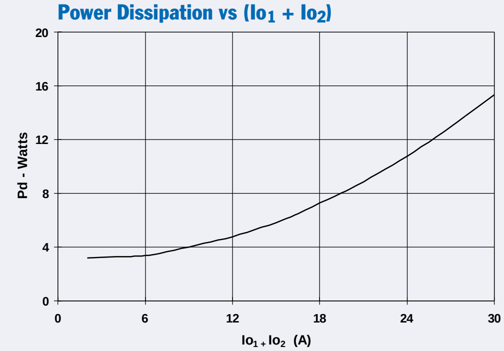
PT4662 (V_1/V_2 =3.3 V/2.5 V); V_{in} =48 V (See Notes A & B)

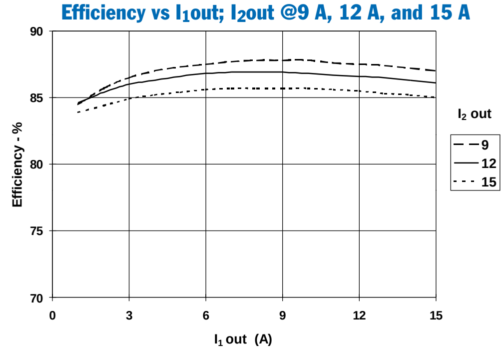
Efficiency vs I_1out; I_2out @1 A, 3 A, and 6 A



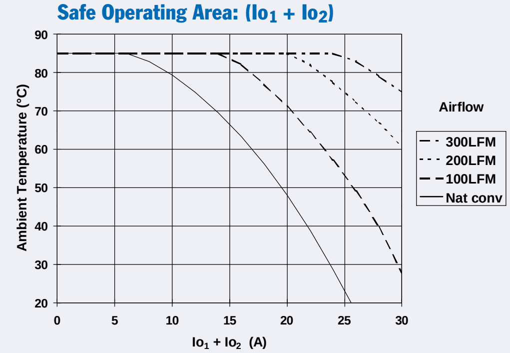
Power Dissipation vs (Io_1 + Io_2)



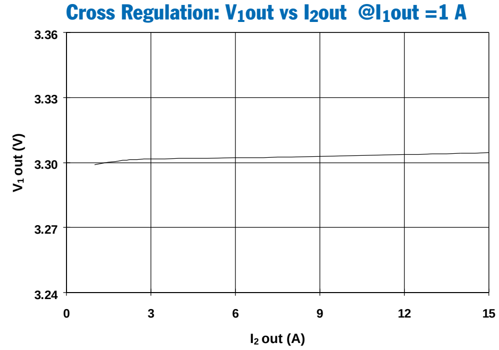
Efficiency vs I_1out; I_2out @9 A, 12 A, and 15 A



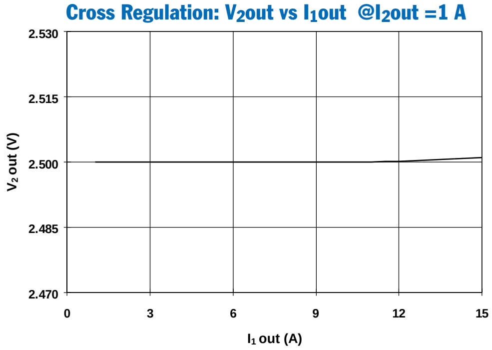
Safe Operating Area: (Io_1 + Io_2)



Cross Regulation: V_1out vs I_2out @I_1out =1 A

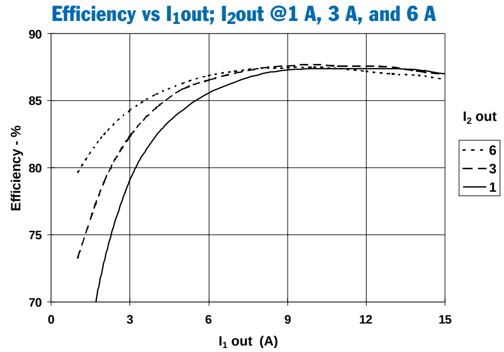


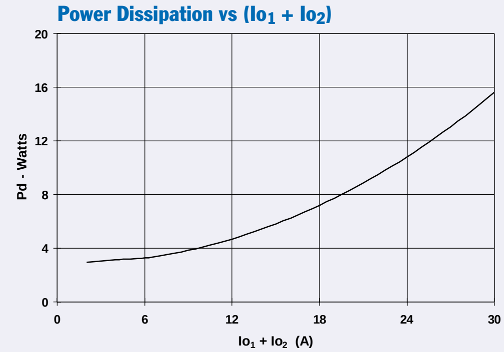
Cross Regulation: V_2out vs I_1out @I_2out =1 A

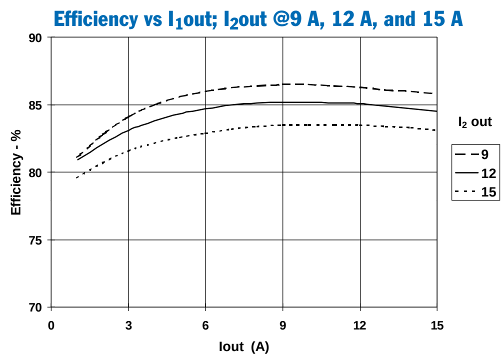


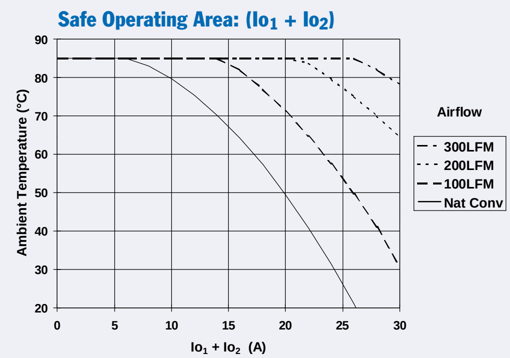
Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25 °C. This data is considered typical data for the converter.*
Note B: *SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.*

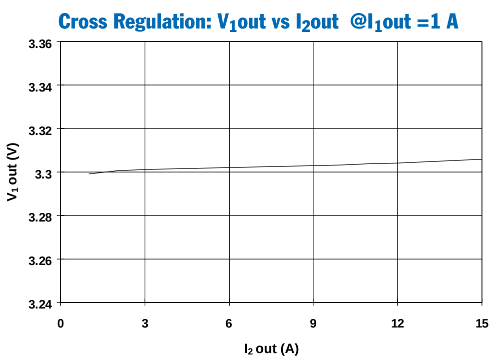
PT4663 (V_1/V_2 =3.3 V/1.8 V); V_{in} =48 V (See Notes A & B)

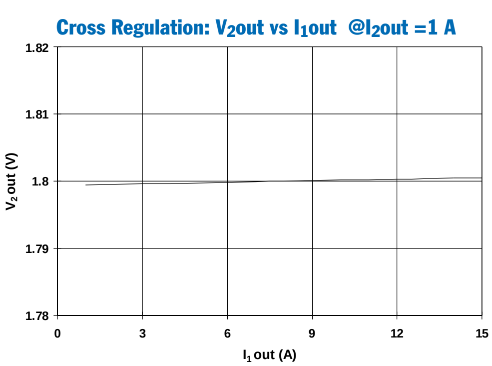








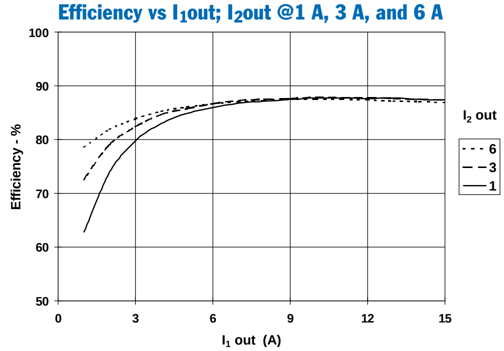




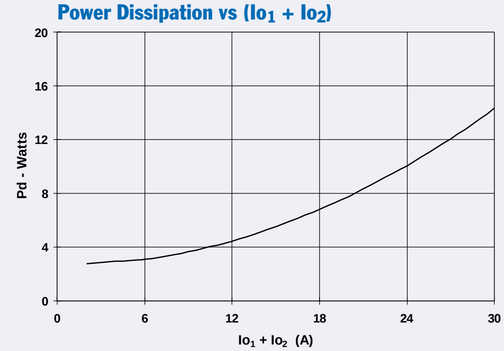
Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25 °C. This data is considered typical data for the converter.*
Note B: *SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.*

PT4665 (V_1/V_2 =3.3 V/1.5 V); V_{in} =48 V (See Notes A & B)

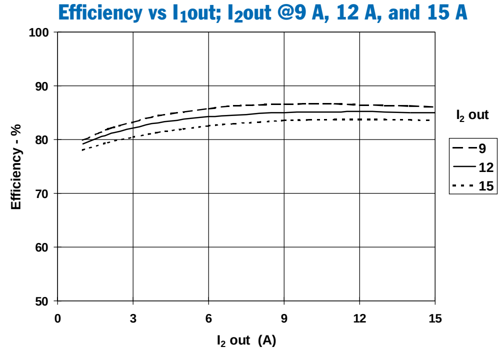
Efficiency vs I_1out; I_2out @1 A, 3 A, and 6 A



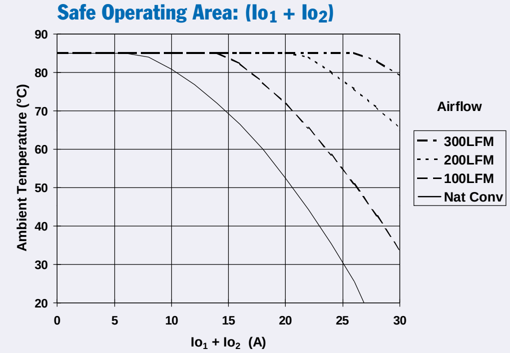
Power Dissipation vs (Io_1 + Io_2)



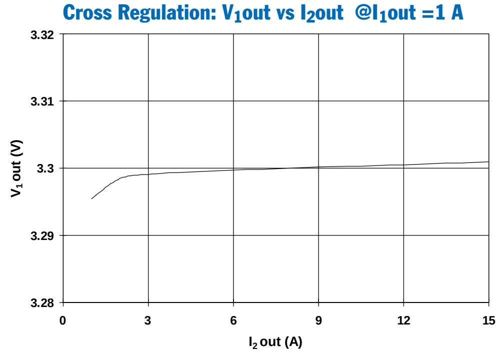
Efficiency vs I_1out; I_2out @9 A, 12 A, and 15 A



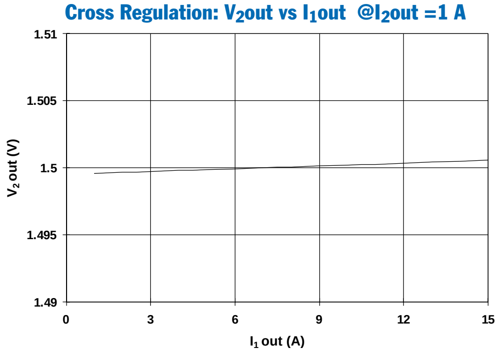
Safe Operating Area: (Io_1 + Io_2)



Cross Regulation: V_1out vs I_2out @I_1out =1 A



Cross Regulation: V_2out vs I_1out @I_2out =1 A

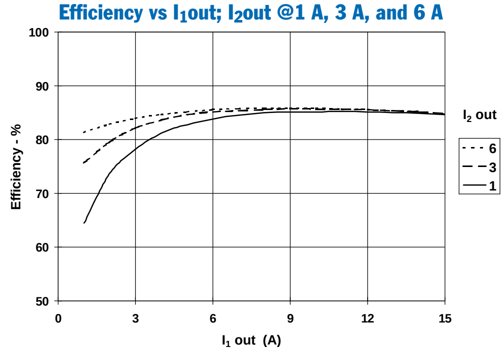


Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25 °C. This data is considered typical data for the converter.*
Note B: *SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.*

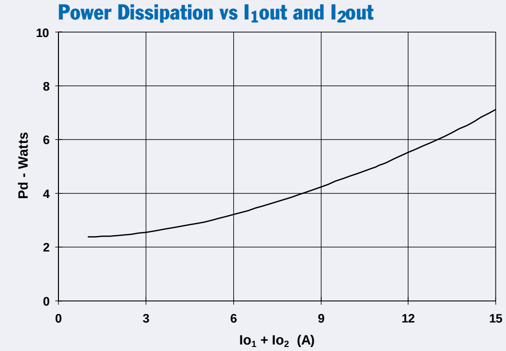
Typical Characteristics

PT4666 (V_1/V_2 =2.5 V/1.8 V); V_{in} =48 V (See Notes A & B)

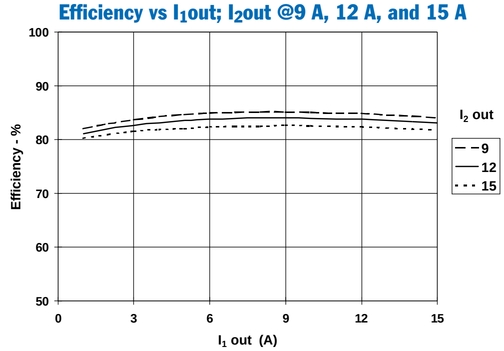
Efficiency vs I_1out; I_2out @1 A, 3 A, and 6 A



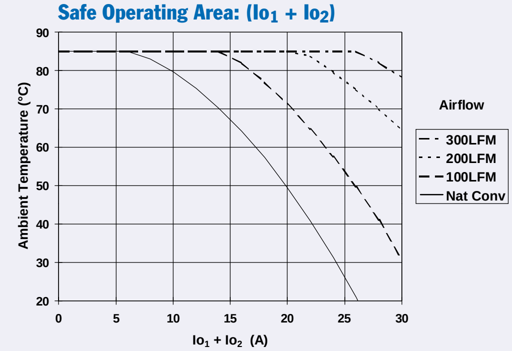
Power Dissipation vs I_1out and I_2out



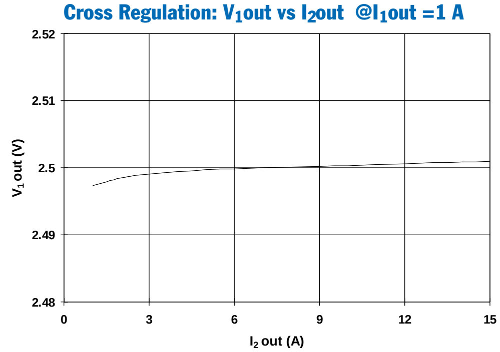
Efficiency vs I_1out; I_2out @9 A, 12 A, and 15 A



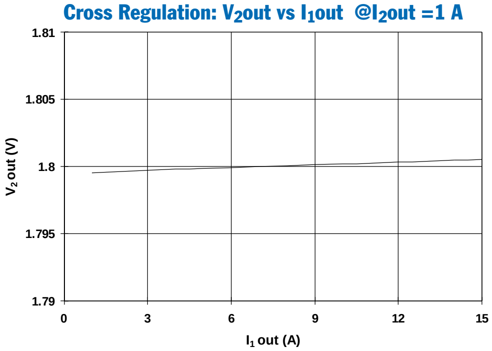
Safe Operating Area: (Io_1 + Io_2)



Cross Regulation: V_1out vs I_2out @I_1out =1 A



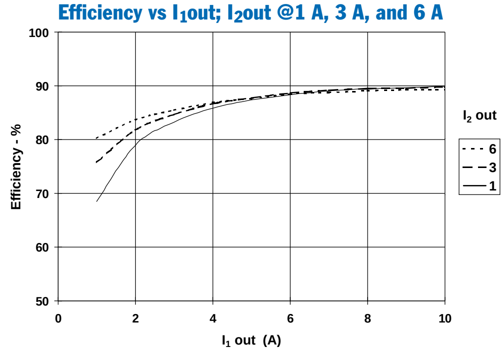
Cross Regulation: V_2out vs I_1out @I_2out =1 A



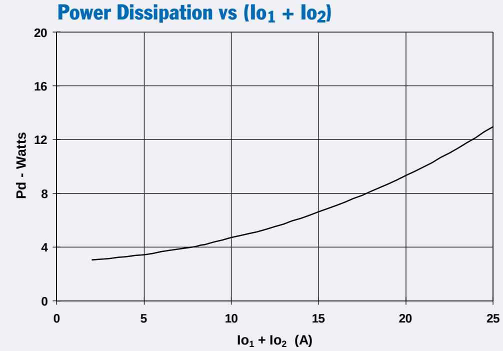
Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25 °C. This data is considered typical data for the converter.*
Note B: *SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.*

PT4667 (V_1/V_2 =5 V/1.8 V); V_{in} =48 V (See Notes A & B)

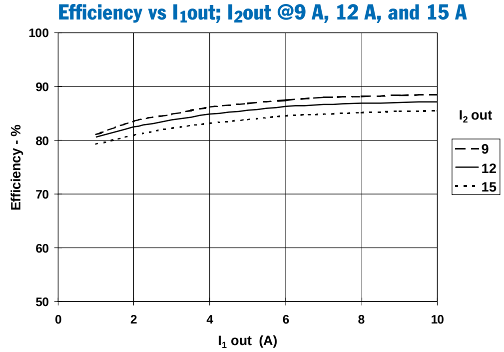
Efficiency vs I_1out; I_2out @1 A, 3 A, and 6 A



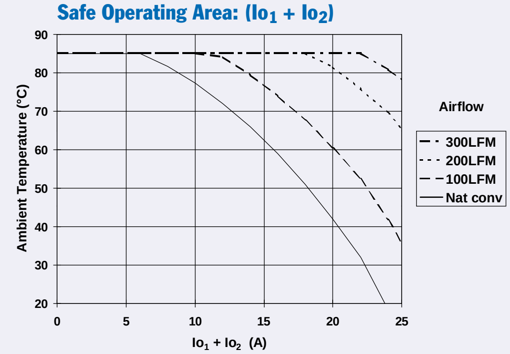
Power Dissipation vs (Io_1 + Io_2)



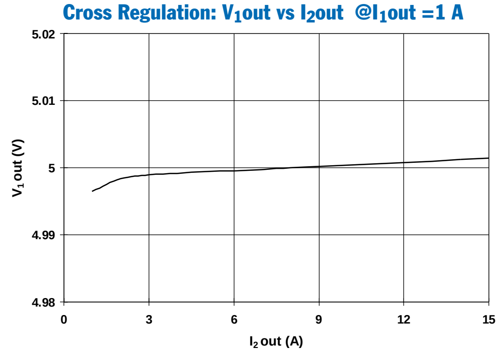
Efficiency vs I_1out; I_2out @9 A, 12 A, and 15 A



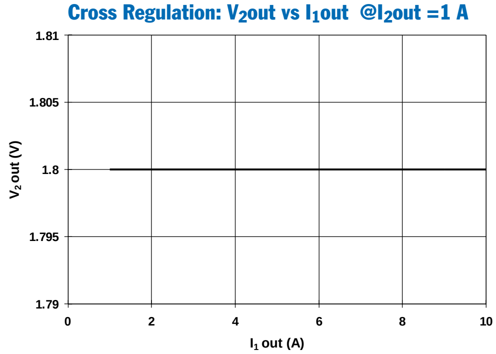
Safe Operating Area: (Io_1 + Io_2)



Cross Regulation: V_1out vs I_2out @I_1out =1 A



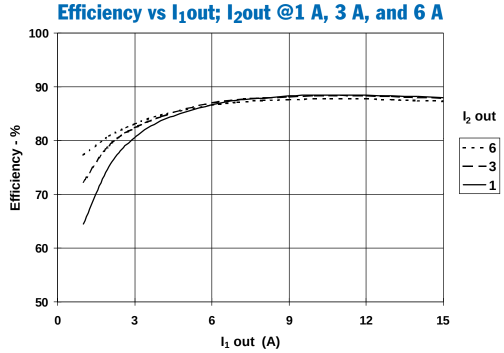
Cross Regulation: V_2out vs I_1out @I_2out =1 A



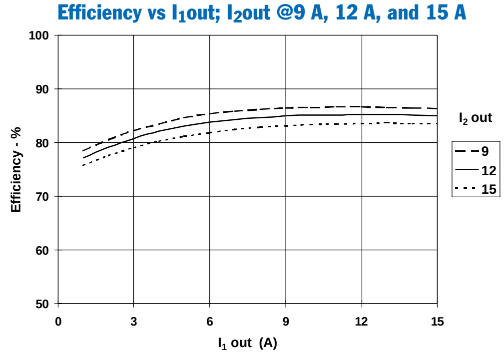
Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25 °C. This data is considered typical data for the converter.*
Note B: *SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.*

PT4668 (V_1/V_2 =3.3 V/1.2 V); V_{in} =48 V (See Notes A & B)

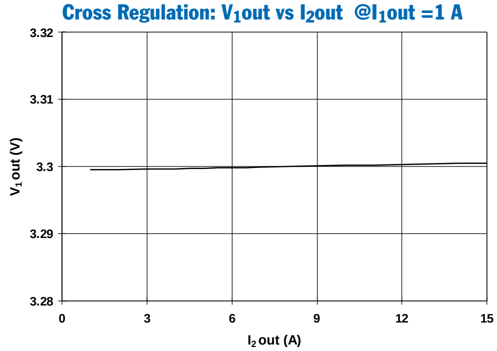
Efficiency vs I_1out; I_2out @1 A, 3 A, and 6 A



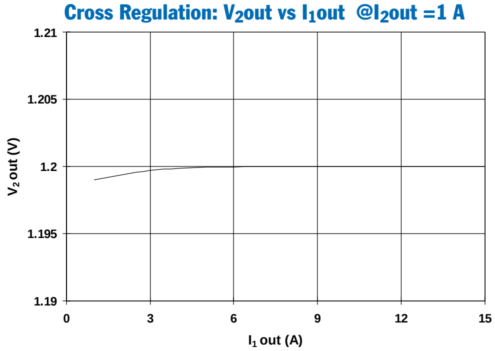
Efficiency vs I_1out; I_2out @9 A, 12 A, and 15 A



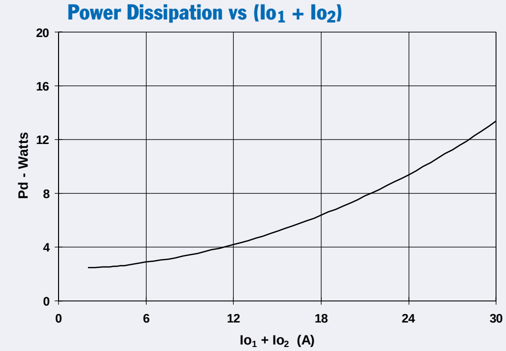
Cross Regulation: V_1out vs I_2out @I_1out =1 A



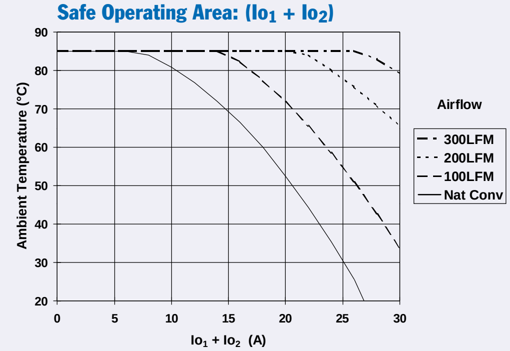
Cross Regulation: V_2out vs I_1out @I_2out =1 A



Power Dissipation vs (Io_1 + Io_2)



Safe Operating Area: (Io_1 + Io_2)



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25 °C. This data is considered typical data for the converter.*
Note B: *SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.*

Operating Features & System Considerations for the PT4660 & PT4680 Dual-Output Converters

Over-Current Protection

The dual-outputs of the PT4660 and PT4680 series of DC/DC converters have independent output voltage regulation and current limit control. Applying a load current in excess of the current limit threshold at either output will cause the respective output voltage to drop. However, the voltage at Vo_2 is derived from Vo_1. Therefore a current limit fault on Vo_1 will also cause Vo_2 to drop. Conversely, a current limit fault applied to Vo_2 will only cause Vo_2 voltage to drop, and Vo_1 will remain in regulation.

The current limit is continuous with some current foldback. This means that at short circuit, the value of the output current can be less than the rated output of the converter. This is to reduce power dissipation when a fault is present. As with any foldback-limited source, if a constant current load is applied to the converter with a value greater than the short-circuit current, the output voltage will not come up. Resistive and non-linear load circuits are not affected by this characteristic as long as the current at startup does not exceed the short-circuit current of the converter. The majority of low-voltage analog and digital applications are not affected by this restriction. However, when testing with an electronic load the constant resistance setting should be used.

Output Over-Voltage Protection

Each output is monitored for over voltage (OV). For fail safe operation and redundancy, the OV fault detection circuitry uses a separate reference to the voltage regulation circuits. The OV threshold is fixed, and set nominally 25 % higher than the set-point output voltage. If either output exceeds the threshold, the converter is shutdown and must be actively reset. The OV protection circuit can be reset by momentarily turning the converter off. This is accomplished by either cycling one of the output enable control pins (*EN1* or *EN2*), or by removing the input power to the converter. Note: *If Vo_1 or Vo_2 is adjusted to a higher voltage, the margin between the respective steady-state output voltage and its OV threshold is reduced. This can make the module sensitive to OV fault detection, that may result from random noise and load transients.*

Over-Temperature Protection

The converter has an internal temperature sensor. At a case temperature of approximately 115 °C the converter will shut down, and will automatically restart when the temperature returns to about 100 °C. The analog voltage generated by the sensor is also made available at the *TEMP* output (pin 5), and can be monitored by the host system for diagnostic purposes. Consult the 'Pin Descriptions' section of the data sheet for further information on this feature.

Under-Voltage Lock-Out

The Under-Voltage Lock-Out (UVLO) circuit prevents operation of the converter whenever the input voltage to the module is insufficient to maintain output regulation. The UVLO has approximately 2 V of hysterisis. This is to prevent oscillation with a slowly changing input voltage. Below the UVLO threshold the module is off and the enable control inputs, *EN1* and *EN2* are inoperative.

Primary-Secondary Isolation

The PT4460 and PT4680 series of DC/DC converters incorporate electrical isolation between the input terminals (primary) and the output terminals (secondary). All converters are production tested to a withstand voltage of 1500 VDC. The isolation complies with UL60950 and EN60950, and the requirements for operational isolation. This allows the converter to be configured for either a positive or negative input voltage source.

The regulation control circuitry for these modules is located on the secondary (output) side of the isolation barrier. Control signals are passed between the primary and secondary sides of the converter via a proprietory magnetic coupling scheme. This eliminates the use of opto-couplers. The data sheet 'Pin Descriptions' and 'Pin-Out Information' provides guidance as to which reference (primary or secondary) that must be used for each of the external control signals.

Fuse Requirements

To comply with safety agency requirements, these converters **must** be operated with an external input fuse. A fast-acting 250-V fuse is required. Table 1-1 gives the recommended current rating for the product series being used.

Table 1-1; Recommended Fuse Rating

Product Series	Input Bus	Total Iout	Fuse Rating
PT4660	48 V	30 A	7 A
PT4680	24 V	20 A	10 A

Using the On/Off Enable Controls on the PT4660 & PT4680 Series of Dual-Output Converters

The PT4660 (48V input) and PT4680 (24V input) series of dual-output DC/DC converters incorporate both positive and negative logic output enable controls. *EN1* (pin 3) is the negative enable input, and *EN2* (pin 4) is the positive enable input. Both inputs are TTL logic compatible, and are electrically referenced to $-V_{in}$ (pin 2) on the primary (input) side of the converter. A pull-up resistor is not required, but may be added if desired. Adding a pull-up resistor from either *EN1* or *EN2*, up to $+V_{in}$, will not damage the converter.

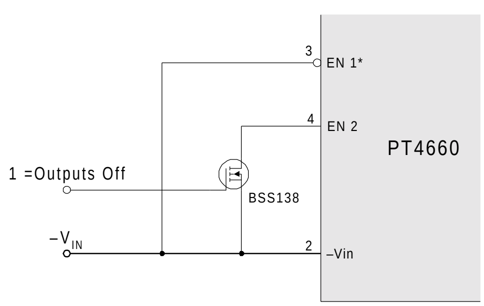
Automatic (UVLO) Power-Up

Connecting *EN1* (pin 3) to $-V_{in}$ (pin 2) and leaving *EN2* (pin 4) open-circuit configures the converter for automatic power up. (See data sheet "Typical Application"). The converter control circuitry incorporates an "Under Voltage Lockout" (UVLO) function, which disables the output until the minimum specified input voltage is present (See data sheet Specifications). The UVLO circuitry ensures a clean transition during power-up and power-down, allowing the converter to tolerate a slow-rising input voltage. For most applications *EN1* and *EN2*, can be configured for automatic power-up.

Positive Output Enable (Negative Inhibit)

To configure the converter for a positive enable function, connect *EN1* (pin 3) to $-V_{in}$ (pin 2), and apply the system On/Off control signal to *EN2* (pin 4). In this configuration, a logic '0' ($-V_{in}$ potential) applied to pin 4 disables the converter outputs. An example of this configuration is detailed in Figure 2-1.

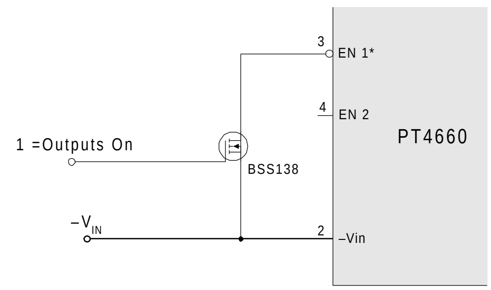
Figure 2-1; Positive Enable Configuration



Negative Output Enable (Positive Inhibit)

To configure the converter for a negative enable function, *EN2* (pin 4) is left open circuit, and the system On/Off control signal is applied to *EN1* (pin 3). A logic '0' ($-V_{in}$ potential) must then be applied to pin 3 in order to enable the outputs of the converter. An example of this configuration is detailed in Figure 2-2. *<u>Note</u>: The converter will only produce and output voltage if a valid input voltage is applied to* $\pm V_{in}$.

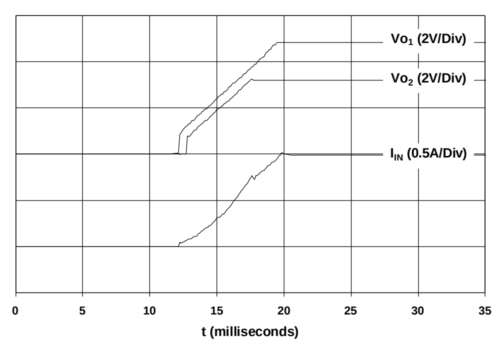
Figure 2-2; Negative Enable Configuration



On/Off Output Voltage Sequencing

The output voltages from these dual-output DC/DC converters are independantly regulated, and are internally sequenced to meet the power-up requirements of popular microprocessor and DSP chipsets. Figure 2-3 shows the waveforms from a PT4661 after the converter is enabled at t=0s. During power-up, the Vo_1 and Vo_2 voltage waveforms typically track within 0.4V prior to Vo_2 reaching regulation. The waveforms were measured with a 5-Adc resistive load at each output, and with a 48-VDC input source applied. The converter typically produces a fully regulated output within 25ms. The actual turn-on time will vary slightly with input voltage, but the power-up sequence is independent of the load at either output.

Figure 2-3; Vo_1, Vo_2 Power-Up Sequence



During turn-off, both outputs drop rapidly due to the discharging effect of actively switched rectifiers. The voltage at Vo_1 remains higher than Vo_2 during this period. The discharge time is typically 100µs, but will vary with the amount of external load capacitance.

Adjusting the Output Voltage of the PT4660 & PT4680 Series of Dual-Output Converters

The dual output voltages from the PT4660 (48-V Bus), and PT4680 (24-V Bus) series of DC/DC converters can be independently adjusted by up to 10 %, higher or lower than the factory trimmed pre-set voltage. The adjustment method requires the addition of a single external resistor [1]. Table 3-1 gives the adjustment range of Vo_1 and Vo_2 for each model in the series as V_a(min) and V_a(max).

Vo_1 Adjust Down: Add a resistor (R_1), between pin 13 (*Vo_1 Adj*) and pin 12 (*Vo_1*) [2].

Vo_1 Adjust Up: To increase the output, add a resistor R_2 between pin 13 (*Vo_1 Adj*) and pin 14 (*COM*) [2, 4].

Vo_2 Adjust Down: Add a resistor (R_3) between pin 20 (*Vo_2 Adj*) and pin 21 (*Vo_2*) [2].

Vo_2 Adjust Up: Add a resistor R_4 between pin 20 (*Vo_2 Adj*) and pin 19 (*COM*) [2, 4].

Refer to Figure 3-1 and Table 3-2 for both the placement and value of the required resistor.

Notes:

1. Adjust resistors are not required if Vo_1 and Vo_2 are to remain at their respective nominal set-point voltage. In this case, *Vo_1 Adj* (pin 13) and *Vo_2 Adj* (pin 20) are left open-circuit
2. Use only a single 1% resistor in either the (R_1) or R_2 location to adjust Vo_1, and in the (R_3) or R_4 location to adjust Vo_2. Place the resistor as close to the converter as possible.
3. Vo_2 must always be at least 0.3 V lower than Vo_1.
4. **<u>The over-voltage protection</u>** threshold is fixed, and is set nominally 25 % above the set-point output voltage. Adjusting Vo_1 or Vo_2 higher will reduce the voltage margin between the respective steady-state output voltage and its over-voltage (OV) protection threshold. This could make the module sensitive to OV fault detection, as a result of random noise and load transients.
   <u>Note</u>: An OV fault is a latched condition that shuts down both outputs of the converter. The fault can only be cleared by cycling one of the Enable control pins (EN_1 / EN_2), or by momentarily removing the input power to the module.*
5. Never connect capacitors to either the *Vo_1 Adj* or *Vo_2 Adj* pins. Any capacitance added to these control pins will affect the stability of the respective regulated output.

The adjust up and adjust down resistor values can also be calculated using the following formulas. Be sure to select the correct formula parameter from Table 3-1 for the output and model being adjusted.

$$(R_1) \text{ or } (R_3) = R_o \cdot \frac{(V_a - V_r)}{(V_o - V_a)} - R_s \quad k\Omega$$

$$R_2 \text{ or } R_4 = R_o \cdot \frac{V_r}{V_a - V_o} - R_s \quad k\Omega$$

Where:
- V_o = Original output voltage, (*Vo_1* or *Vo_2*)
- V_a = Adjusted output voltage
- V_r = The reference voltage from Table 3-1
- R_o = The resistance constant in Table 3-1
- R_s = The series resistance from Table 3-1

Figure 3-1; Placement of Output Adjust Resistors

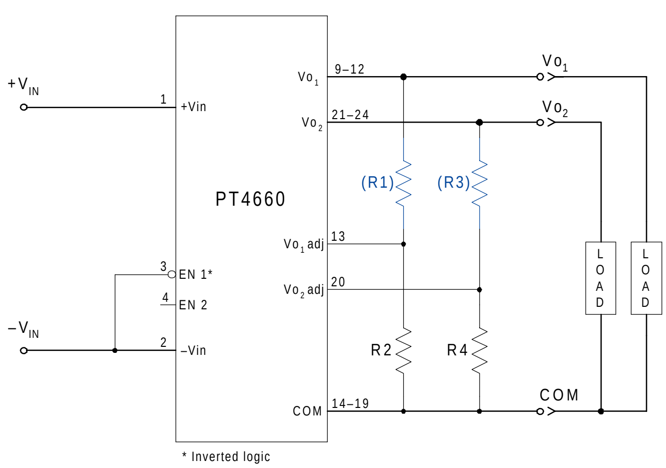


Table 3-1; ADJUSTMENT RANGE AND FORMULA PARAMETERS

Vo_1 Bus				Vo_2 Bus (2)					
24 V Bus Pt.#	**PT4681/7**	**PT4682/3/5/8**	**PT4686**	**PT4681**	**PT4682**	**PT4683/7**	**PT4686**	**PT4685**	
48 V Bus Pt.#	**PT4661/7**	**PT4662/3/5/8**	**PT4666**	**PT4661**	**PT4662**	**PT4663/7**	**PT4666**	**PT4665**	**PT4668**
Adj. Resistor	**(R1)/R2**	**(R1)/R2**	**(R1)/R2**	**(R3)/R4**	**(R3)/R4**	**(R3)/R4**	**(R3)/R4**	**(R3)/R4**	**(R3)/R4**
V_o(nom)	5.0 V	3.3 V	2.5 V	3.3 V	2.5 V	1.8 V	1.8 V	1.5 V	1.2 V
Va(min)	4.5 V	2.97 V	2.25 V	2.97 V	2.25 V	1.62 V	1.62 V	1.35 V	1.08 V
Va(max)	5.5 V	3.63 V	2.75 V	3.63 V	2.75 V	1.98 V	1.98 V	1.65 V	1.32 V
Vr	2.5 V	1.65 V	1.25	1.65 V	1.25 V	0.9 V	0.9 V	0.75 V	0.6V
R_o (kΩ)	4.99	4.99	4.99	1.21	1.21	1.21	1.21	1.21	1.21
R_s (kΩ)	20.0	20.0	20.0	4.99	4.99	4.99	3.32	4.99	3.32

Table 3-2a; ADJUSTMENT RESISTOR VALUES, Vo_1

24 V Bus Pt.#	**PT4681/7**		**PT4682/3/5**		**PT4686**
48 V Bus Pt.#	**PT4661/7**		**PT4662/3/5/8**		**PT4666**
Adj. Resistor	**(R1)/R2**		**(R1)/R2**		**(R1)/R2**
V_o(nom)	5.0 V		3.3 V		2.5 V
V_a(req'd)		**V_a(req'd)**		**V_a(req'd)**	
5.5	5.0 kΩ	3.6	7.4 kΩ	2.75	5.0 kΩ
5.4	11.2 kΩ	3.54	14.3 kΩ	2.7	11.2 kΩ
5.3	21.6 kΩ	3.48	25.7 kΩ	2.65	21.6 kΩ
5.2	42.4 kΩ	3.42	48.6 kΩ	2.6	42.4 kΩ
5.1	105.0 kΩ	3.36	117.0 kΩ	2.55	105.0 kΩ
5.0		3.3		2.5	
4.9	(99.8) kΩ	3.24	(112.0 kΩ)	2.45	(99.8 kΩ)
4.8	(37.4) kΩ	3.18	(43.6 kΩ)	2.4	(37.4 kΩ)
4.7	(16.6) kΩ	3.12	(20.8 kΩ)	2.35	(16.6 kΩ)
4.6	(6.2) kΩ	3.06	(9.3 kΩ)	2.3	(6.2 kΩ)
4.5	(0.0)	3.0	(2.5 kΩ)	2.25	(0.0 kΩ)

R_1 = (Blue), R_2 = Black

Table 3-2b; ADJUSTMENT RESISTOR VALUES, Vo_2

24 V Bus Pt.#	**PT4681**	**PT4682**		**PT4683/6/7**	**PT4686**	**PT4685**	
48 V Bus Pt.#	**PT4661**	**PT4662**		**PT4663/6/7**	**PT4666**	**PT4665**	**PT4668**
Adj. Resistor	**(R3)/R4**	**(R3)/R4**		**(R3)/R4**	**(R3)/R4**	**(R3)/R4**	**(R3)/R4**
V_o(nom)	3.3 V	2.5 V		1.8 V	1.8 V	1.5 V	1.2 V
V_a(req'd)			**V_a(req'd)**				
3.6	1.7 kΩ		1.95	2.3 kΩ	3.9 kΩ		
3.54	3.3 kΩ		1.9	5.9 kΩ	7.6 kΩ		
3.48	6.1 kΩ		1.85	16.8 kΩ	18.5 kΩ		
3.42	11.6 kΩ		1.8				
3.36	28.3 kΩ		1.75	(15.6) kΩ	(17.3) kΩ		
3.3			1.7	(4.7) kΩ	(6.4) kΩ		
3.24	(27.1) kΩ		1.65	(1.1) kΩ	(2.7) kΩ	1.1 kΩ	
3.18	(10.4) kΩ		1.6			4.1 kΩ	
3.12	(4.9) kΩ		1.55			13.2 kΩ	
3.06	(2.1) kΩ		1.5				
3.0	(0.5) kΩ		1.45			(12.0) kΩ	
2.75		1.1 kΩ	1.4			(2.9) kΩ	
2.7		2.6 kΩ	1.35			(0.0) kΩ	
2.65		5.1 kΩ	1.3				3.9 kΩ
2.6		10.1 kΩ	1.275				6.4 kΩ
2.55		25.3 kΩ	1.25				11.2 kΩ
2.5			1.225				25.7 kΩ
2.45		(24.1) kΩ	1.2				
2.4		(8.9) kΩ	1.175				(24.5) kΩ
2.35		(3.9) kΩ	1.15				(10.0) kΩ
2.3		(1.4) kΩ	1.125				(5.2) kΩ
2.25		(0.0)kΩ	1.1				(2.7) kΩ

R_3 = (Blue), R_4 = Black

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
PT4661C	LIFEBUY	SIP MODULE	EKC	26	6	TBD	Call TI	Level-3-215C-168HRS	
PT4661N	LIFEBUY	SIP MODULE	EKD	26	6	TBD	Call TI	Level-1-215C-UNLIM	
PT4662C	LIFEBUY	SIP MODULE	EKC	26	6	TBD	Call TI	Level-3-215C-168HRS	
PT4663A	LIFEBUY	SIP MODULE	EKA	26	6	TBD	Call TI	Level-1-215C-UNLIM	

(1) The marketing status values are defined as follows:
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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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