S-24H30R/I

8-word×8-bit Serial NON-VOLATILE RAM

The S-24H30R/I is a non-volatile CMOS RAM, composed of a CMOS static RAM and a non-volatile electrically erasable programmable memory (E^2PROM) to backup the SRAM. The organization is 8-word × 8-bit (total 64 bits) and data can be transferred serially by a data bus.
Data is stored from SRAM to E^2PROM by the store signal or an instruction from a CPU, and is recalled from E^2PROM to SRAM by the recall signal or instruction from a CPU. The SRAM data can be read or written separately from non-volatile data stored in the E^2PROM.

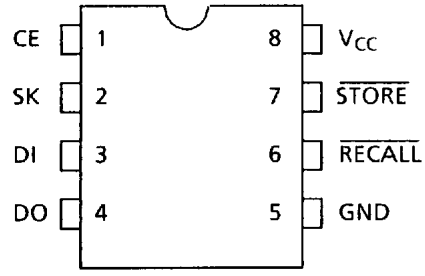
■ Features

- Ideal as a peripheral for microcomputers
  - Static timing
  - Minimum input/output interface
  - Compatible with serial port as Intel 8051
- Non-volatile functions can be controlled by software or hardware
- Erroneous store protection
- All inputs and outputs are compatible with TTL
- High drive output
- +5-V single power supply (+5 V ± 10%)
- Low current consumption
  - Operating : 5 mA typ.
  - Store : 5 mA typ.
  - Standby : 1 μA max.
  - Sleep : 1 μA max.
- Compact 8 pin DIP/SOP
- E^2PROM store cycles: 10^4 or 10^5 times
- E^2PROM data retention: 10 years

■ Pin Arrangement

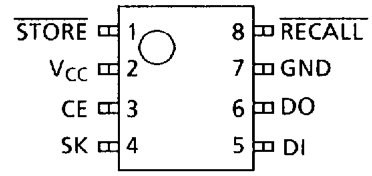
8-pin DIP

Top view



8-pin SOP

Top view



CE	Chip enable
SK	Serial clock
DI	Serial data input
DO	Serial data output
$\overline{\text{RECALL}}$	Recall
$\overline{\text{STORE}}$	Store
V_{CC}	Power supply voltage (+ 5 V)
GND	Ground (0 V)

Figure 1

■ Block Diagram

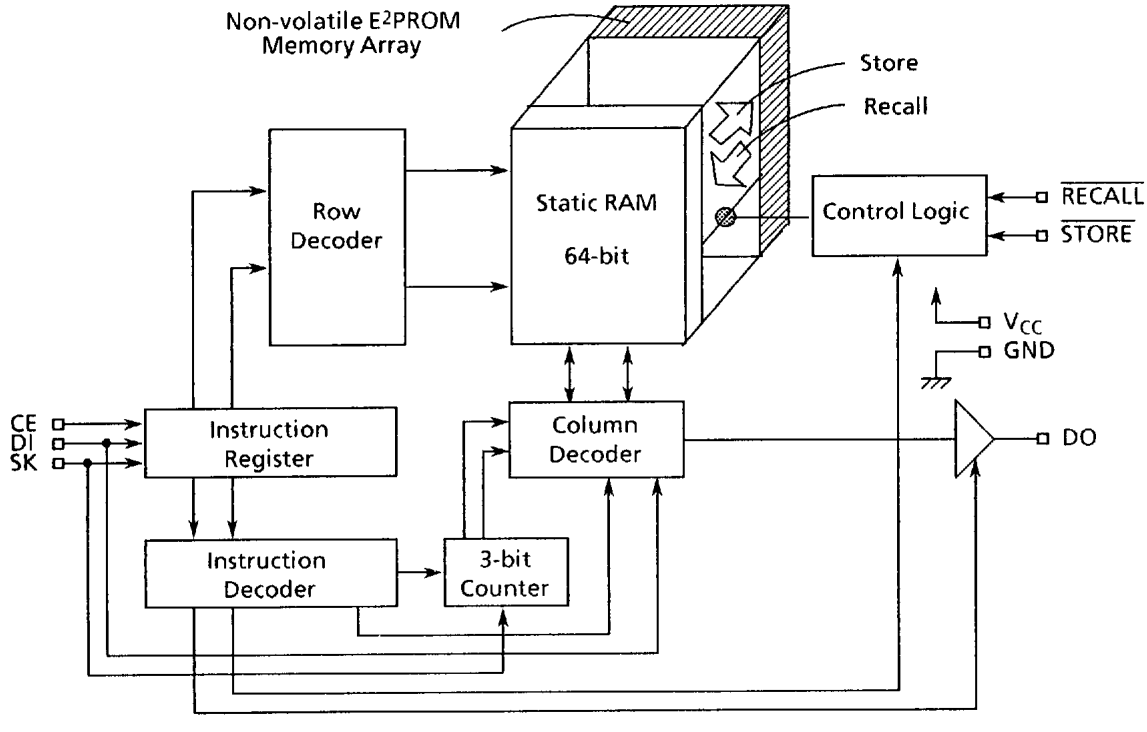


Figure 2

■ Absolute Maximum Ratings

Table 1

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	T_{stg}	S-24H30R	-65 to + 125	°C
		S-24H30I	-65 to + 150	°C
Storage temperature under bias	T_{bias}	S-24H30R	-10 to + 85	°C
		S-24H30I	-50 to + 95	°C
Power supply voltage	V_{CC}		-0.3 to + 6.0	V
Input voltage	V_{IN}		-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}		0.0 to V_{CC}	V

■ Recommended Operating Conditions

Table 2

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}	CE, SK, DI, $\overline{\text{STORE}}$, $\overline{\text{RECALL}}$	2.0	—	V_{CC}	V
Low level input voltage	V_{IL}	CE, SK, DI, $\overline{\text{STORE}}$, $\overline{\text{RECALL}}$	0.0	—	0.8	V
Operating temperature	T_{opr}	S-24H30R	0	—	+ 70	°C
		S-24H30I	- 40	—	+ 85	°C

■ DC Electrical Characteristics

Table 3

S-24H30R: Ta = 0°C to +70°C, V_{CC} = +5V ± 10%
S-24H30I : Ta = -40°C to +85°C, V_{CC} = +5V ± 10%

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating current consumption	I_{CC}	DO unloaded	—	5	10	mA
Sleep current	I_{SL}	All inputs are GND or V_{CC}	—	—	1	μA
Standby current	I_{SB}	CE = GND, Other inputs are GND or V_{CC}	—	—	1	μA
Store current	I_{STO}		—	5	10	mA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	—	0.1	1	μA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	—	0.1	1	μA
Low level output voltage	V_{OL}	CMOS : I_{OL} = 100 μA	—	—	0.1	V
		TTL : I_{OL} = 4.2mA	—	—	0.4	V
High level output voltage	V_{OH}	CMOS : I_{OH} = -100 μA	V_{CC}-0.1	—	—	V
		TTL : I_{OH} = -2 mA	2.4	—	—	V
Store inhibition voltage	V_{WI}		—	3.5	4.2	V

■ Data Hold Characteristics

Table 4

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data hold voltage	V_{DH}	CE ≦ 0.2V, $\overline{RECALL}$ ≧ V_{CC}-0.2V	1.5	—	5.5	V
Data hold setup time	t_{CDH}		50	—	—	ns
Recovery time	t_R		300	—	—	ns

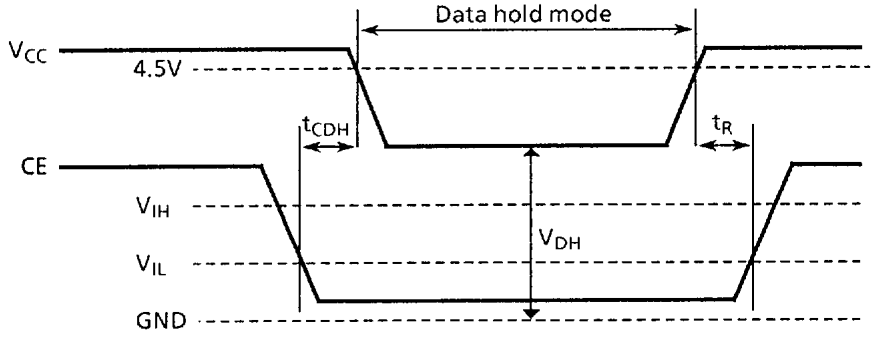


Figure 3 Data hold timing chart

■ Capacitance

Table 5

(Ta = 25°C, f = 1.0 MHz, V_{CC} = 5 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V	—	—	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V	—	—	8	pF

■ AC Electrical Characteristics

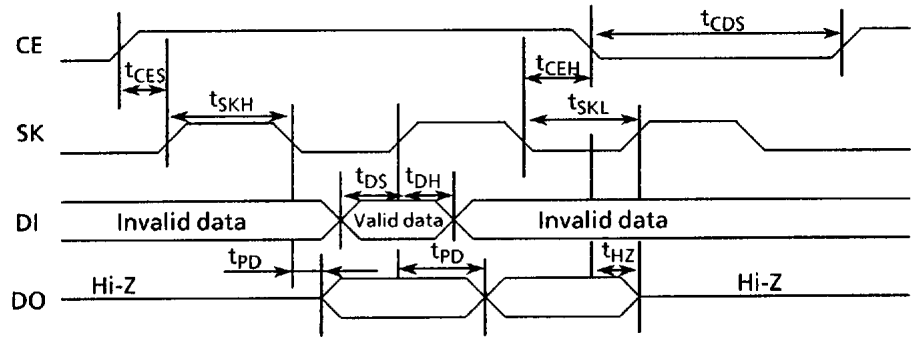
Table 6 Measurement conditions

Item	S-24H30R	S-24H30I	Unit
Input pulse voltage	0.65 to 2.2	0.0 to 3.0	V
Input pulse rise/fall time	10	10	ns
I/O reference voltage	1.5	1.5	V
Output load	1TTL + 100pF	1TTL + 100pF	

1. Data input/output timing

Table 7

Item	Symbol	Min.	Typ.	Max.	Unit
SK frequency	f_{SK}	—	—	1	MHz
SK high level pulse width	t_{SKH}	0.4	—	—	μs
SK low level pulse width	t_{SKL}	0.4	—	—	μs
Input data setup time	t_{DS}	0.4	—	—	μs
Input data hold time	t_{DH}	0.08	—	—	μs
SK data valid time	t_{PD}	—	—	0.3	μs
Output disable time	t_{HZ}	—	—	1.0	μs
CE setup time	t_{CES}	0.8	—	—	μs
CE hold time	t_{CEH}	0.4	—	—	μs
CE deselect time	t_{CDS}	0.8	—	—	μs



- CE must be kept high during instructions.
- When SK rises after selecting CE, the first 1 is taken into DI input and the fetch of an instruction starts. All previous 0 is ignored.

Figure 4 Control data timing

2. Recall Cycle

Table 8

Item	Symbol	Min.	Typ.	Max.	Unit
Recall cycle time	t_{RCC}	2500	—	—	ns
Recall pulse width	t_{RCP}	500	—	—	ns
Recall disable time	t_{RCZ}	—	—	500	ns
Recall enable time	t_{ORC}	10	—	—	ns
Recall data access time	t_{ARC}	—	—	1000	ns

Recall times are not limited.

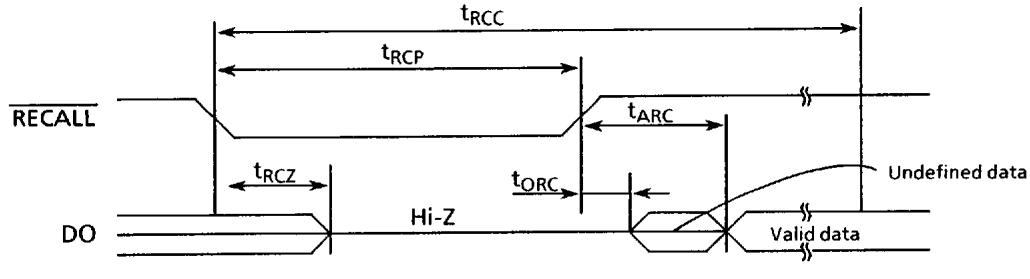


Figure 5 Hardware recall

3. Store Cycle

Table 9

Item	Symbol	Min.	Typ.	Max.	Unit
Store time	t_{ST}	—	—	10	ms
Store pulse width	t_{STP}	0.2	—	—	μs
Store disable time	t_{STZ}	—	—	1.0	μs

Store times: $10^4/10^5$
Data retention : 10 years

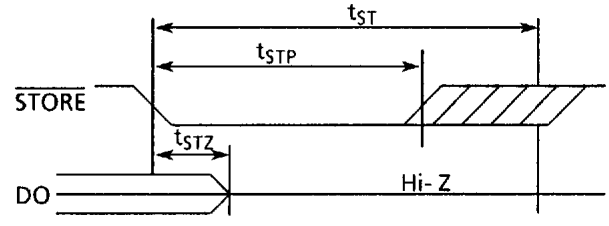


Figure 6 Hardware store

■ Instruction Set

Table 10

Instruction	Symbol	Format $I_2 I_1 I_0$	Function
Write enable latch reset	WRDS	1XXXX000	Reset write enable latch (Disable write and store)
Write enable latch set	WREN	1XXXX100	Set write enable latch (Enable write and store)
Read	READ	1AAAX11X	Read data from RAM address AAA
Write	WRITE	1AAAX011	Write data into RAM address AAA
Store	STO	1XXXX001	Store RAM data in E^2PROM
Recall	RCL	1XXXX101	Recall E^2PROM data into RAM
Sleep	SLEEP	1XXXX010	Enter sleep mode

X : Don't care
A : Address bit

■ Operation

1. Internal latches

The S-24H30R/I has two latches, one of which controls write operation of the SRAM, and both of which control permission/inhibition of store operation of the E²PROM.

1.1 Previous recall latch

The previous recall latch controls permission/inhibition of store operation of E²PROM. It is reset when the power is turned on, and it inhibits store operation of the E²PROM. It is set by executing the software recall instruction or hardware recall, and it permits store operation of the E²PROM.

1.2 Write enable latch

The write enable latch controls permission/inhibition of both store operation of the E²PROM and write operation of the SRAM. It is reset when the power is turned on or by executing WRDS instruction, and it inhibits both store operation of the E²PROM and write operation of the SRAM.

It is set by executing WREN instruction, and it permits both store operation of the E²PROM and write operation of the SRAM.

When store operation of the E²PROM is completed, the write enable latch is automatically reset. Therefore, in order to execute store operation again, it is necessary to execute WREN instruction and to set the write enable latch.

1.3 Both the previous recall latch and the write enable latch must be set for permission of store operation.

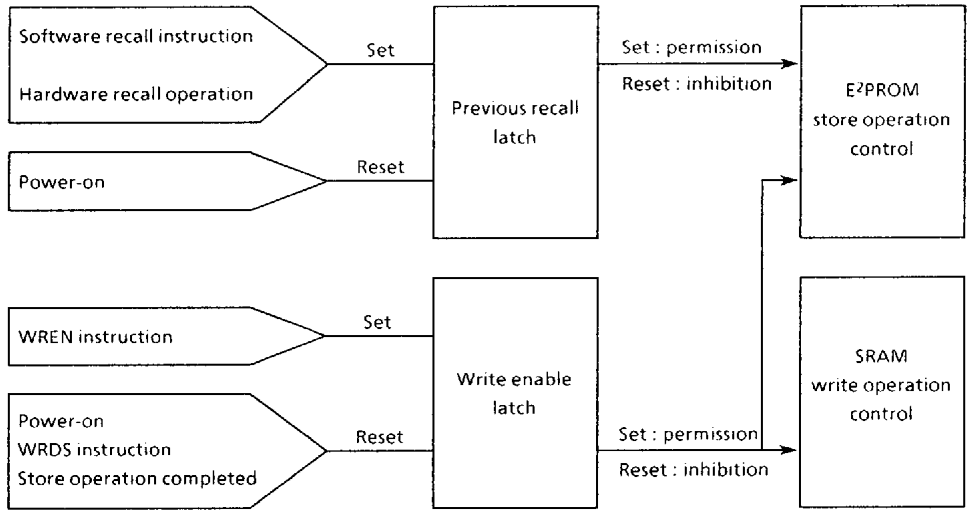


Figure 7 Internal latch

2. SRAM mode

2.1 Read

The data is read from the SRAM with READ instruction. Inputting a start bit, 3-bit address and 4-bit instruction code causes 8-bit data output on DO. In S-24H30R/I, a bi-directional serial interface can be made by connecting DI and DO. See Figure 8 for the timing.

2.2 Write

The data is written into the SRAM with WRITE instruction. 8-bit data is input on DI following a start bit, 3-bit address and 4-bit instruction code. See Figure 9 for the timing. The write enable latch must be set before WRITE instruction.

3. E^2PROM mode

Data is input to and output from the E^2PROM through the SRAM.

3.1 Store

The SRAM data is copied into the E^2PROM when STO instruction is executed or $\overline{\text{STORE}}$ goes low. The SRAM data does not change after STO instruction. Since the data stored in the E^2PROM is non-volatile, it is retained even if power is turned off. In the case that store operation is performed while data is output on DO and during read operation of the SRAM, DO becomes high-impedance. During store operation, all other operations are inhibited.

Both the previous recall latch and the write enable latch must be set for store operation.

3.2 Recall

The E^2PROM data is recopied into the SRAM when $\overline{\text{RECALL}}$ goes low or RCL instruction is executed. In the case that recall operation is performed while data is output on DO and during read operation of SRAM, DO becomes high-impedance. During recall operation, all other operations are inhibited.

4. Sleep mode

Executing SLEEP instruction disables operation of the SRAM. The E^2PROM data is retained. The sleep mode can be exited by recall operation.

Since the S-24H30R/I is in standby status and the current consumption is low when CE is at GND level, it is not necessary to set to sleep mode in order to reduce the current consumption during non-operation.

5. Operation timing

After CE rose, when SK clock rises and DI becomes high, a start bit is recognized and the fetch of an instruction starts. Data is fetched to DI terminal at the rise of SK clock.

5.1 Read

D0 is output at the fall of the 8th clock, and others are output at the rise of the clock.

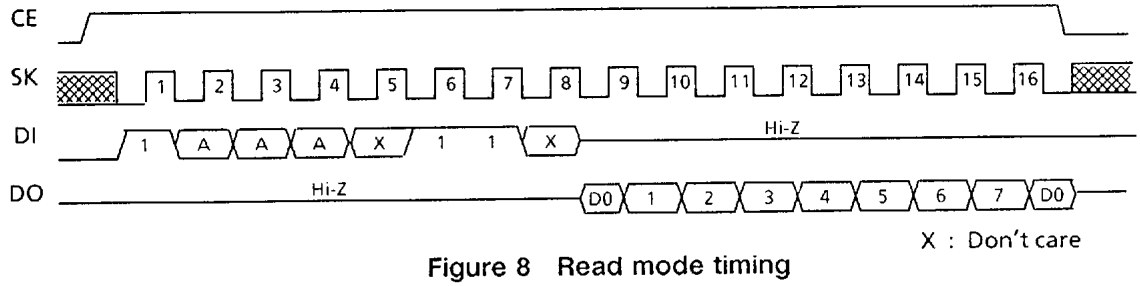


Figure 8 Read mode timing

5.2 Write

Data is written to the SRAM at the rise of the SK clock.

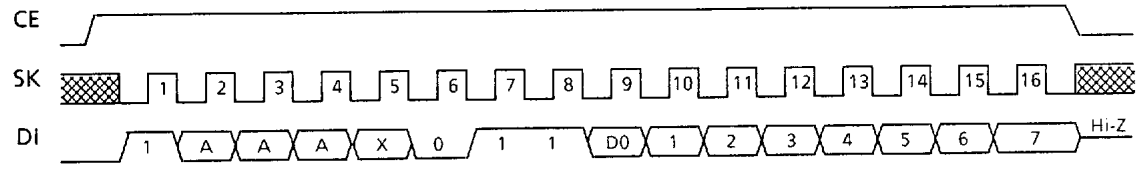


Figure 9 Write mode timing

5.3 Other operation modes

CE must be low between instructions.

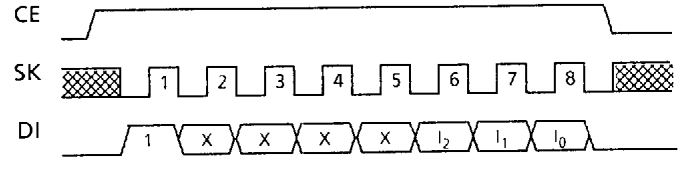


Figure 10 Other operation mode

■ Interface with CPU with Serial Port

- When SK and DI are high at the rise of CE, high of DI is regarded as a start bit and the clock 1 generates and the high of DI is fetched. When DI is low, DI is regarded as a start bit after DI becomes high at the rise of SK.
- After power on or after instruction is performed, DI must be set 1 for preparing the fetch of the start bit of a next instruction.

Figures 11 to 13 show the timings of write/read, and other operation modes, and interfacing examples are shown on the next page.

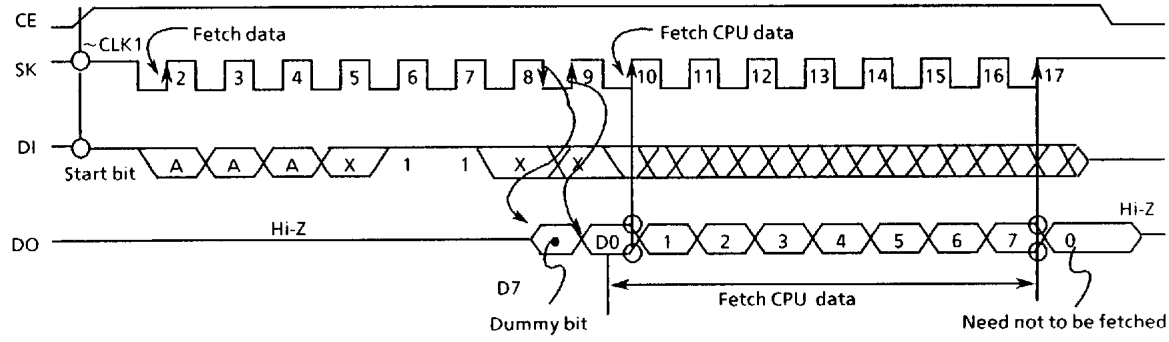


Figure 11 Read mode timing

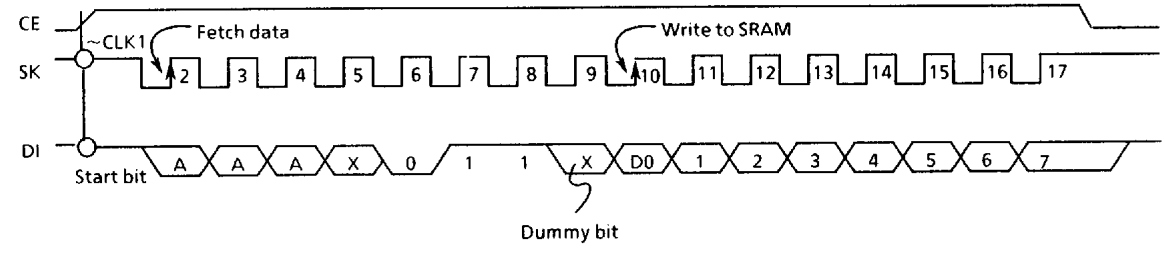


Figure 12 Write mode timing

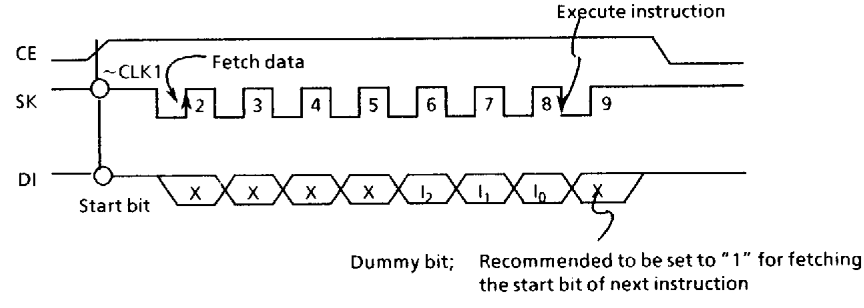


Figure 13 Other operation mode timing

Interfacing example 1 : With Intel 8051, 8052

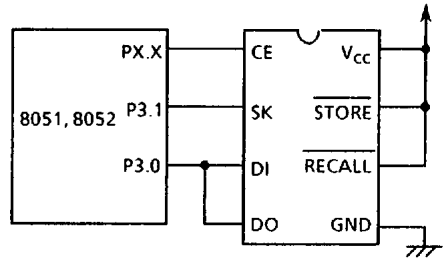


Figure 14

Interfacing example 2 : With other CPU

When S-24H30R/I is connected to CPU other than Intel 8051 and 8052, delay circuit should be set by capacitor and resistor at DO terminal (Figure 15), delaying the signal more than 200 ns as in Figure 16 to assure the data hold time (t_{DHU}) and the data setup time (t_{DSU}) of CPU.

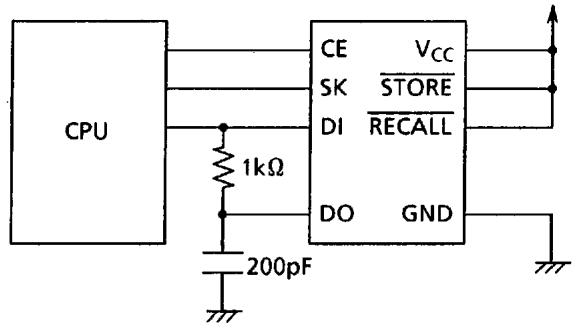


Figure 15

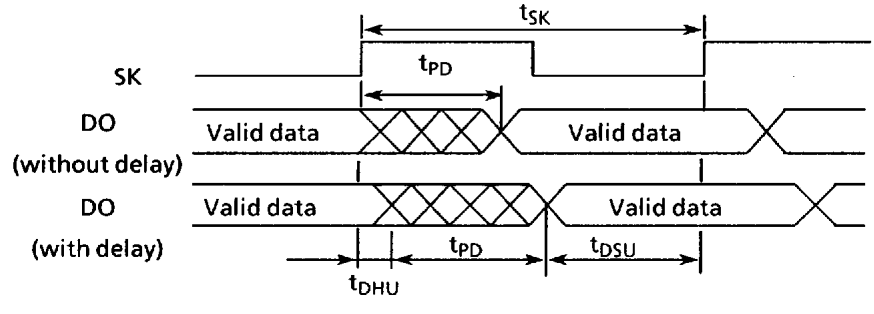


Figure 16

The maximum speed of the SK clock (f_{SKMAX}) is expressed by the following formula:

$$f_{SKMAX} = \frac{1}{t_{SK}} = \frac{1}{t_{DSU} + t_{DHU} + t_{PD}\,max.}$$

For example, when interfacing with NEC μPD75XX series, f_{SKMAX} is as follows:

μPD75XX series t_{DSU} : 300 ns min.

t_{DHU} : 450 ns min.

S-24H30R/I t_{PD} : 0 ns min. , 300 ns max.

$$f_{SKMAX} = \frac{1}{t_{SK}} = \frac{1 \times 10^9}{300 + 450 + 300} = \frac{1}{1.05\ \mu s} = 952\ kHz$$

■ Dimensions (Unit:mm)

1. S-24H30R/I (8-pin DIP)

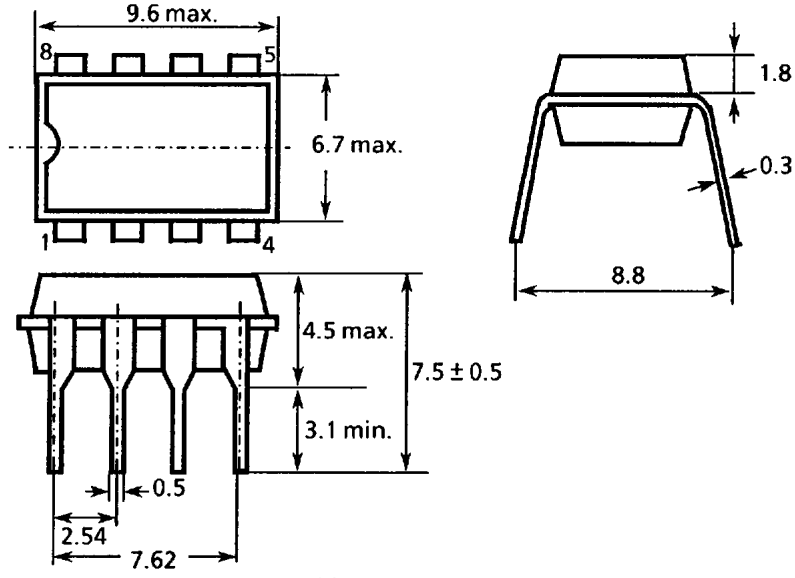


Figure 17

2. S-24H30RF/IF (8-pin SOP)

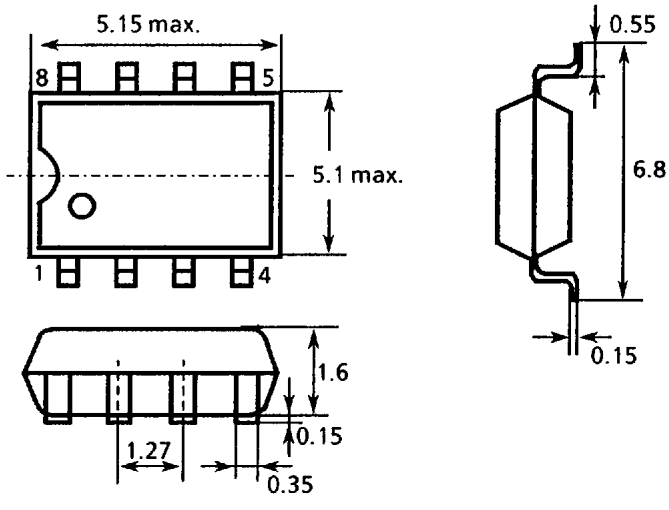


Figure 18

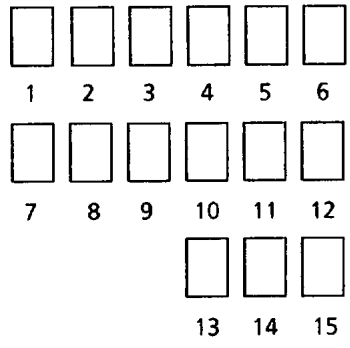
■ Ordering Information

Table 11

Product name	Store cycles	Store cycles per bit	Temperature	Package
S-24H30R 01/10	$10^4/10^5$	$10^4/10^5$	0°C to + 70°C	Plastic DIP
S-24H30I 01/10	$10^4/10^5$	$10^4/10^5$	-40°C to + 85°C	Plastic DIP
S-24H30RF 01/10	$10^4/10^5$	$10^4/10^5$	0°C to + 70°C	Plastic SOP
S-24H30IF 01/10	$10^4/10^5$	$10^4/10^5$	-40°C to + 85°C	Plastic SOP

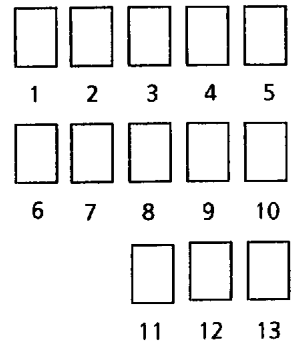
■ Markings

1. S-24H30R/I (8-pin DIP)



1 to 9 : Product name
10 to 12 : Lot No.
13 : Assembly mark
14 : Last column of year
15 : Month of manufacture: January = 1, February = 2, March = 3, April = 4, May = 5, June = 6, July = 7,August = 8, September = 9, October = X, November = Y, December = Z

2. S-24H30RF/IF (8-pin SOP)

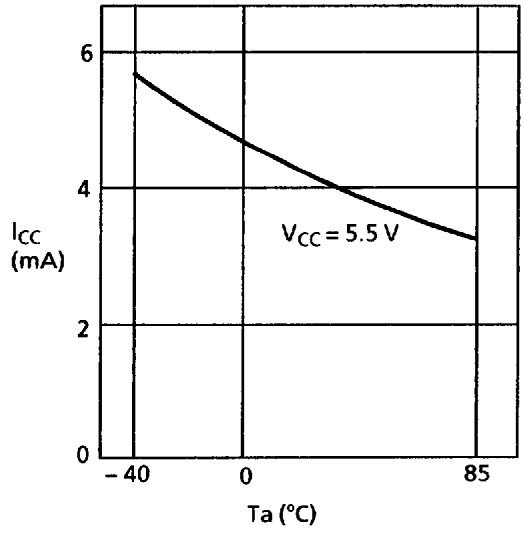


1 to 10 : Product name
11 : Month of manufacture: January = 1, February = 2, March = 3, April = 4, May = 5, June = 6, July = 7, August = 8, September = 9, October = X, November = Y, December = Z
12 to 13 : Lot No.

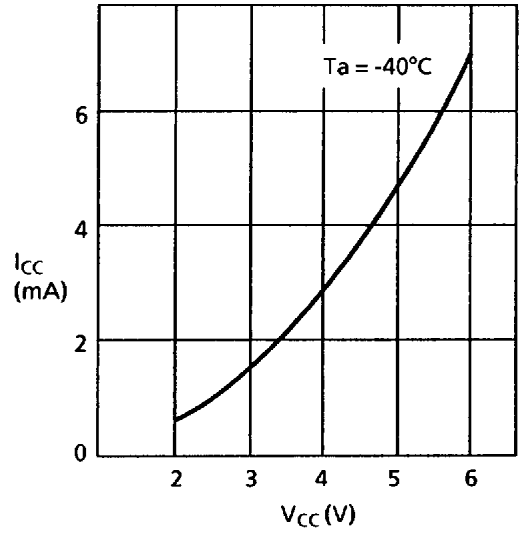
■ Characteristics

1. DC characteristics

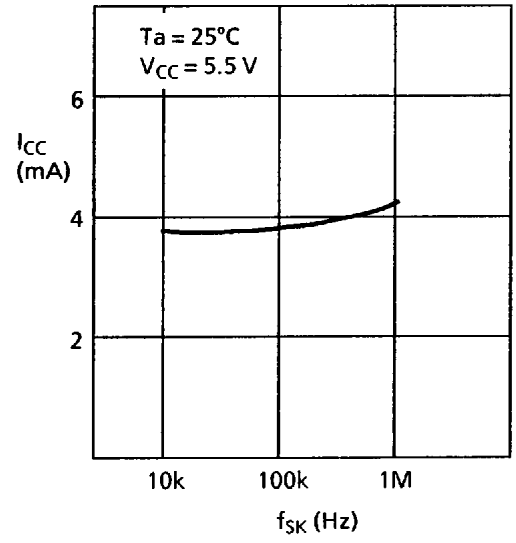
1.1 Operating current consumption I_{CC} — Ambient temperature Ta



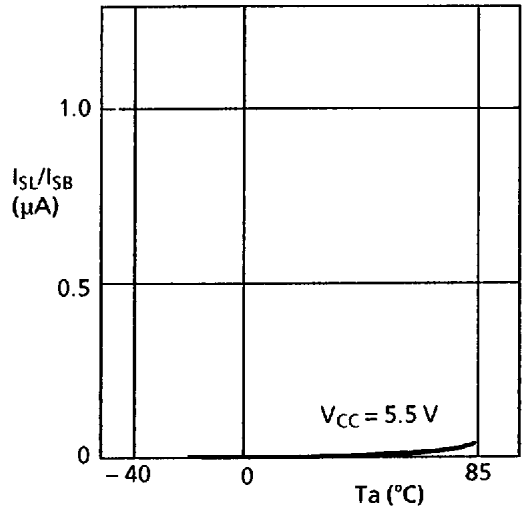
1.2 Operating current consumption I_{CC} — Power supply voltage V_{CC}



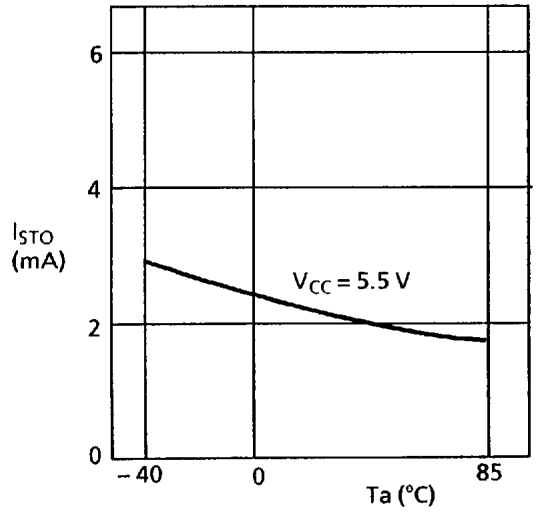
1.3 Operating current consumption I_{CC} — SK frequency f_{SK}



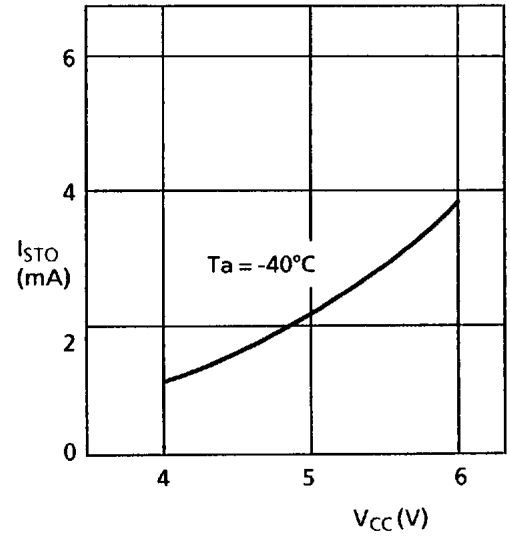
1.4 Sleep/standby current consumption I_{SL}/I_{SB} — Ambient temperature Ta



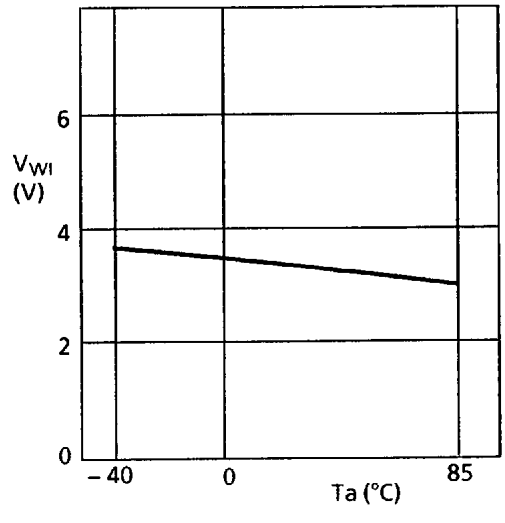
1.5 Store current consumption I_{STO} — Ambient temperature Ta



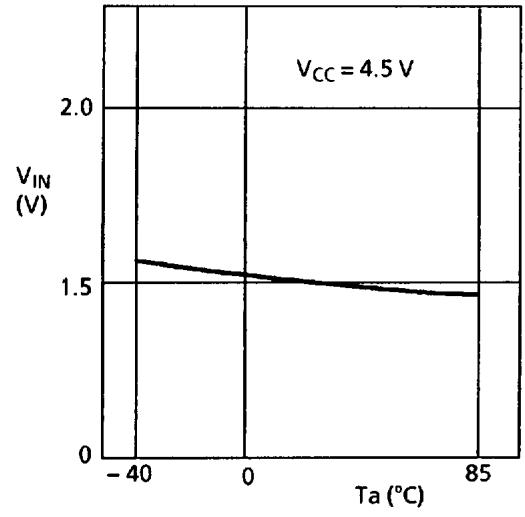
1.6 Store current consumption I_{STO} — Power supply voltage V_{CC}



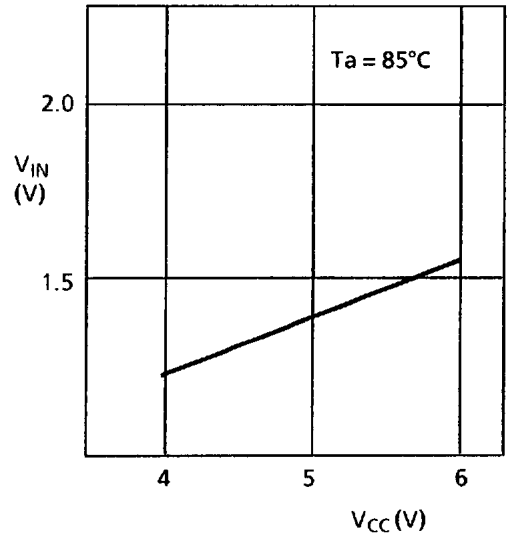
1.7 Store inhibition voltage V_{WI} — Ambient temperature Ta



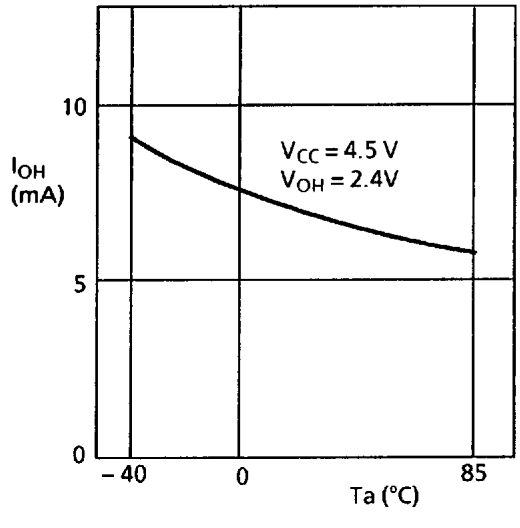
1.8 Input voltage V_{IN} — Ambient temperature Ta



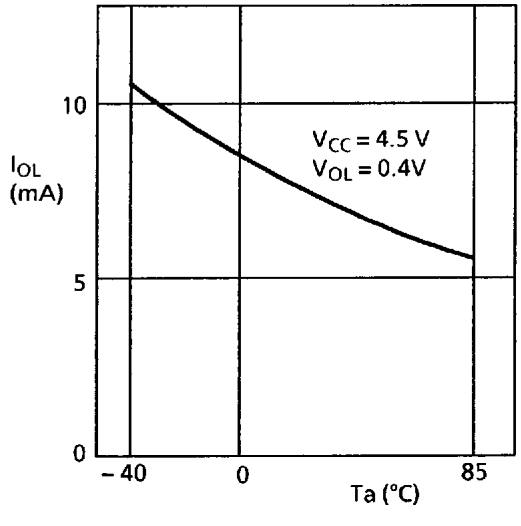
1.9 Input voltage V_{IN} — Power supply voltage V_{CC}



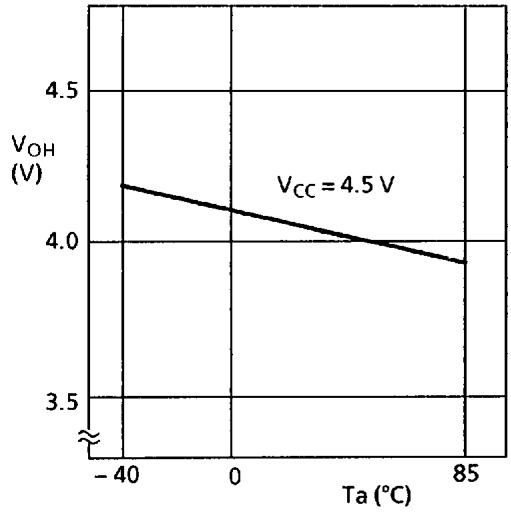
1.10 High level output current I_{OH} — Ambient temperature Ta



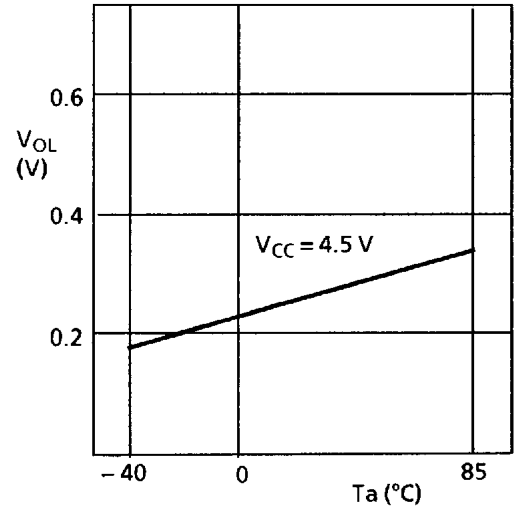
1.11 Low level output current I_{OL} — Ambient temperature Ta



1.12 High level output voltage V_{OH} — Ambient temperature Ta

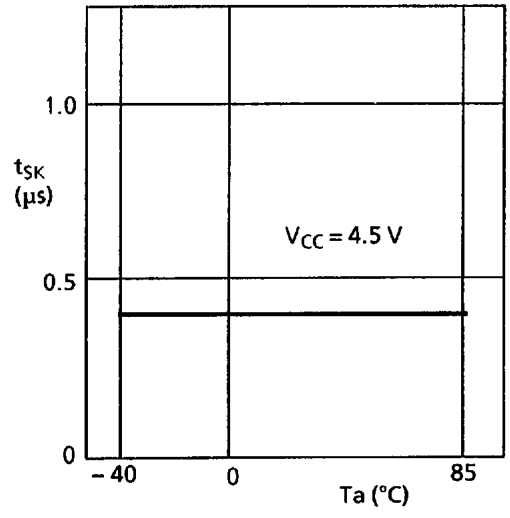


1.13 Low level output voltage V_{OL} — Ambient temperature Ta

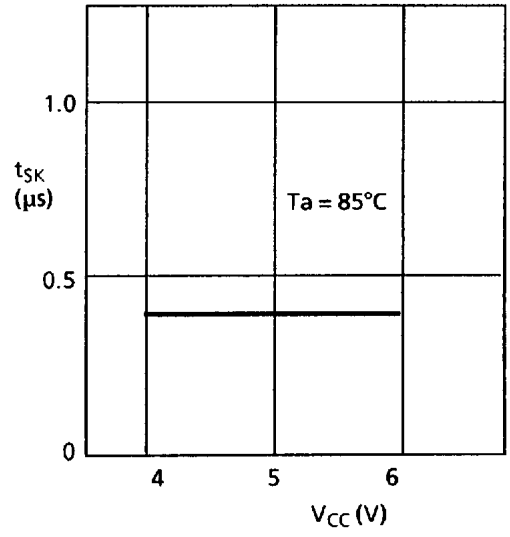


2. AC characteristics

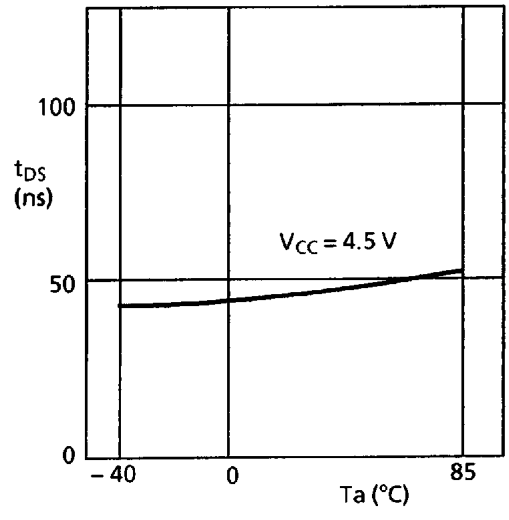
2.1 SK pulse width t_{SK} — Ambient temperature Ta



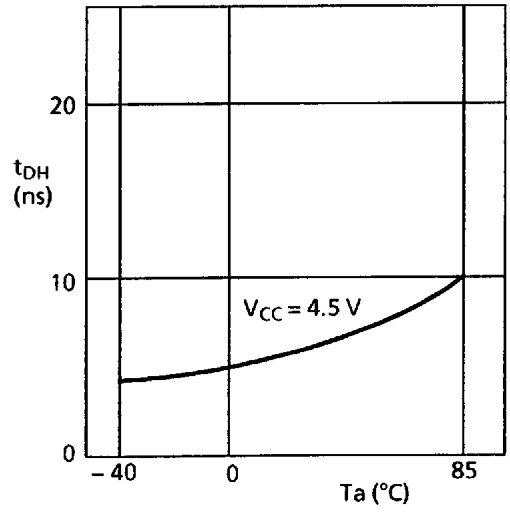
2.2 SK pulse width t_{SK} — Power supply voltage V_{CC}



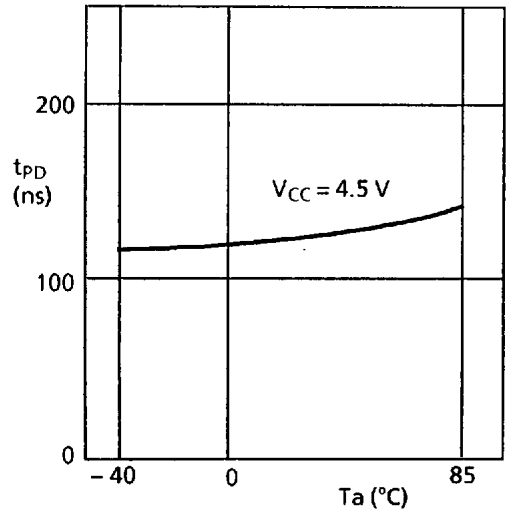
2.3 Input data setup time t_{DS} — Ambient temperature Ta



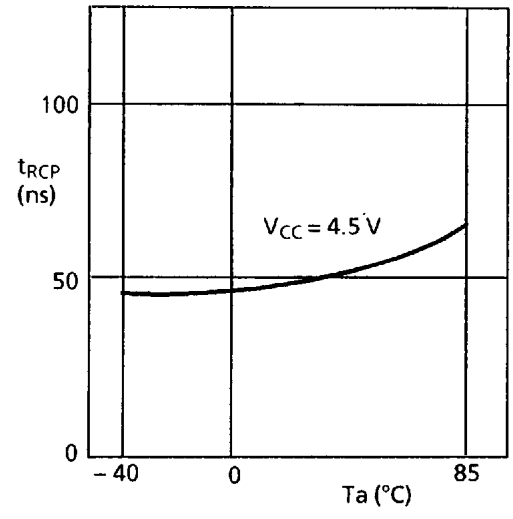
2.4 Input data hold time t_{DH} — Ambient temperature Ta



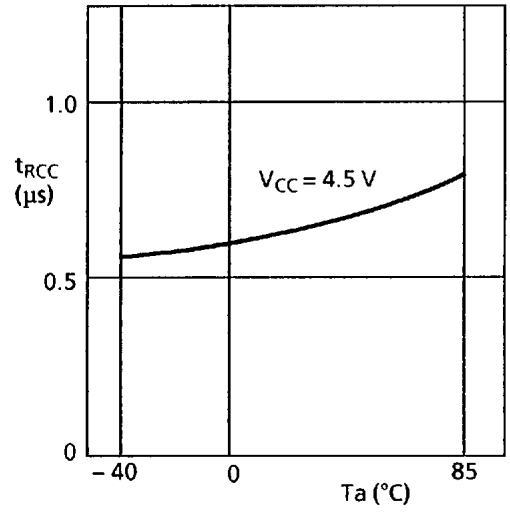
2.5 SK data valid time t_{PD} — Ambient temperature Ta



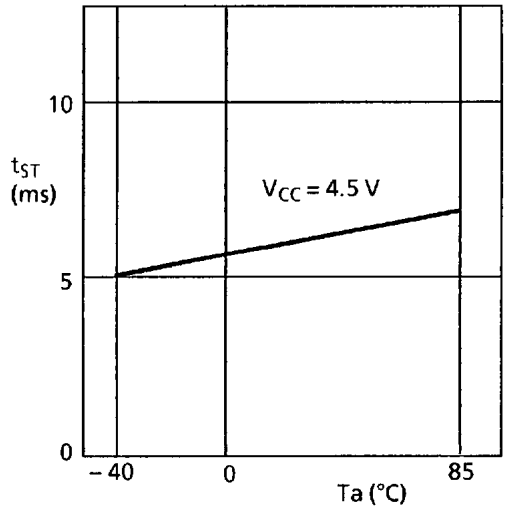
2.6 Recall pulse width t_{RCP} — Ambient temperature Ta



2.7 Recall cycle time t_{RCC} — Ambient temperature Ta



2.8 Store time t_{ST} — Ambient temperature Ta



3. Endurance characteristics