SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER WITH PRESET INPUTS

S54193
N74193

S54193–B,F,W • N74193–B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S54193 and N74193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The oututs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, the outputs may be preset to any state by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

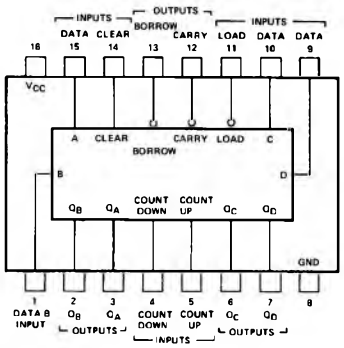
A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. An input buffer has been placed on the clear, count, and load inputs to lower the drive requirements to one normalized Series 54/74 load. This is important when the output of the driving circuitry is somewhat limited.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

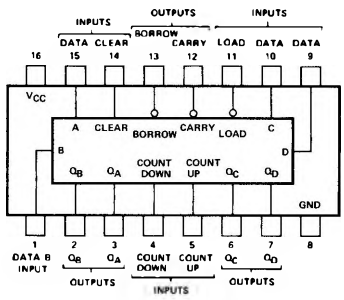
Power dissipation is typically 325 milliwatts for either the decade or binary version. Maximum input count frequency is typically 32 megahertz and is guaranteed to be 25MHz minimum. All inputs are buffered and represent only one normalized Series 54/74 load. Input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

PIN CONFIGURATIONS

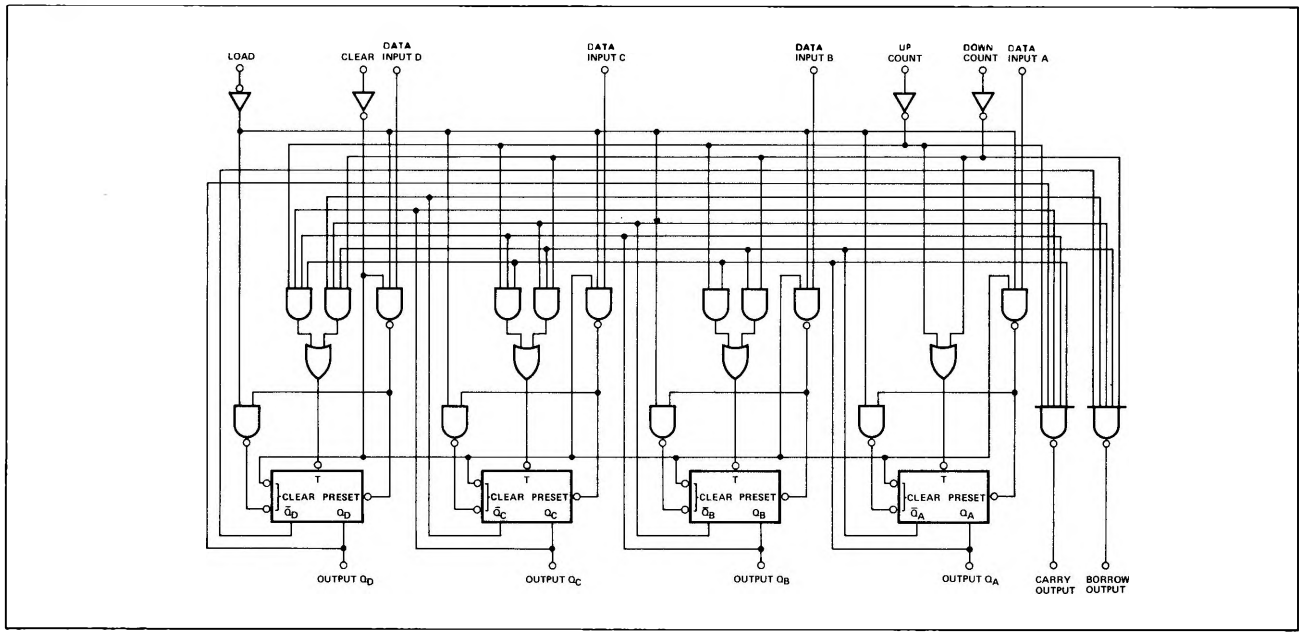
W PACKAGE



B,F PACKAGE

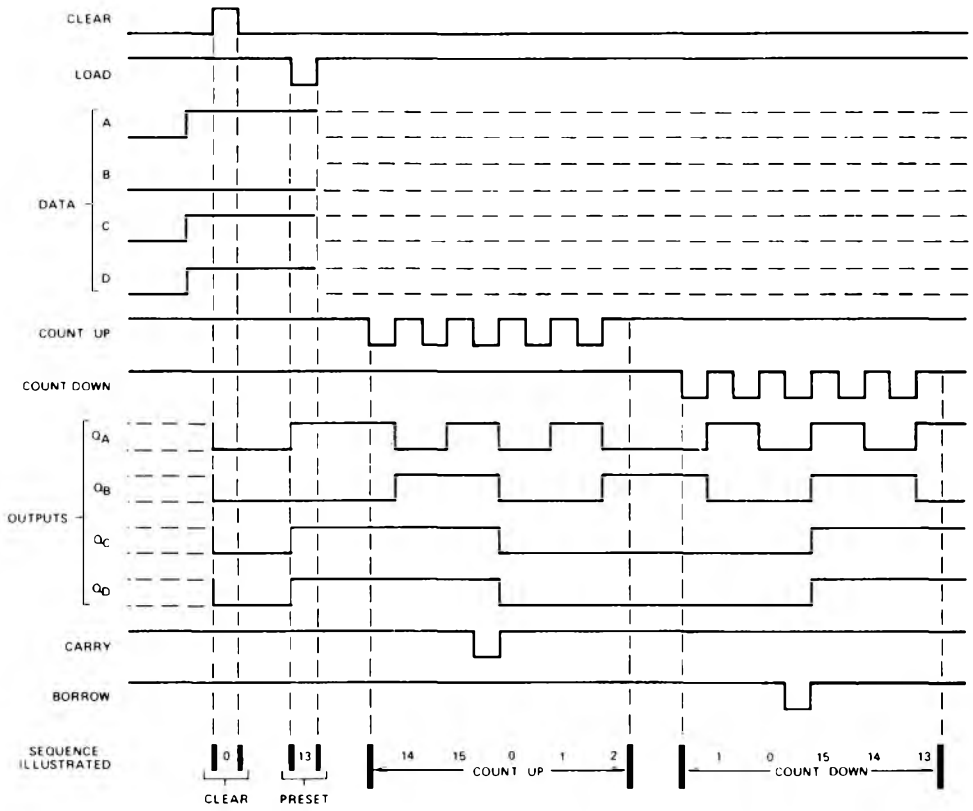


LOGIC DIAGRAM



BINARY COUNTER (typical clear, load, and count sequences)

Illustrated below is the following sequence:
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES:
A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

RECOMMENDED OPERATING CONDITIONS

	S54193			N74193			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10			10	
Input Count Frequency, f_{count}	0		25*	0		25*	MHz
Width of Any Input Pulse, t_w	20*			20*			ns
Data Setup Time, t_{setup} (See Note 2)	20*			20*			ns
Data Hold Time, t_{hold} (See Note 3)	0			0			ns
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

NOTES:
1. Voltage values are with respect to network ground terminal.
2. Setup time is the interval immediately preceding the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
3. Hold time is the interval immediately following the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

*These conditions are recommended for use at V_{CC} = 5V, T_A = 25°C.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
S54193							
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -400μA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40	μA
		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		-20		-65	mA
I_{CC}	Supply current	V_{CC} = MAX			65	89	mA
N74193							
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -400μA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40	μA
		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		-18		-65	mA
I_{CC}	Supply current	V_{CC} = MAX			65	102	mA

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10 (See Note)

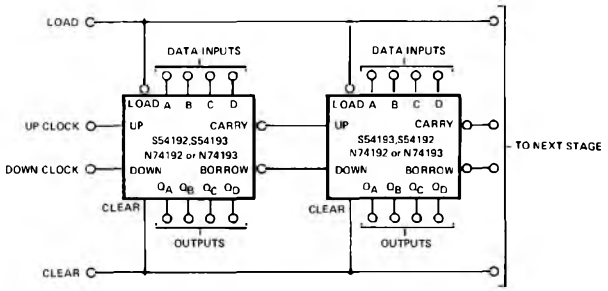
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15pF, R_L = 400Ω	25	32		MHz
t_{setup}	Minimum input setup time			14	20	ns
t_{PLH}	Propagation delay time, low-to-high-level carry output from count-up input			17	26	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from count-up input			16	24	ns
t_{PLH}	Propagation delay time, low-to-high-level borrow output from count-down input			16	24	ns
t_{PHL}	Propagation delay time, high-to-low-level borrow output from count-down input			16	24	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from either count input			25	38	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from either count input			31	47	ns
t_{PLH} LOAD				27	40	
t_{PLH} LOAD				29	40	
t_{PHL} CLEAR				22	25	

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

CASCADING



Circuitry is provided internally for cascading these counters. The mode of cascading shown is ripple borrow/carry. No external components are required.