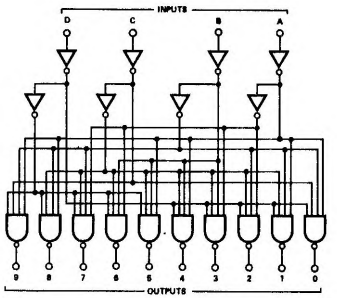
DESCRIPTION

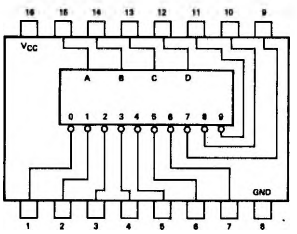
The 54/7444 Excess-3-Gray Code to Decimal Decoder is a TTL MSI array utilized in decoding and logic conversion applications. The 54/7444 decodes excess three gray code to one of ten outputs.

LOGIC DIAGRAM



PIN CONFIGURATIONS

B,F,W PACKAGE



TRUTH TABLE

S5444/N7444 EXCESS 3 GRAY INPUT

D	C	B	A
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	1
0	1	0	0
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0
1	0	1	0
1	0	1	1
1	0	0	1
1	0	0	0
0	0	0	0
0	0	0	1
0	0	1	1

ALL TYPES DECIMAL OUTPUT

0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5444 Circuits	4.5	5	5.5	V
N7444 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$		V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = -400μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX,	S5444	-20		-55	mA
			N7444	-18		-55	mA
I_{CC}	Supply Current	V_{CC} = MAX,	S5444		28	41	mA
			N7444		28	56	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level through two logic levels	C_L = 15pF,	R_L = 400Ω	10	22	30	ns
t_{pd0}	Propagation delay time to logical 0 level through three logic levels	C_L = 15pF,	R_L = 400Ω		23	35	ns
t_{pd1}	Propagation delay time to logical 1 level through two logic levels	C_L = 15pF,	R_L = 400Ω	10	17	25	ns
t_{pd1}	Propagation delay time to logical 1 level through three logic levels	C_L = 15pF,	R_L = 400Ω		26	35	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.