

J-K EDGE-TRIGGERED FLIP-FLOP

S54H101 N74H101

S54H101-A,F,W • N74H101-A,F

DESCRIPTION

These monolithic J-K flip-flops are negative-edge-triggered. The AND-OR gate inputs are inhibited while the clock input is low; when the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum setup times are observed. Input data are transferred to the outputs on the negative edge of the clock pulse.

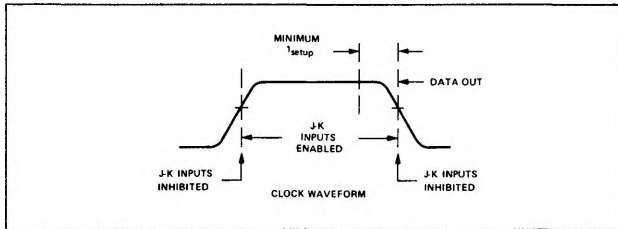
TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

NOTES:

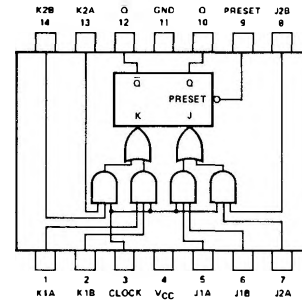
- $J = (J1A \bullet J1B) + (J2A \bullet J2B)$
- $K = (K1A \bullet K1B) + (K2A \bullet K2B)$
- t_n = Bit time before clock pulse
- t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM

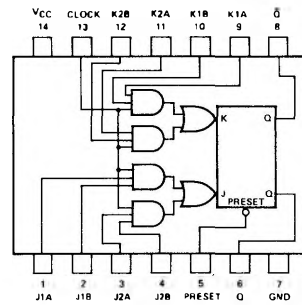


PIN CONFIGURATIONS

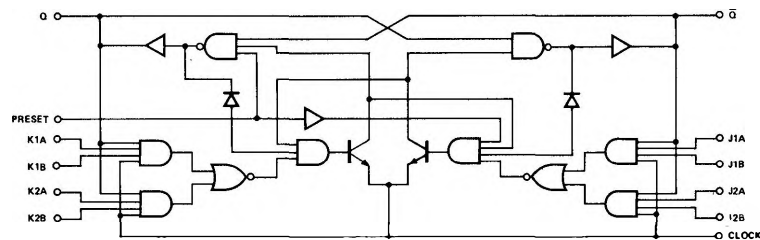
W PACKAGE



A,F PACKAGE



LOGIC DIAGRAM



SIGNETICS DIGITAL 54/74 TTL SERIES – S54H101 • N74H101

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} : S54H101 Circuits	4.5	5	5.5	V
N74H101 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A : S54H101 Circuits	-55	25	125	$^{\circ}$ C
N74H101 Circuits	0	25	70	$^{\circ}$ C
Normalized Fan-Out from each Output, N			10	
Width of Clock Pulse, $t_{p(\text{clock})}$	10			ns
Width of Preset Pulse, $t_{p(\text{preset})}$	16			ns
Input Setup Time, t_{setup} (See Above): Logical 1	10			ns
Logical 0	13			ns
Input Hold Time, t_{hold}	0			ns
Clock Pulse Transition Time, t_0			150	ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP†	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal		2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal				0.8	V
$V_{out(1)}$ Logical 1 output voltage	$V_{CC} = \text{MIN}, I_{\text{load}} = -500\mu\text{A}$	2.4	3.2		V
$V_{out(0)}$ Logical 0 output voltage	$V_{CC} = \text{MIN}, I_{\text{sink}} = 20 \text{ mA}$		0.25	0.4	V
$I_{in(0)}$ Logical 0 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, or preset	$V_{CC} = \text{MAX}, V_{in} = 0.4 \text{ V}$		-1	-2	mA
$I_{in(0)}$ Logical 0 level input current at clock	$V_{CC} = \text{MAX}, V_{in} = 0.4 \text{ V}$		-3	-4.8	mA
$I_{in(1)}$ Logical 1 level input current at J or K	$V_{CC} = \text{MAX}, V_{in} = 2.4 \text{ V}$			50	μA
$I_{in(1)}$ Logical 1 level input current at preset	$V_{CC} = \text{MAX}, V_{in} = 5.5 \text{ V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at clock	$V_{CC} = \text{MAX}, V_{in} = 2.4 \text{ V}$			100	μA
I_{OS} Short-circuit output current**	$V_{CC} = \text{MAX}, V_{in} = 5.5 \text{ V}$			1	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, V_{in} = 2.4 \text{ V}$	0		-1	mA
	$V_{CC} = \text{MAX}, V_{in} = 5.5 \text{ V}$			1	mA
	$V_{CC} = \text{MAX}, V_{in} = 0$	-40		-100	mA
	$V_{CC} = \text{MAX}$		20	38	mA

SWITCHING CHARACTERISTICS, $V_{CC} = 5\text{V}, T_A = 25^{\circ}\text{C}, N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock} Maximum input clock frequency	$C_L = 25 \text{ pF}, R_L = 280 \Omega$	40	50		MHz
t_{pd1} Propagation delay time to logical 1 level from preset to output	$C_L = 25 \text{ pF}, R_L = 280 \Omega$		8	12	ns
t_{pd0} Propagation delay time to logical 0 level from preset to output (clock low)	$C_L = 25 \text{ pF}, R_L = 280 \Omega$		23	35	ns
t_{pd0} Propagation delay time to logical 0 level from preset to output (clock high)	$C_L = 25 \text{ pF}, R_L = 280 \Omega$		15	20	ns
t_{pd1} Propagation delay time to logical 1 level from clock to output	$C_L = 25 \text{ pF}, R_L = 280 \Omega$	5	10	15	ns
t_{pd0} Propagation delay time to logical 0 level from clock to output	$C_L = 25 \text{ pF}, R_L = 280 \Omega$	8	16	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

† All typical values are at $V_{CC} = 5\text{V}, T_A = 25^{\circ}\text{C}$.