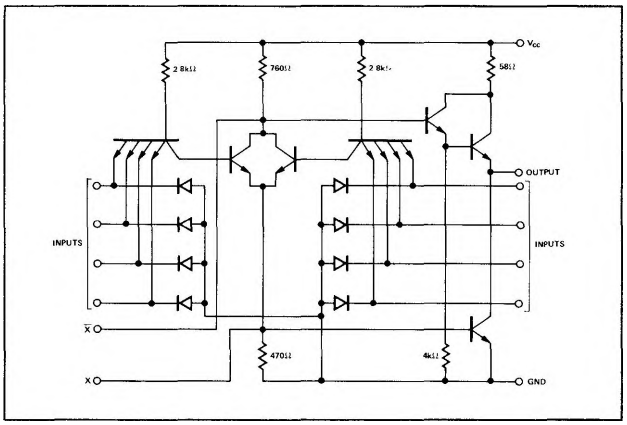
EXPANDABLE 4-INPUT AND-OR-INVERT GATES

S54H55 N74H55

S54H55–A,F,W • N74H55–A,F

DIGITAL 54/74 TTL SERIES

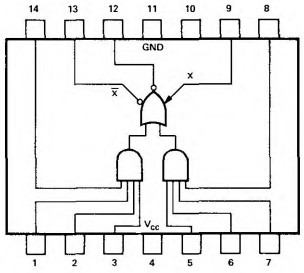
SCHEMATIC DIAGRAM



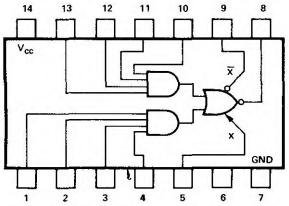
NOTES:
1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used, leave X and X pins open.
4. A total of four S54H60/N74H60 expander gates or one S54H62/N74H62 expander gate may be connected to the expander inputs.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H55 Circuits		4.5	5	5.5	V
N74H55 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H55 Circuits	-55	25	125	°C
	N74H55 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of either AND section to ensure logical 0 at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current**	V_{CC} = MAX,		-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		7.5	12	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		4.5	6.4	mA

ELECTRICAL CHARACTERISTICS (S54H55 circuits only) using expander inputs, V_{CC} = 4.5V, T_A = -55°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{in\overline{X}}$	Expander-node input current	$V_{\overline{X}}$ = 1.4V					-5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	I_{sink} = 20mA,	I_1 = 700μA,	R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -500μA, I_2 = -320μA	I_1 = 320μA,		2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 20mA,	I_1 = 470μA,	R_1 = 68Ω			0.4	V

ELECTRICAL CHARACTERISTICS (N74H55 circuits only) using expander inputs, V_{CC} = 4.75V, T_A = 0°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{in\overline{X}}$	Expander-node input current	$V_{\overline{X}}$ = 1.4V					-6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	I_{sink} = 20mA,	I_1 = 1.1mA,	R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -500μA I_2 = -570μA	I_1 = 570μA,		2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 20mA,	I_1 = 600μA,	R_1 = 63Ω			0.4	V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10, expander pins are open

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		6.5	11	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		7	11	ns

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10, C_X = 15pF

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		7.7		ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		11.4		ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.

** Duration of short circuit test should not exceed 1 second.

† All typical values are at V_{CC}= 5V, T_A = 25°C.