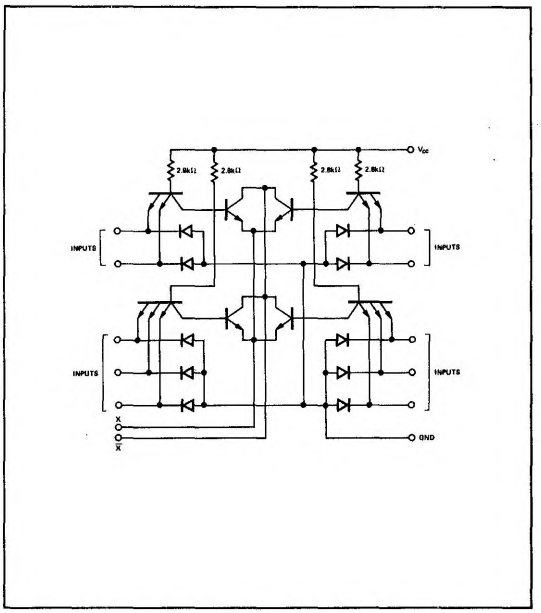
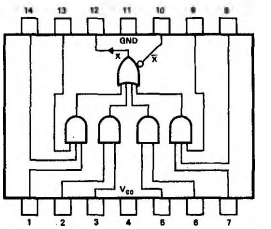
SCHEMATIC (each gate)

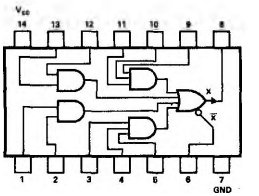


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



NOTES:
1. Connect to X input of S54H50, S54H53, or S54H55 circuit
2. Connect to $\overline{X}$ input of S54H50, S54H53, or S54H55 circuit
3. Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}	4.5V to 5.5V
Maximum number of expanders that may be fanned-in to one S54H50, S54H53, or S54H55 circuit	1

ELECTRICAL CHARACTERISTICS (unless otherwise noted T_A = -55°C to 125°C)

	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure output is in the on state	V_{CC} = 4.5V			2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure output is in the off state	V_{CC} = 4.5V,					0.8	V
V_{on}	On-state output voltage	V_{CC} = 4.5V, I_{on} = 5.85mA,	V_{in} = 2V, T_A = -55°C	V_1 = 1V,			0.4	V
		V_{CC} = 5.5V, I_{on} = 7.85mA,	V_{in} = 2V, T_A = 125°C	V_1 = 0.6V,			0.4	V
I_{off}	Off-state output current	V_{CC} = 4.5V, R = 575Ω,	V_{in} = 0.8V, T_A = -55°C	V_1 = 4.5V,			320	μA
I_{on}	On-state output current	V_{CC} = 4.5V, T_A = -55°C	V_{in} = 2V,	V_1 = 1V,	-470			μA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = 5.5V,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = 5.5V,	V_{in} = 2.4V			50	μA
		V_{CC} = 5.5V,	V_{in} = 5.5V			1	mA
$I_{CC(on)}$	On-state supply current	V_{CC} = 5.5V, V_1 = 0.85V	V_{in} = 4.5V,		3.8	7	mA
$I_{CC(off)}$	Off-state supply current	V_{CC} = 5.5V, V_1 = 0.85V	V_{in} = 0,		6	9	mA

OUTPUT CAPACITANCE, V_{CC} and GND terminals open, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cx	Effective capaitance of output transistor Q_1	f = 1 MHz		1.3		pF

†All typical values are at V_{CC} = 5V, T_A = 25°C.