signetics

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

S54S195
N74S195

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These high-performance 4-bit registers feature a 110-megahertz typical maximum shift-frequency which makes them particularly attractive for very high-speed data processing systems. As the pin assignments are the same as the S54195 and N74195, existing systems can in most cases be upgraded merely by utilizing the Schottky-clamped versions. The registers have two modes of operation:

Parallel (Broadside) Load
Shift (In the direction Q_A toward Q_D)

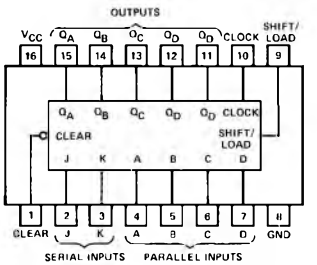
Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

These shift registers are fully compatible with other TTL families. All inputs are buffered to lower the drive requirements to one normalized Series 54S/74S load, including the clock input. The S54S195 is characterized for operation over the full military temperature range of −55°C to 125°C; the N74S195 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATION

J OR N DUAL-IN-LINE OR W FLAT PACKAGE
(TOP VIEW)



Positive Logic: See function table

FEATURES

- SCHOTTKY-CLAMPED TO ACHIEVE TYPICAL MAXIMUM SHIFT FREQUENCY OF 110 MHz
- FUNCTIONALLY AND MECHANICALLY IDENTICAL TO N54195, S74195 AND CAN BE USED TO UPGRADE EXISTING DESIGNS WITH SIGNIFICANT IMPROVEMENT IN SPEED
- FULLY COMPATIBLE WITH OTHER TTL CIRCUITS
- N54S195 OPERATES OVER FULL MILITARY TEMPERATURE RANGE OF −55°C TO 125°C
- USE IN HIGH-PERFORMANCE:
  ACCUMULATORS/PROCESSORS
  SERIAL-TO-PARALLEL,
  PARALLEL-TO-SERIAL CONVERTERS

FUNCTION TABLE

INPUTS									OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	A	B	C	D	A	B	C	D	$\overline{D}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{B0}	Q_{C0}	$\overline{Q}_{C0}$
H	H	↑	L	L	X	X	X	X	L	Q_{A0}	Q_{B0}	Q_{C0}	$\overline{Q}_{C0}$
H	H	↑	H	H	X	X	X	X	H	Q_{A0}	Q_{B0}	Q_{C0}	$\overline{Q}_{C0}$
H	H	↑	H	L	X	X	X	X	Q_{A0}	Q_{A0}	Q_{B0}	Q_{B0}	$\overline{Q}_{C0}$

H = High level (steady state)
L = Low level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from low to high level
A, B, C, D, = The level of steady state input at A, B, C, or D respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D respectively before the indicated steady state input conditions were established.

RECOMMENDED OPERATING CONDITIONS

		S54S195			N74S195			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		75	0		75	MHz
Width of clock input pulse, $t_{w(clock)}$		12			12			ns
Width of clear input pulse, $t_{w(clear)}$		12			12			ns
Setup time, t_{setup}	Shift/load	12			12			ns
	Serial and parallel data	10			10			
	Clear inactive-state	15			15			
Shift/load release time, $t_{release}$				7			7	ns
Serial and parallel data hold time, t_{hold}		2			2			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA					−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	S54S195		2.5	3.4		V
			N74S195		2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA					0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					−2	mA
I_{OS}	Short-circuit output current‡	V_{CC} = MAX			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 1	S54S195			75	99	mA
			N74S195			75	109	

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15 pF, R_L = 280 Ω, See Note 2	75	110		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			11		ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			9		ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			10		ns

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

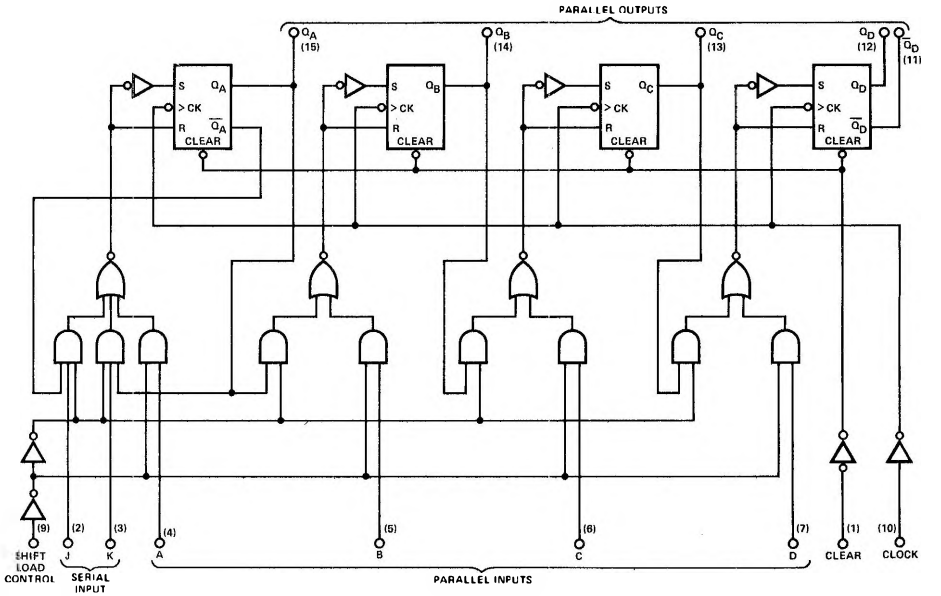
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTES: 1. With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

2. Load circuit and waveforms are shown on page 2-293 with the following additions: $t_{w(clock)} \geq 12$ns, $t_{w(clear)} \geq 12$ns.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES