

# DATA SHEET

## **SA8016**

2.5GHz low voltage fractional-N  
synthesizer

Product specification  
Supersedes data of 1999 Mar 08

1999 Apr 16

## 2.5GHz low voltage fractional-N synthesizer

SA8016

## GENERAL DESCRIPTION

The SA8016 BICMOS device integrates programmable dividers, charge pumps and a phase comparator to implement a phase-locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at VCO input frequencies up to 2.5 GHz. The synthesizer has fully programmable main and reference dividers. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage.  $V_{DDCP}$  must be greater than or equal to  $V_{DD}$ .

The charge pump current (gain) is set by an external resistance at the RSET pin. Only passive loop filters could be used; the charge pump operates within a wide voltage compliance range to provide a wider tuning range.

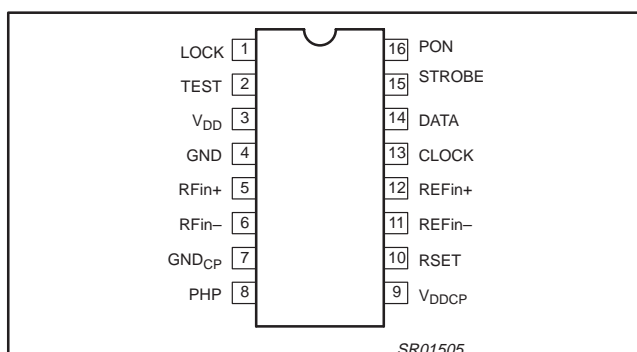


Figure 1. Pin Configuration

## FEATURES

- Low phase noise
- Low power
- Fully programmable main divider
- Internal fractional spurious compensation
- Hardware and software power down
- Split supply for  $V_{DD}$  and  $V_{DDCP}$

## APPLICATIONS

- 350–2500 MHz wireless equipment
- Cellular phones (all standards)
- WLAN
- Portable battery-powered radio equipment.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DD}$	Supply voltage		2.7	–	5.5	V
$V_{DDCP}$	Analog supply voltage	$V_{DDCP} \geq V_{DD}$	2.7	–	5.5	V
$I_{DDCP}+I_{DD}$	Supply current		–	8.0	9.5	mA
$I_{DDCP}+I_{DD}$	Total supply current in power-down mode		–	1	–	$\mu$ A
$f_{VCO}$	Input frequency		350	–	2500	MHz
$f_{REF}$	Crystal reference input frequency		5	–	40	MHz
$f_{PC}$	Maximum phase comparator frequency		–	–	4	MHz
$T_A$	Operating ambient temperature		–40	–	+85	$^{\circ}$ C

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA8016	TSSOP16	Plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403–1

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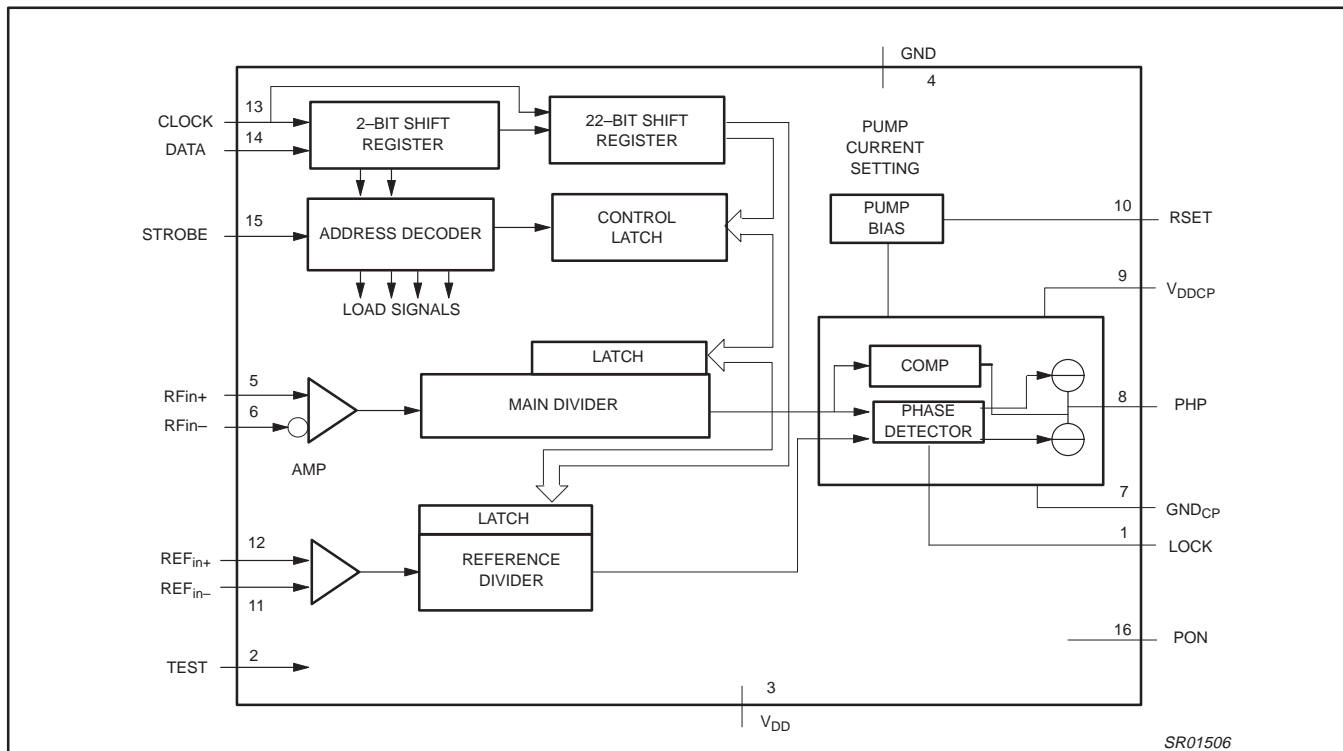


Figure 2. Block Diagram

### PINNING

SYMBOL	PIN	DESCRIPTION
LOCK	1	Lock detect output
TEST	2	Test (should be either grounded or connected to V <sub>DD</sub> )
V <sub>DD</sub>	3	Digital supply
GND	4	Digital ground
RFin+	5	RF input to main divider
RFin-	6	RF input to main divider
GND <sub>CP</sub>	7	Charge pump ground
PHP	8	Main normal charge pump
V <sub>D</sub> DCP	9	Charge pump supply voltage
RSET	10	External resistor from this pin to ground sets the charge pump current
REFIn-	11	Reference input
REFIn+	12	Reference input
CLOCK	13	Programming bus clock input
DATA	14	Programming bus data input
STROBE	15	Programming bus enable input
PON	16	Power down control

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DD}$	Digital supply voltage	-0.3	+5.5	V
$V_{DDCP}$	Analog supply voltage	-0.3	+5.5	V
$\Delta V_{DDCP} - V_{DD}$	Difference in voltage between $V_{DDCP}$ and $V_{DD}$ ( $V_{DDCP} \geq V_{DD}$ )	-0.3	+2.8	V
$V_n$	Voltage at pins 1, 2, 5, 6, 11 to 16	-0.3	$V_{DD} + 0.3$	V
$V_1$	Voltage at pin 8, 9	-0.3	$V_{DDCP} + 0.3$	V
$\Delta V_{GND}$	Difference in voltage between $GND_{CP}$ and $GND$ (these pins should be connected together)	-0.3	+0.3	V
$T_{stg}$	Storage temperature	-55	+125	°C
$T_{amb}$	Operating ambient temperature	-40	+85	°C
$T_j$	Maximum junction temperature		150	°C

**Handling**

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	VALUE	UNIT
$R_{thj-a}$	Thermal resistance from junction to ambient in free air	120	K/W

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**CHARACTERISTICS** $V_{DDCP} = V_{DD} = +3.0V$ ,  $T_A = +25^\circ C$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply; pins 3, 9</b>						
$V_{DD}$	Digital supply voltage		2.7	–	5.5	V
$V_{DDCP}$	Analog supply voltage	$V_{DDCP} = V_{DD}$	2.7	–	5.5	V
$I_{DDTotal}$	Synthesizer operational digital supply current	$V_{DD} = +3.0 V$	–	8.0	9.5	mA
$I_{Standby}$	Total supply current in power-down mode	logic levels 0 or $V_{DD}$	–	1		$\mu A$
<b>RFin main divider input; pins 5, 6</b>						
$f_{VCO}$	VCO input frequency		350	–	2500	MHz
$V_{RFin(rms)}$	AC-coupled input signal level	$R_{in}$ (external) = $R_s = 50\Omega$ ; single-ended drive; max. limit is indicative @ 500 to 2500 MHz	–18	–	0	dBm
$Z_{IRFin}$	Input impedance (real part)	$f_{VCO} = 2.4 GHz$	–	210	–	$\Omega$
$C_{IRFin}$	Typical pin input capacitance	$f_{VCO} = 2.4 GHz$	–	1.0	–	pF
$N_{main}$	Main divider ratio		512	–	65535	
$f_{PCmax}$	Maximum loop comparison frequency	indicative, not tested	–	–	4	MHz
<b>Reference divider input; pins 11, 12</b>						
$f_{REFin}$	Input frequency range from TCXO		5	–	40	MHz
$V_{RFin}$	AC-coupled input signal level	single-ended drive; max. limit is indicative	360	–	1300	mV <sub>PP</sub>
$Z_{REFin}$	Input impedance (real part)	$f_{REF} = 20 MHz$	–	10	–	k $\Omega$
$C_{REFin}$	Typical pin input capacitance	$f_{REF} = 20 MHz$	–	1.0	–	pF
$R_{REF}$	Reference division ratio		4	–	1023	
<b>Charge pump current setting resistor input; pin 10</b>						
$R_{SET}$	External resistor from pin to ground		6	7.5	15	k $\Omega$
$V_{SET}$	Regulated voltage at pin	$R_{SET} = 7.5 k\Omega$	–	1.25	–	V
<b>Charge pump outputs (including fractional compensation pump); pin 8; <math>R_{SET} = 7.5k\Omega</math>, <math>FC=80</math></b>						
$I_{CP}$	Charge pump current ratio to $I_{SET}^1$	Current gain $I_{PH}/I_{SET}$	–15		+15	%
$I_{MATCH}$	Sink-to-source current matching	$V_{PH} = 1/2 V_{DDCP}$	–10		+10	%
$I_{ZOUT}$	Output current variation versus $V_{PH}^2$	$V_{PH}$ in compliance range	–10		+10	%
$I_{LPH}$	Charge pump off leakage current	$V_{PH} = 1/2 V_{CC}$	–10		+10	nA
$V_{PH}$	Charge pump voltage compliance		0.7	–	$V_{DDCP} - 0.8$	V
<b>Phase noise (<math>R_{SET} = 7.5 k\Omega</math>, <math>CP = 00</math>)</b>						
C/N	Synthesizer's contribution to close-in phase noise of 800 MHz RF signal at 1 kHz offset.	$f_{REF} = 19.44MHz$ , TCXO, $f_{COMP} = 240kHz$ indicative, not tested	–	–85	–	dBc/Hz
	Synthesizer's contribution to close-in phase noise of 1800 MHz RF signal at 1 kHz offset.		–	–78	–	dBc/Hz
	Synthesizer's contribution to close-in phase noise of 2100 MHz RF signal at 1 kHz offset.		–	–77	–	dBc/Hz
<b>Interface logic input signal levels; pins 13, 14, 15, 16</b>						
$V_{IH}$	HIGH level input voltage		$0.7 \cdot V_{DD}$	–	$V_{DD} + 0.3$	V
$V_{IL}$	LOW level input voltage		–0.3	–	$0.3 \cdot V_{DD}$	V
$I_{LEAK}$	Input leakage current	logic 1 or logic 0	–0.5	–	+0.5	$\mu A$

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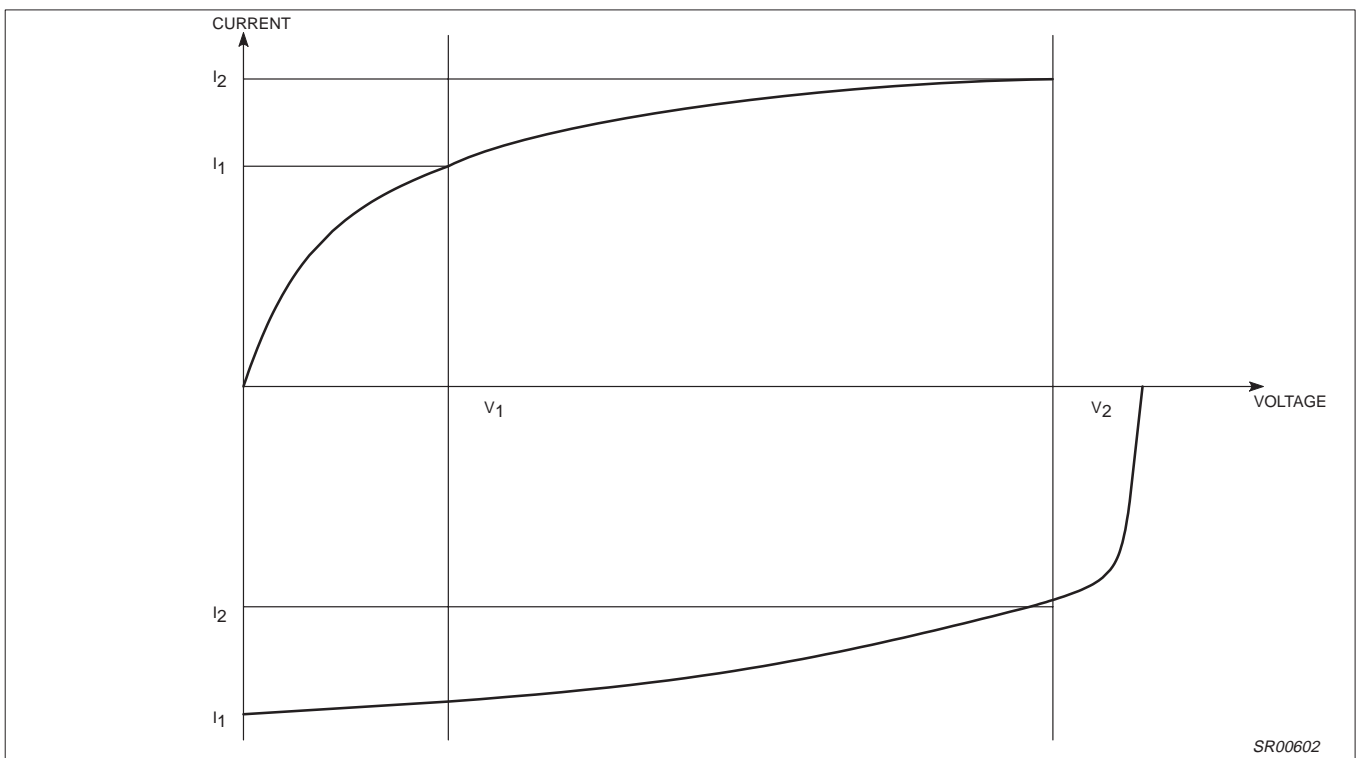
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Lock detect output signal (in push/pull mode); pin 1</b>						
V <sub>OL</sub>	LOW level output voltage	I <sub>sink</sub> = 2mA	-	-	0.4	V
V <sub>OH</sub>	HIGH level output voltage	I <sub>source</sub> = -2mA	V <sub>DD</sub> -0.4	-	-	V

**NOTES:**

1.  $I_{SET} = \frac{V_{SET}}{R_{SET}}$  bias current for charge pumps.

2. The relative output current variation is defined as:

$$\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{I(I_2 + I_1)}; \text{ with } V_1 = 0.7V, V_2 = V_{DDCP} - 0.8V \text{ (See Figure 3.)}$$



**Figure 3. Relative Output Current Variation**

SR00602

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## FUNCTIONAL DESCRIPTION

### Main Fractional-N divider

The RFin inputs drive a pre-amplifier to provide the clock to the first divider stage. For single ended operation, the signal should be fed to one of the inputs while the other one is AC grounded. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from -18dBm to 0dBm, and at frequencies as high as 2.5 GHz. The divider consists of a fully programmable bipolar prescaler followed by a CMOS counter. Total divide ratios range from 512 to 65536.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented by the value of NF. The accumulator works with modulo Q set by FMOD. When the accumulator overflows, the overall division ratio N will be increased by 1 to N + 1, the average division ratio over Q main divider cycles (either 5 or 8) will be

$$N_{frac} = N + \frac{NF}{Q}$$

The output of the main divider will be modulated with a fractional phase ripple. The phase ripple is proportional to the contents of the

fractional accumulator and is nulled by the fractional compensation charge pump.

The reloading of a new main divider ratio is synchronized to the state of the main divider to avoid introducing a phase disturbance.

### Reference divider

The reference divider consists of a divider with programmable values between 4 and 1023 followed by a three bit binary counter. The 3 bit SM (SA) register (see Figure 4) determines which of the 5 output pulses are selected as the main (auxiliary) phase detector input.

### Phase detector (see Figure 5)

The reference and main (aux) divider outputs are connected to a phase/frequency detector that controls the charge pump. The pump current is set by an external resistor in conjunction with control bits CP0 and CP1 in the B-word (see Charge Pump table). The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by forcing the pumps ON for a minimum time at every cycle (backlash time) providing improved linearity.

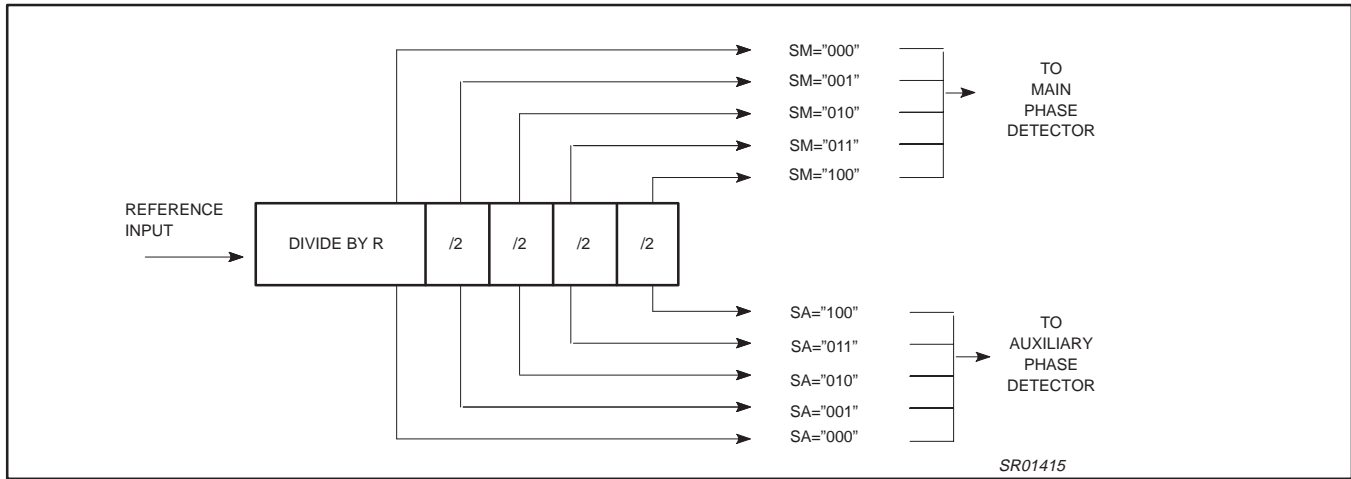


Figure 4. Reference Divider

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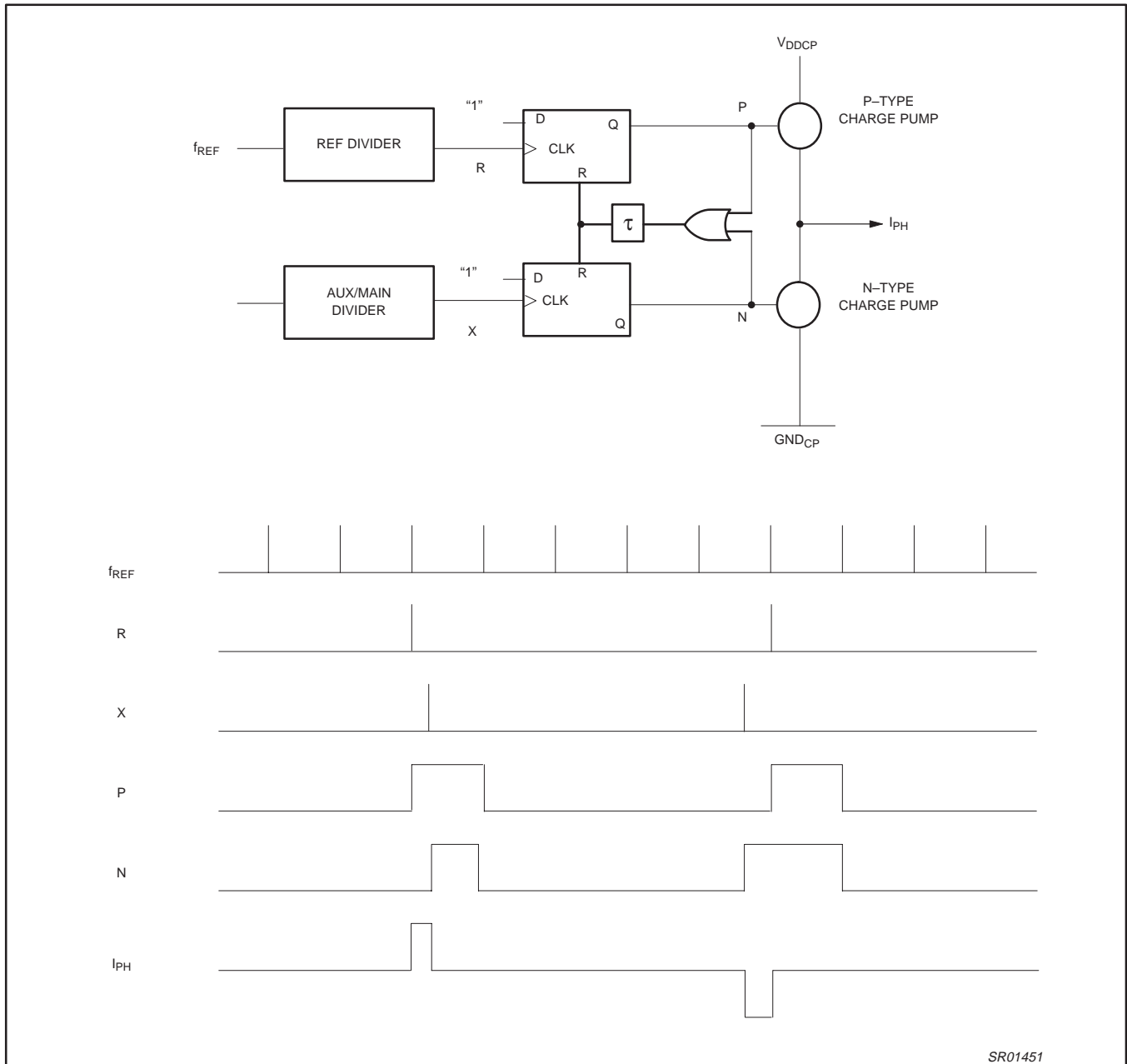


Figure 5. Phase Detector Structure with Timing

SR01451



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## Main Output Charge Pumps and Fractional Compensation Currents (see Figure 6)

The main charge pumps on pins PHP and PHI are driven by the main phase detector and the charge pump current values are determined by the current at pin R<sub>SET</sub> in conjunction with bits CP0, CP1 in the B-word (see table of charge pump ratios). The fractional compensation is derived from the current at R<sub>SET</sub>, the contents of the fractional accumulator FRD and by the program value of the FDAC. The timing for the fractional compensation is derived from the main divider. The main charge pumps will enter speed up mode after the A-word is set and strobe goes High. When strobe goes Low, charge pump will exit speed up mode.

## Principle of Fractional Compensation

The fractional compensation is designed into the circuit as a means of reducing or eliminating fractional spurs that are caused by the fractional phase ripple of the main divider. If I<sub>COMP</sub> is the compensation current and I<sub>PUMP</sub> is the pump current, then for each charge pump:

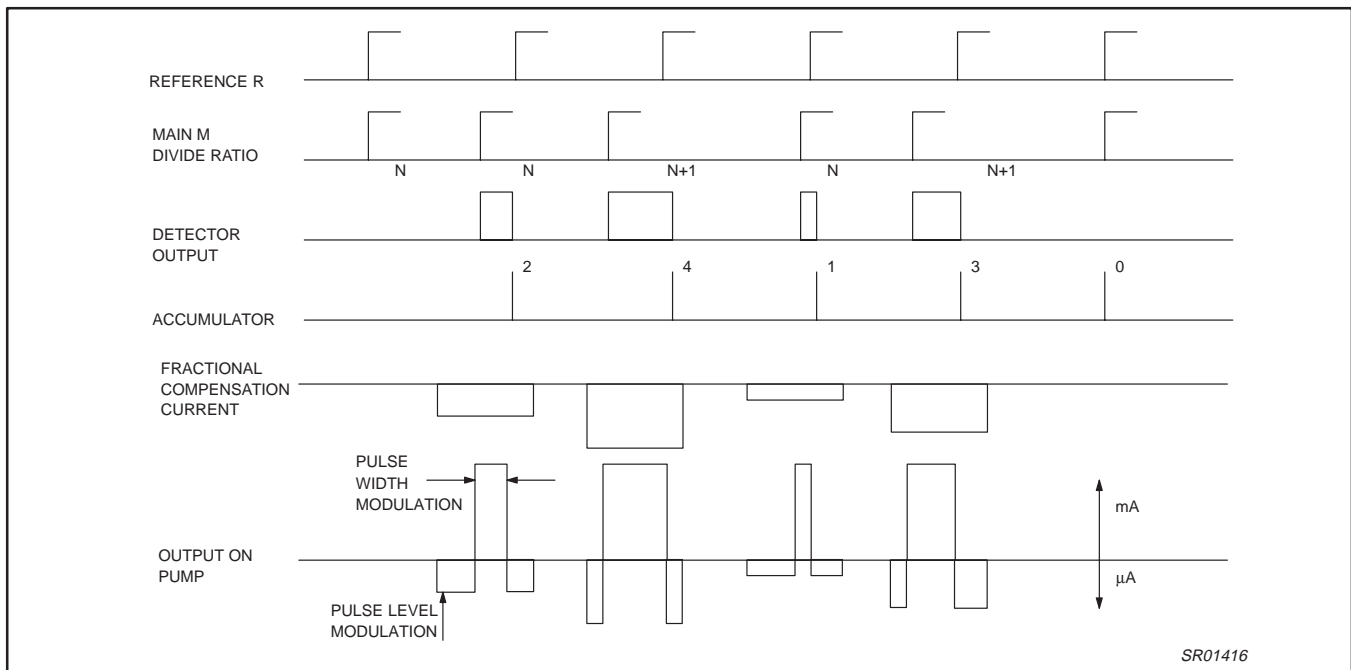
The compensation is done by sourcing a small current, I<sub>COMP</sub>, see Figure 7, that is proportional to the fractional error phase. For proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the fractional charge pump ripple. The width of the fractional compensation pulse is fixed to 128 VCO cycles, the amplitude is proportional to the fractional accumulator value and is adjusted by FDAC values (bits FC7–0 in the B-word). The fractional compensation current is derived from the main charge pump in that it follows all the current scaling through external resistor setting, R<sub>SET</sub>, programming or speed-up operation. For a given charge pump,

$$I_{COMP} = (I_{PUMP} / 128) * (FDAC / 5 * 128) * FRD$$

FRD is the fractional accumulator value.

The target values for FDAC are: 128 for F<sub>MOD</sub> = 1 (modulo 5) and 80 for F<sub>MOD</sub> = 0 (modulo 8).

$$I_{PUMP\_TOTAL} = I_{PUMP} + I_{COMP}$$



NOTE: For a proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output.

Figure 6. Waveforms for NF = 2 Modulo 5 → fraction = 2/5

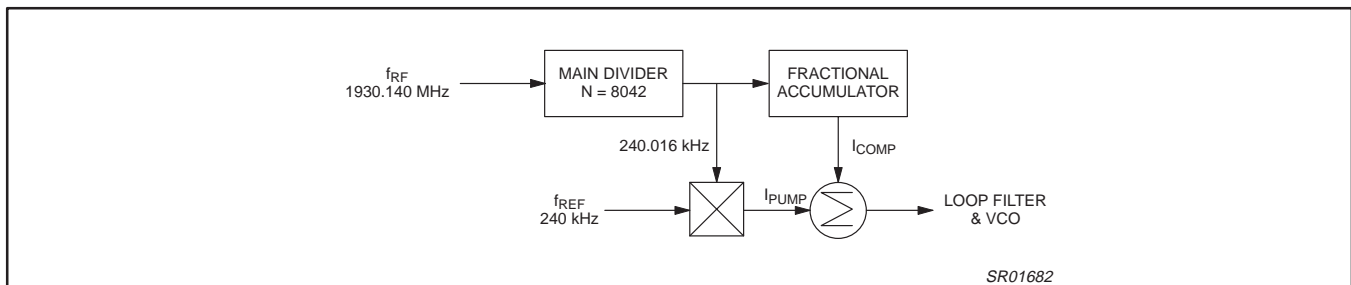


Figure 7. Current Injection Concept

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**Charge pump currents**

CP0	I <sub>PHP</sub>	I <sub>PHP-SU</sub>
0	3xI <sub>SET</sub>	15xI <sub>SET</sub>
1	1xI <sub>SET</sub>	5xI <sub>SET</sub>

**NOTES:**

1.  $I_{SET} = V_{SET} / R_{SET}$  bias current for charge pumps.
2. I<sub>PHP-SU</sub> is the total current at pin PHP during speed up condition.

**Lock Detect**

The output LOCK maintains a logic '1' when the auxiliary phase detector ANDed with the main phase detector indicates a lock condition. The lock condition for the main and auxiliary synthesizers is defined as a phase difference of less than  $\pm 1$  period of the frequency at the input REFin+, -. One counter can fulfill the lock condition when the other counter is powered down. Out of lock (logic '0') is indicated when both counters are powered down.

**Power-down mode**

The power-down signal can be either hardware (PON) or software (PD). The PON signal is exclusively ORed with the PD bits in B-word. If PON = 0, then the part is powered up when PD = 1. PON can be used to invert the polarity of the software bit PD. When the synthesizer is reactivated after power-down, the main and reference dividers are synchronized to avoid possibility of random phase errors on power-up.

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### Serial programming bus

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program all counter divide ratios, fractional compensation DAC, selection and enable bits. The programming data is structured into 24 bit words; each word includes 2 or 3 address bits. Figure 8 shows the timing diagram of the serial input. When the STROBE goes active HIGH, the clock is disabled and the data in the shift register remains unchanged. Depending on the address bits, the

data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 2 words must be sent: B, and A. Table 1 shows the format and the contents of each word. The D word is normally used for testing purposes. When sending the B-word, data bits FC7-0 for the fractional compensation DAC are not loaded immediately. Instead they are stored in temporary registers. Only when the A-word is loaded, these temporary registers are loaded together with the main divider ratio.

### Serial bus timing characteristics. See Figure 8.

$V_{DD} = V_{DDCP} = +3.0V$ ;  $T_A = +25^\circ C$  unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
<b>Serial programming clock; CLK</b>					
$t_r$	Input rise time	–	10	40	ns
$t_f$	Input fall time	–	10	40	ns
$T_{cy}$	Clock period	100	–	–	ns
<b>Enable programming; STROBE</b>					
$t_{START}$	Delay to rising clock edge	40	–	–	ns
$t_w$	Minimum inactive pulse width	$1/f_{COMP}$	–	–	ns
$t_{SU;\bar{E}}$	Enable set-up time to next clock edge	20	–	–	ns
<b>Register serial input data; DATA</b>					
$t_{SU;DAT}$	Input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	Input data to clock hold time	20	–	–	ns

### Application information

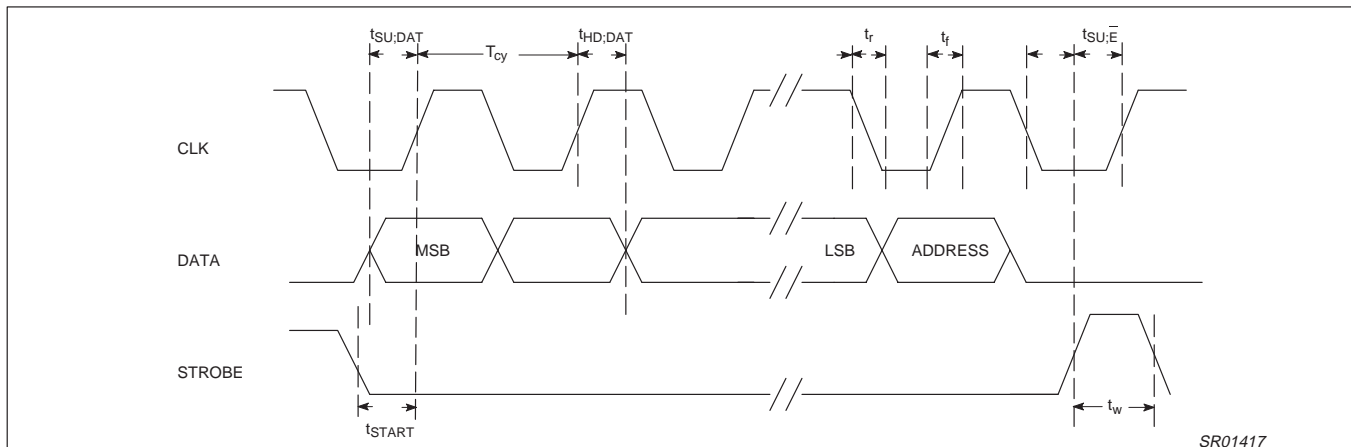


Figure 8. Serial Bus Timing Diagram

SR01417

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## Data format

**Table 1. Format of programmed data**

LAST IN				MSB		SERIAL PROGRAMMING FORMAT						FIRST IN LSB	
p23		p22		p21		p20	../..	../..			p1		p0

**Table 2. A word, length 24 bits**

LAST IN																						LSB		FIRST IN	
Address		fmod		Fractional-N				Main Divider ratio																Spare	
0	0	FM	NF2	NF1	NF0	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	SP1	SP2		
Default:	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0		
A word select				Fixed to 00.																					
Fractional Modulus select				FM 0 = modulo 8, 1 = modulo 5.																					
Fractional-N Increment				NF2..0 Fractional N Increment values 000 to 111.																					
N-Divider				N0..N15, Main divider values 512 to 65535 allowed for divider ratio.																					

**Table 3. B word, length 24 bits**

Address		REFERENCE DIVIDER										LOCK	PD	CP	FRACTIONAL COMPENSATION DAC								SPARE
0	1	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	LO	MAIN	CP0	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	SP3
Default:	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0
B word select		Fixed to 01																					
R-Divider		R0..R9, Reference divider values 4 to 1023 allowed for divider ration.																					
Charge pump current Ratio		CP0: Charge pump current ratio, see table of charge pump currents.																					
Lock detect output		L0 0 Main lock detect signal present at the LOCK pin (push/pull). 1 Main lock detect signal present at the LOCK pin (open drain). When main loop is in power down mode, the lock indicator is low.																					
Power down		Main = 1: power to main divider, reference divider, main charge pumps, Main = 0 to power down.																					
Fractional Compensation		FC7..0 Fractional Compensation charge pump current DAC, values 0 to 255.																					

**Table 4. D word, length 24 bits**

Address			SYNTHESIZER TEST BITS				SYNTHESIZER TEST BITS																
1	1	0	-	-	-	-	-	Tspu	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Tspu: Speed up = 1			Forces the main charge pumps in speed-up mode all the time. <b>NOTE:</b> All test bits must be set to 0 for normal operation.																				

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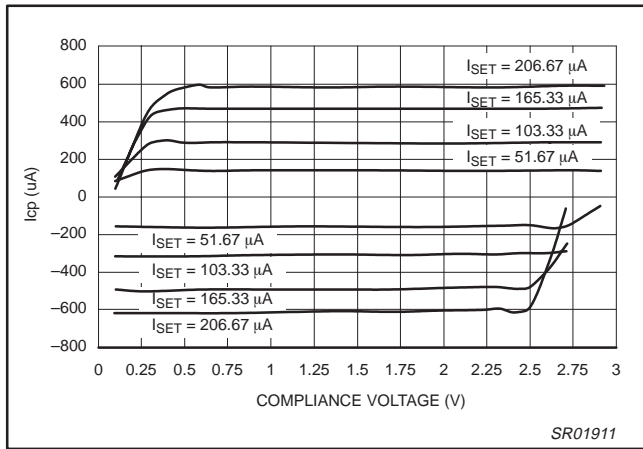


Figure 9. Php Charge Pump Output vs. ISET (CP = 0, TEMP = 25°C)

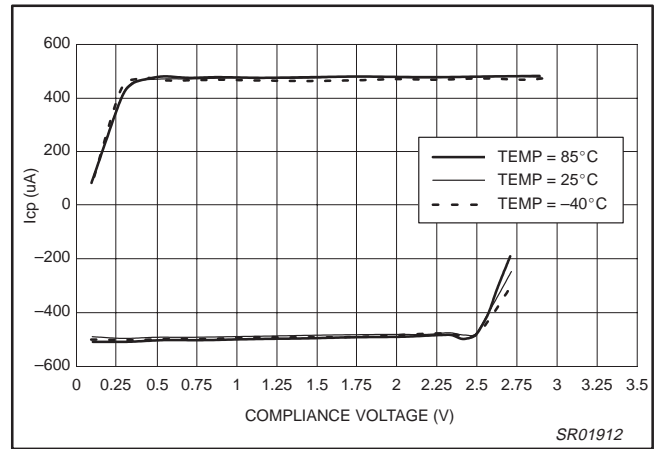


Figure 10. Php Charge Pump Output vs. Temperature (CP = 0; VDD = 3.0 V; ISET = 165.33 uA)

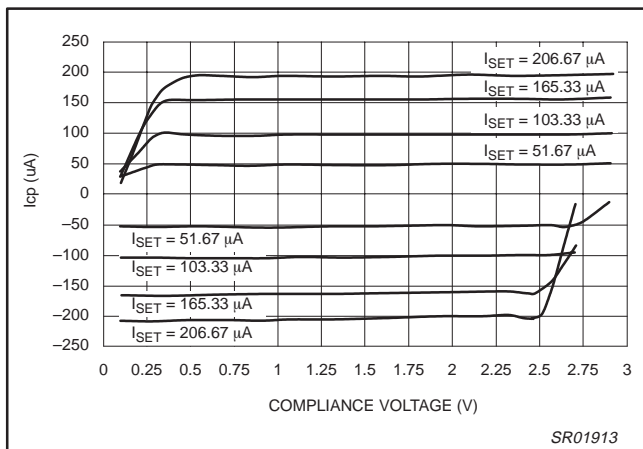


Figure 11. Php Charge Pump Output vs. ISET (CP = 1; TEMP = 25°C)

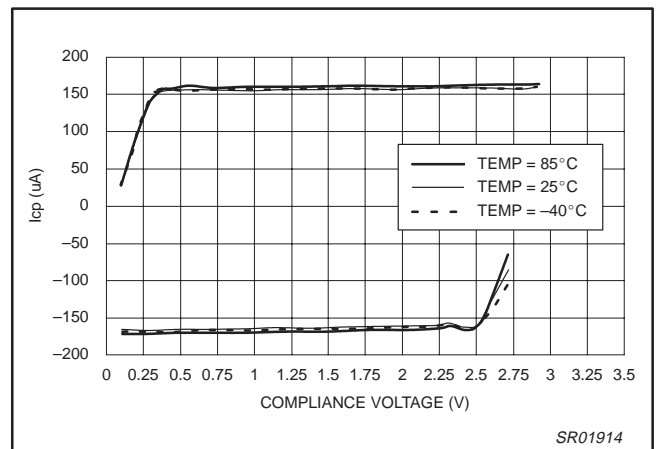


Figure 12. Php Charge Pump Output vs. Temperature (CP = 1; VDD = 3.0 V; ISET = 165.33 uA)

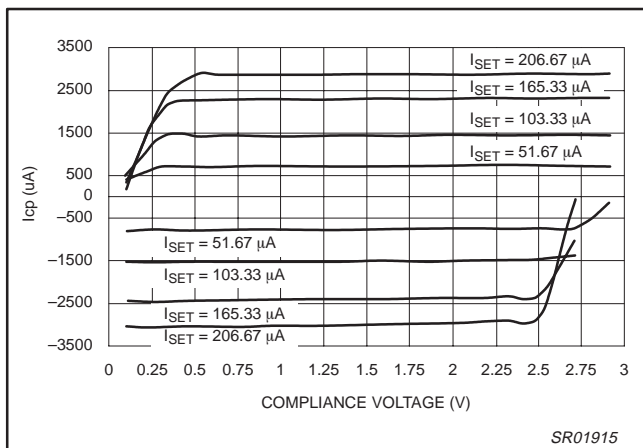


Figure 13. Php-su Charge Pump Output vs. ISET (CP = 0; TEMP = 25°C)

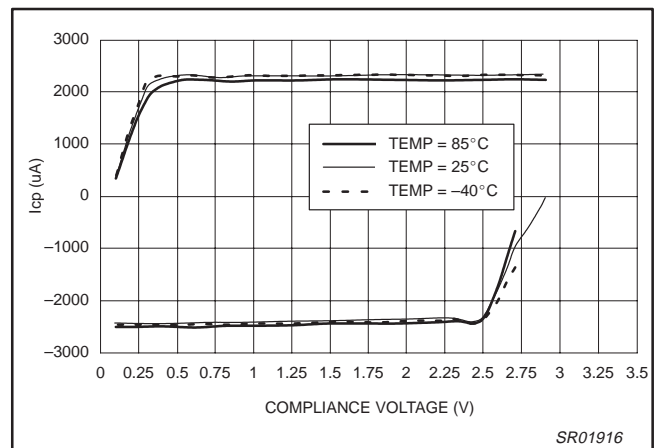
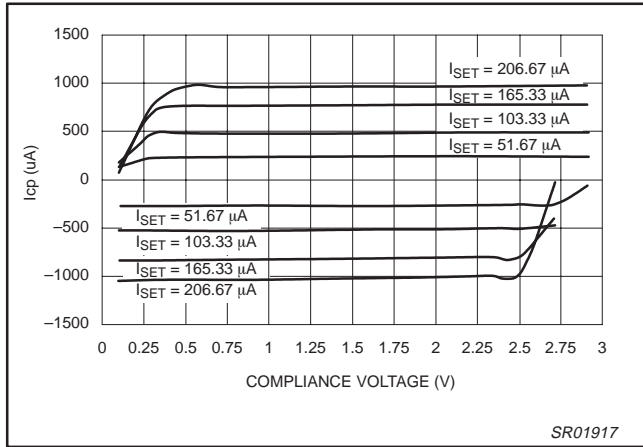


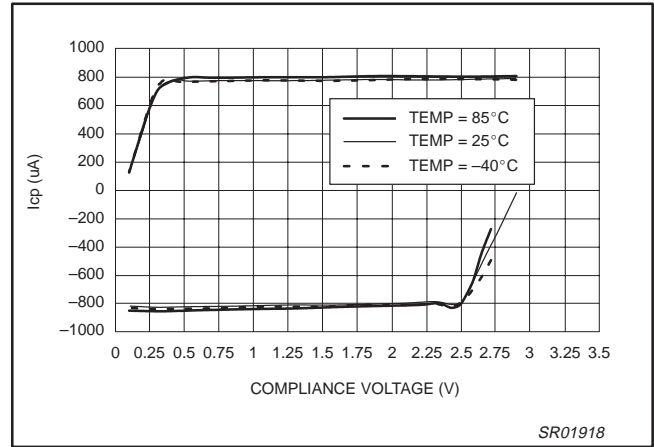
Figure 14. Php-su Charge Pump Output vs. Temperature (CP = 0; VDD = 3.0 V; ISET = 165.33 uA)

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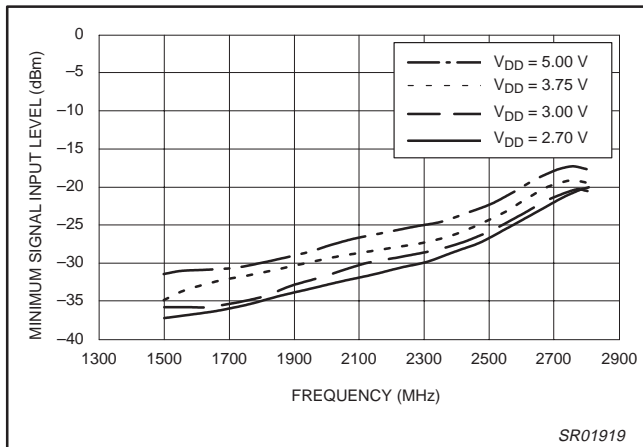
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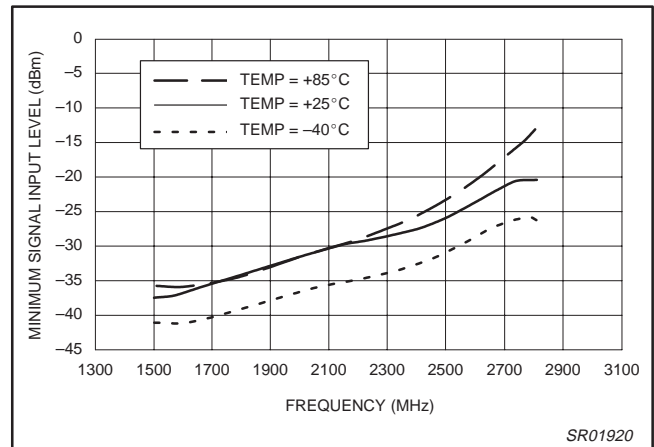
**Figure 15. Php-su Charge Pump Output vs. ISET (CP = 1; TEMP = 25°C)**



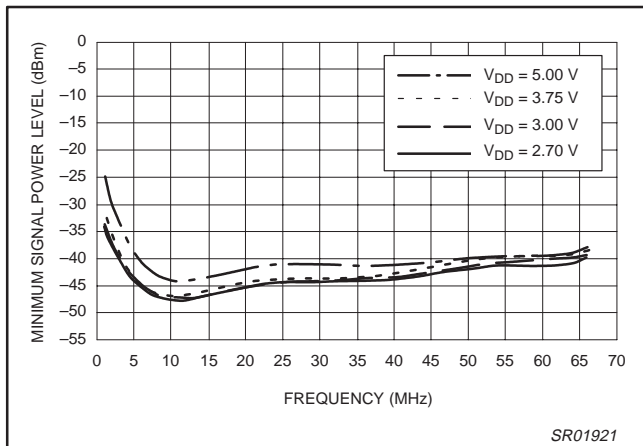
**Figure 16. Php-su Charge Pump Output vs. Temperature (CP = 1; VDD = 3.0 V; ISET = 165.33 uA)**



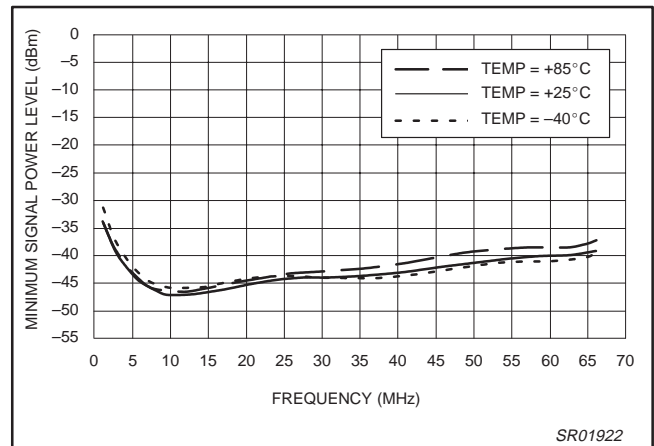
**Figure 17. Main Divider Input Sensitivity vs. Frequency and Supply Voltage (TEMP = 25°C)**



**Figure 18. Main Divider Input Sensitivity vs. Frequency and Temperature (VDD = 3.00 V)**



**Figure 19. Reference Divider Input Sensitivity vs. Frequency and Supply Voltage (TEMP = 25°C)**



**Figure 20. Reference Divider Input Sensitivity vs. Frequency and Temperature (VDD = 3.00 V)**

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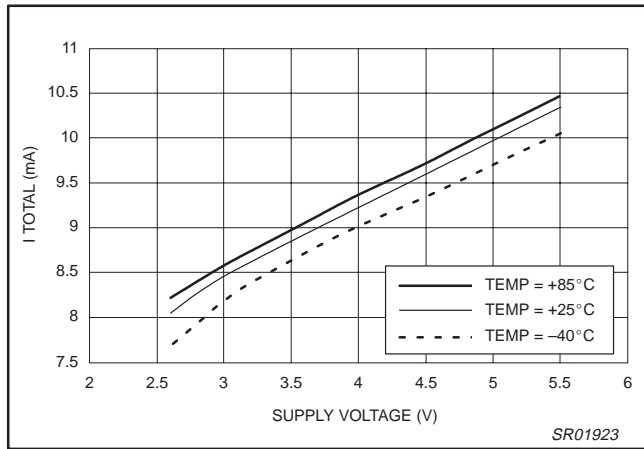


Figure 21. Current Supply Over V<sub>DD</sub>

# 2.5GHz low voltage fractional-N frequency synthesizer

SA8016

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	$\theta$
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				94-07-12 95-04-04



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2.5GHz low voltage fractional-N frequency synthesizer

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SA8016

**NOTES**

# 2.5GHz low voltage fractional-N frequency synthesizer

SA8016

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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