DATA SHEET

SA8028
2.5 GHz sigma delta fractional-N / 760 MHz IF integer frequency synthesizers

Product data
Supersedes data of 2002 Jan 09
File under Integrated Circuits — IC17

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Philips
Semiconductors

PHILIPS

GENERAL DESCRIPTION

The SA8028 BICMOS device integrates programmable dividers, charge pumps and phase comparators to implement phase–locked loops. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at VCO input frequencies up to 2.5 GHz. The synthesizer has fully programmable RF, IF, and reference dividers. All divider ratios are supplied via a 3-wire serial programming bus. The RF divider is a fractional-N divider with programmable integer ratios from 33 to 509 and a fractional resolution of 22 programmable bits (23 bits internal). A 2^{nd} order sigma-delta modulator is used to achieve fractional division.

Separate power and ground pins are provided to the charge pumps and digital circuits. V_{DDCP} must be equal to or greater than V_{DD}. The ground pins should be externally connected to prevent large currents from flowing across the die and thus causing damage.

The charge pump current (gain) is fully programmable, while I_{SET} is set by an external resistance at the R_{SET} pin (refer to section 1.5, RF and IF Charge Pumps). The phase/frequency detector charge pump outputs allow for implementing a passive loop filter.

FEATURES

- Extremely low phase noise:
  $L_{(f)}$ = –101 dBc/Hz at 5 kHz offset at 800 MHz
- Low power
- Programmable Normal & Integral charge pump outputs:
  Maximum output = 10.4 mA
- Digital fractional spurious compensation
- Hardware and software power-down
- $I_{DDsleep}$ < 0.1 µA (typ) at V_{DD} = 3.0 V
- Seperate supply for V_{DD} and V_{DDCP}
- Programmable loop filter bandwidth

APPLICATIONS

- 500 to 2500 MHz wireless equipment
- Cellular phones, all standards including:
  CDMA : IS95-B,C WCDMA
  3G : WCDMA / UMTS
  GSM : EDGE / GPRS
  TDMA : IS136 and EDGE
  GAIT : GSM and TDMA
- WLAN
- Wireless PDAs
- Satellite tuners and all other high frequency equipment
- Extreme fine frequency resolution applications

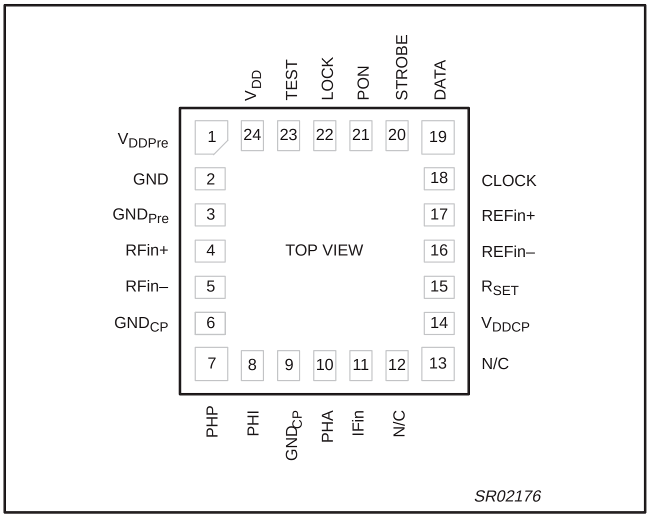


Figure 1. HBCC24 pin configuration.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA8028W	HBCC24	Plastic, heatsink bottom chip carrier; 24 terminals; body 4 x 4 x 0.65 mm (CSP package)	SOT564-1

QUICK REFERENCE DATA

$V_{DDCP} = V_{DD} = V_{DDpre} = +3.0$ V, $T_{amb} = +25°C$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}, V_{DDpre}	Digital supply voltage	$V_{DD} = V_{DDpre}$	2.7	–	3.6	V
V_{DDCP}	Charge pump supply voltage	$V_{DDCP} \geq V_{DD}$, V_{DDpre}	2.7	–	3.6	V
$I_{DDtotal}$	Total supply current	RF and IF. on	–	7.6	–	mA
$I_{DDsleep}$	Total supply current in power-down mode		–	0.1	1	μA
f_{RFin}	VCO Input frequency range		500	–	2500	MHz
f_{IFin}	Input frequency range		100	–	760	MHz
f_{REFin}	Crystal reference input frequency		5	–	30	MHz
$f_{COMPMAX}$	Maximum phase comparator frequency	RF phase comparator; max. limit is indicative	–	–	30	MHz
T_{amb}	Operating ambient temperature		–40	–	+85	°C

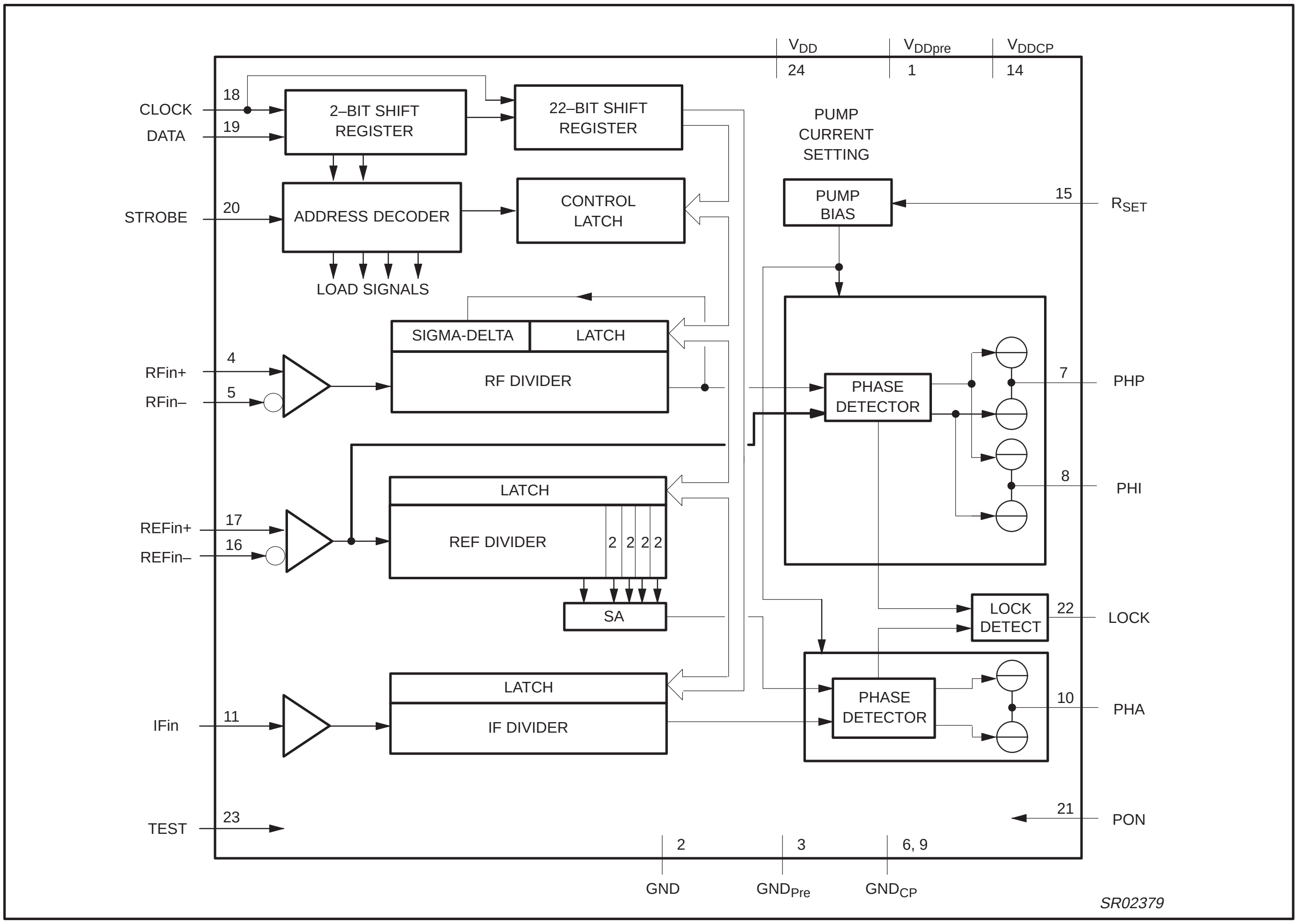


Figure 2. HBCC24 Block Diagram

HBCC24 PIN DESCRIPTION

SYMBOL	PIN	DESCRIPTION
V_{DDpre}	1	Prescaler supply voltage
GND	2	Ground; digital
GND_{Pre}	3	Prescaler ground; analog
RFin+	4	Input to RF divider (+)
RFin–	5	Input to RF divider (–)
GND_{CP}	6	Charge pump ground; analog
PHP	7	RF normal charge pump output
PHI	8	RF integral charge pump output
GND_{CP}	9	Charge pump ground; analog
PHA	10	IF charge pump output
IFin	11	Input to IF divider
N/C	12	Not connected

SYMBOL	PIN	DESCRIPTION
N/C	13	Not connected
V_{DDCP}	14	Charge pump supply voltage; analog
R_{SET}	15	External resistor from this pin to ground sets the charge pump current
REFin–	16	Input to reference (–)
REFin+	17	Input to reference (+)
CLOCK	18	Programming bus clock input
DATA	19	Programming bus data input
STROBE	20	Programming bus enable input
PON	21	Power-down control input
LOCK	22	Lock detect output
TEST	23	Test (should be either grounded or connected to V_{DD})
V_{DD}	24	Supply; digital

LIMITING VALUES

In accordance with the Absolute Maximum Rating System

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Digital supply voltage	–0.3	+3.6	V
V_{DDCP}	Charge pump supply voltage	–0.3	+3.6	V
V_{DDpre}	Analog supply voltage	–0.3	+3.6	V
ΔV_{DD}	Difference in supply voltages $V_{DDCP} - V_{DDpre}$ ($V_{DDCP} \geq V_{DDpre}$, V_{DD})	–0.3	+0.9	V
V_n	All input pins	–0.3	V_{DD} + 0.3	V
ΔV_{GND}	Difference in voltage between GND_{pre}, GND_{CP} and GND (these pins should be connected together)	–0.3	+0.3	V
T_{stg}	Storage temperature	–55	+125	°C
T_{amb}	Operating ambient temperature	–40	+85	°C
T_j	Maximum junction temperature		150	°C

Handling

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	HBCC24: Thermal resistance from junction to ambient in still air	30	°C/W

CHARACTERISTICS

$V_{DDCP} = V_{DD} = V_{DDpre} = +3.0$ V, $T_{amb} = +25$°C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}, V_{DDpre}	Digital supply voltage, prescaler supply voltage	$V_{DD} = V_{DDpre}$	2.7	–	3.6	V
V_{DDCP}	Charge pump supply voltage	$V_{DDCP} \geq V_{DD}, V_{DDpre}$	2.7	–	3.6	V
$I_{DDTotal}$	Synthesizer operational total supply current	f_{REF} = 20 MHz (with RF on, IF on)	–	7.6	–	mA
		(with RF on, IF off)	–	6.4	–	mA
$I_{DDsleep}$	Total supply current in power-down mode	logic levels 0 or V_{DD}	–	0.1	1	μA
RF divider input						
f_{RFin}	RF VCO input frequency range		500	–	2500	MHz
V_{RFin}	AC-coupled input signal level	R_{in} (external) = R_S = 50 Ω; single-ended drive; max. limit is indicative @ 500 to 2500 MHz	–15	–	0	dBm
			112	–	632	mV_{pp}
Z_{RFin}	Input impedance Re (Z)	f_{RFin} = 2.4 GHz	–	300	–	Ω
C_{RFin}	Typical pin input capacitance	f_{RFin} = 2.4 GHz	–	1	–	pF
N_{RF}	RF divider ratio ranges	Limited test coverage	33	–	509	
$F_{COMPmax}$	Maximum phase comparator frequency	RF phase comparator	–	–	30	MHz
IF divider input						
f_{IFin}	Input frequency range		100	–	760	MHz
V_{IFin}	AC-coupled input signal level	f_{IFin}: 100 MHz to 500 MHz	–15	–	0	dBm
		R_{in} (external) = R_S = 50 Ω; max. limit is indicative	112	–	632	mV_{pp}
		f_{IFin}: 500 MHz to 760 MHz	–10	–	0	dBm
		R_{in} (external) = R_S = 50 Ω; max. limit is indicative	200	–	632	mV_{pp}
Z_{Fin}	Input impedance Re (Z)	f_{RFin} = 500 MHz	–	3.9	–	kΩ
C_{Fin}	Typical pin input capacitance	f_{RFin} = 500 MHz	–	0.5	–	pF
N_{IF}	IF division ratio		128	–	16383	
Reference divider input						
f_{REFin}	Input frequency range from TCXO		5	–	30	MHz
V_{REFin}	AC-coupled input signal level	single-ended drive; max. limit is indicative	360	–	1300	mV_{PP}
Z_{REFin}	Input impedance Re (Z)	f_{REF} = 20 MHz	–	10	–	kΩ
C_{REFin}	Typical pin input capacitance	f_{REF} = 20 MHz	–	1	–	pF
R_{REF}	Reference division ratio	SA = ”000”, IF loop	4	–	1023	
Charge pump current setting resistor input						
R_{SET}	External resistor from pin to ground		6	7.5	15	kΩ
V_{SET}	Regulated voltage at pin	R_{SET} = 7.5 kΩ	–	1.22	–	V
Charge pump outputs; R_{SET} = 7.5 kΩ						
I_{CP}	Charge pump current ratio to I_{SET}[1]	Current gain = I_{PH}/I_{SET}	–15	–	+15	%
I_{MATCH}	Sink-to-source current matching	V_{PH} = 1/2 V_{DDCP}	–10	–	+10	%
I_{ZOUT}	Output current variation versus V_{PH}[2]	V_{PH} in compliance range	–10	–	+10	%
I_{LPH}	Charge pump off leakage current	V_{PH} = 1/2 V_{DDCP}	–10	–	+10	nA
V_{PH}	Charge pump voltage compliance		0.6	–	V_{DDCP}–0.7	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Phase noise (condition R_{SET} = 7.5 kΩ, CP = 00, non speed-up mode)						
$L_{(f)}$	Synthesizer's contribution to close-in phase noise of 900 MHz RF signal at 5 kHz offset.	f_{REF} = 13 MHz, TCXO, f_{COMP} = 13 MHz indicative, not tested	–	–99	–	dBc/Hz
	Synthesizer's contribution to close-in phase noise of 1800 MHz RF signal at 5 kHz offset.	As above	–	–93	–	dBc/Hz
	Synthesizer's contribution to close-in phase noise of 800 MHz RF signal at 5 kHz offset.	f_{REF} = 19.44/19.68 MHz, TCXO, f_{COMP} = 19.44/19.68 MHz indicative, not tested	–	–101	–	dBc/Hz
	Synthesizer's contribution to close-in phase noise of 2100 MHz RF signal at 5 kHz offset.	As above	–	–93	–	dBc/Hz
Interface logic input signal levels						
V_{IH}	HIGH level input voltage		0.7*V_{DD}	–	V_{DD}+0.3	V
V_{IL}	LOW level input voltage		–0.3	–	0.3*V_{DD}	V
I_{LEAK}	Input leakage current	V_{DD} = 3 V, V_{IH} = 3 V, V_{IL} = 0 V	–0.5	–	+0.5	μA
Lock detect output signal (in push/pull mode) and Data output signal (in readout test mode)						
V_{OL}	LOW level output voltage	I_{sink} = 2 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{source} = –2 mA	V_{DD}–0.4	–	–	V

NOTES:

1. $I_{SET} = \frac{V_{SET}}{R_{SET}}$ bias current for charge pumps.
2. The relative output current variation is defined as:

$$\frac{\Delta I_{ZOUT}}{I_{ZOUT}} = 2 \times \frac{(I_2 - I_1)}{|I_2 + I_1|};$$

With I_1 @ V_1 = 0.6 V, I_2 @V_2 = V_{DDCP} – 0.7 V (see Figure 3).

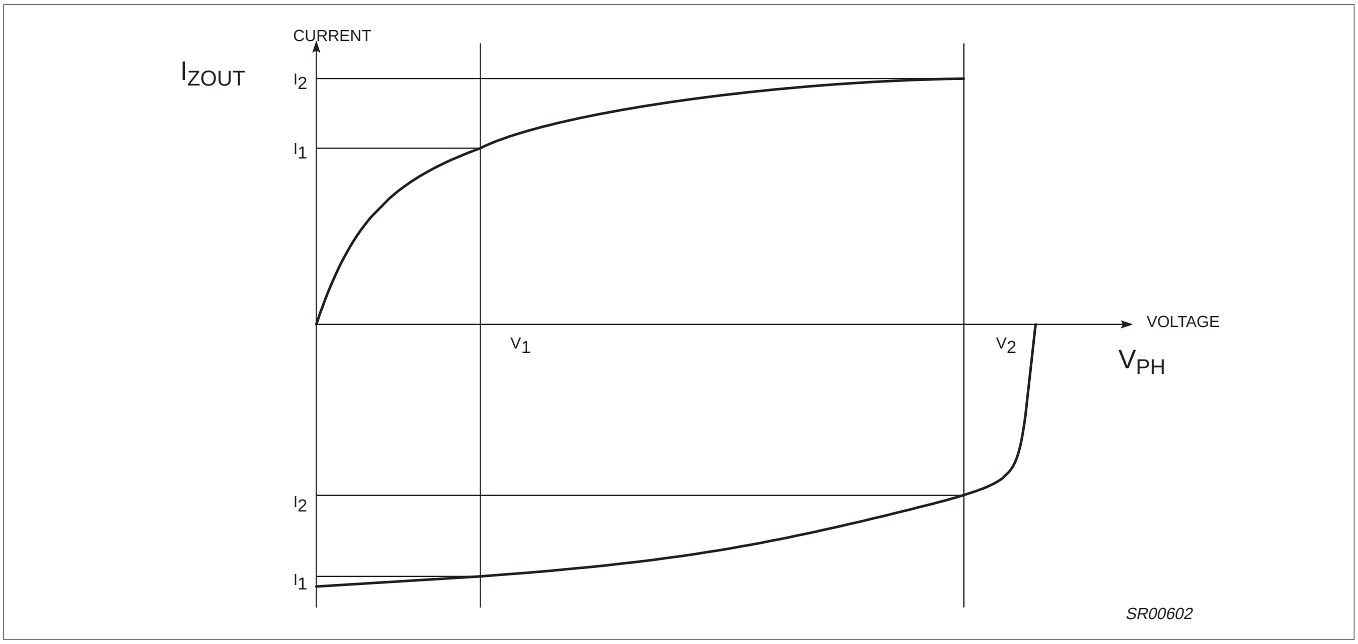


Figure 3. Relative output current variation.

1.0 FUNCTIONAL DESCRIPTION

Frequency synthesizers, such as Philips Semiconductors' SA8028, are a crucial part of Phase Locked Loops (PLL) for both voice and data devices used in communications. Five components make up the basic PLL (see Figure 4). A very stable, low frequency, signal source (typically a temperature controlled crystal oscillator TCXO_) is used as a reference to the system. A second signal source (typically a VCO) is used to generate the desired output frequency. A phase/frequency detector (PFD) is used to compare the phase/frequency error between the two signals. A loop filter (LPF) rejects undesired noise while also integrating the PFD output current to drive the VCO with the necessary tuning voltage, and a divider in the feedback path is used to down-convert the VCO output frequency to the reference frequency for comparison. The SA8028 is a dual synthesizer that integrates programmable dividers, programmable charge pumps and phase comparators to be implemented as part of RF and IF PLLs. The RF synthesizer operates at VCO input frequencies up to 2.5 GHz, while the IF synthesizer operates at VCO input frequencies up to 760 MHz.

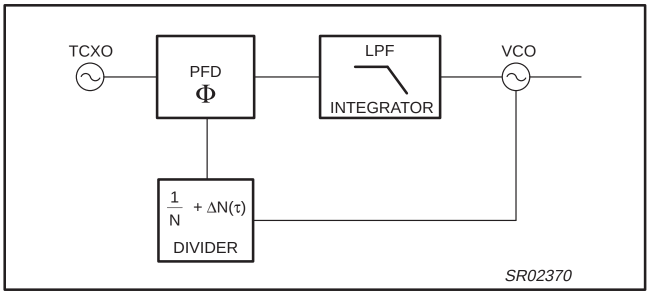


Figure 4. PLL block diagram.

1.1 RF Fractional-N divider

The RFin inputs drive a pre-amplifier to provide the clock to the first divider stage. For single ended operation, the signal should be fed (AC-coupled) to one of the inputs while the other one is AC grounded. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The bipolar divider is fully programmable. For allowable division ratios, see the "characteristics" table.

During each RF divider cycle, one divider output pulse is generated. The positive edge of this pulse drives the phase comparator, the negative edge drives the sigma-delta modulator which is of 2^{nd} order and has an effective resolution of 22 bits. Internally, the modulator works with 23 fractional bits K<22:0>, but the LSB (bit K0) is set to '1' internally to avoid limit cycles (cycles of less than maximum length). This leaves 22 bits (K<22:1>) available for external programming.

Under these conditions (2^{nd} order modulator, 23 fractional bits, K0 = '1'), all possible sigma-delta sequences are $2 \cdot 2^{23}$ divider cycles long, which is the maximum length. The noise shaping characteristic is +20 dB/dec for offset frequencies up to approx. $f_{COMP}/5$, which needs to be cancelled by a closed-loop transfer function of sufficient high order. The output of the sigma-delta modulator is 2 bits, which are added to the integer RF division ratio N, such that the momentary division ratios range from (N–1) to (N+2) in steps of 1.

1.2 IF divider

The IFin input drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The divider consists of a fully programmable bipolar prescaler followed by a CMOS counter. The allowable divide ratios are from 128 to 16383 (C-word bits <21:8>). Table 14 shows all the possible values that can be programmed into the C-Word for the IF divider.

1.3 Reference divider (see Figure 5)

The IF phase detector's reference input is an integer ratio of the reference frequency. The reference divider chain consists of a bipolar input buffer followed by a CMOS divider and a 3-bit binary counter (SA register). The allowable divide ratios, R, are from 4 to 1023 (B-word bits <21:12>) when the 3-bit binary counter (C-word bits <2:0>) is set to all zeros, SA = 000. The 3-bit SA register determines which of the 5 divider outputs (refer to Table 12) is selected as the IF phase detector input (see Figure 5). For the RF synthesizer, the output of the reference input buffer is routed directly (not reference divider) to the input of the RF phase detector.

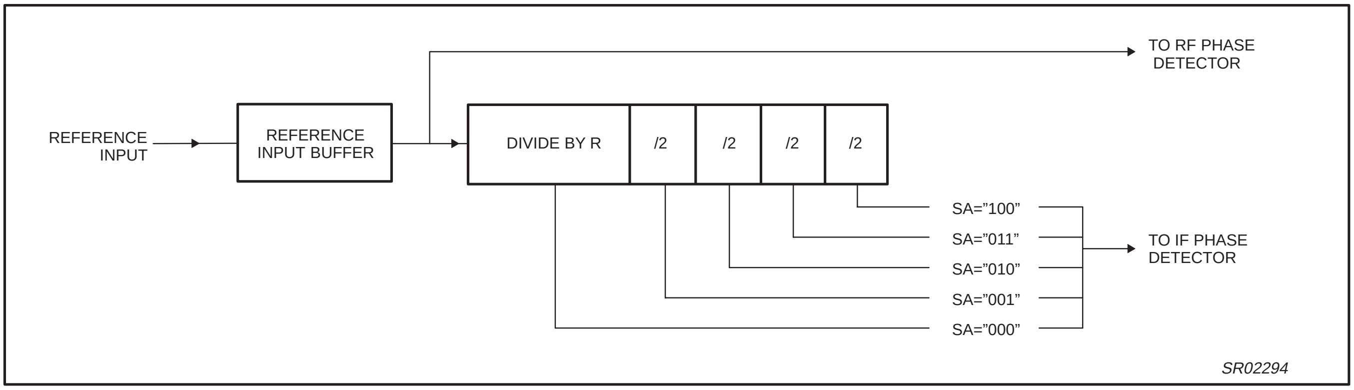
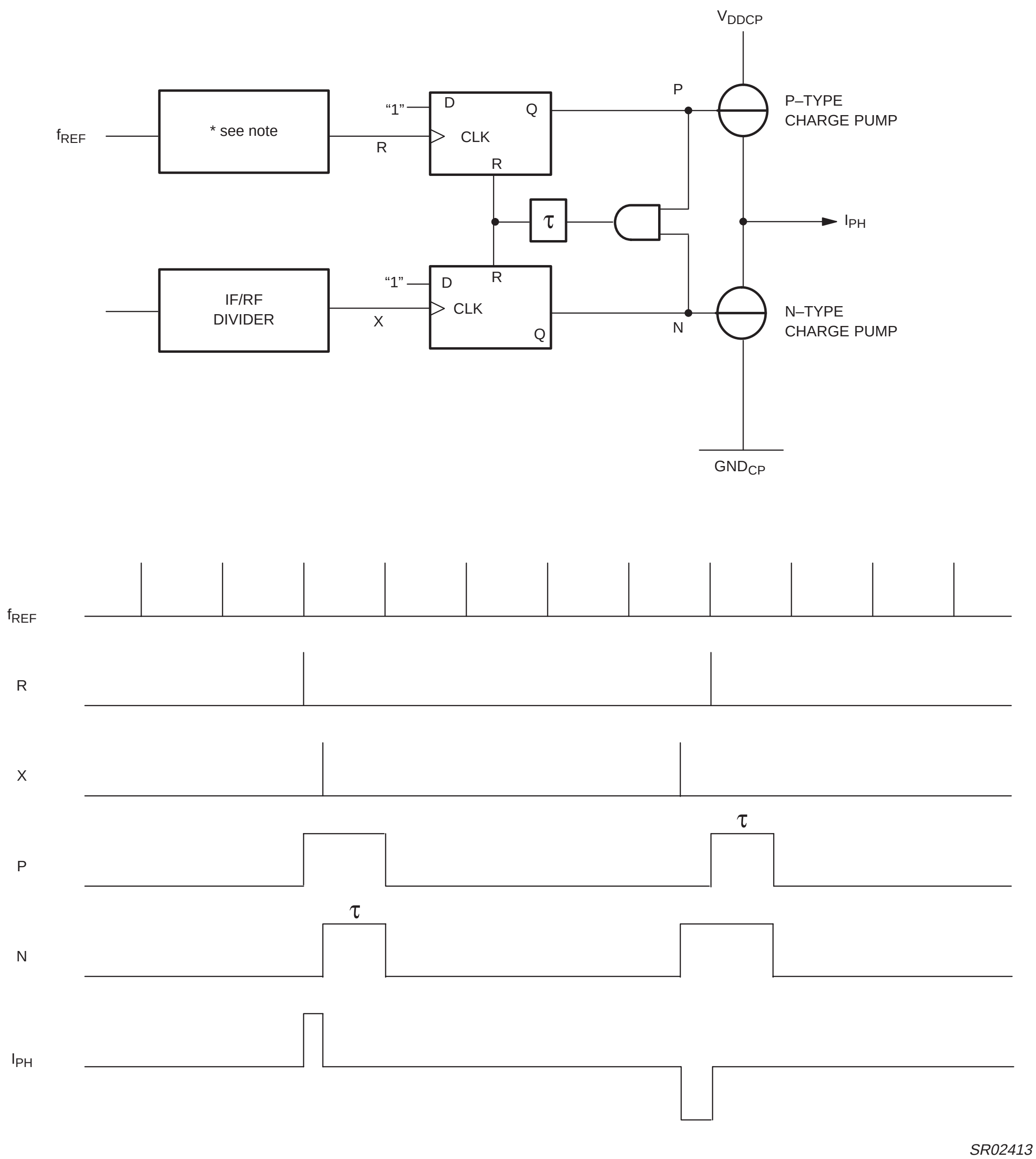


Figure 5. Reference divider.

1.4 Phase detector (see Figure 6)

The reference signal and the RF (IF) divider output are connected to a phase frequency detector that controls the charge pumps. The dead zone (caused by the finite time taken to switch the charge pump current sources on or off) is cancelled by forcing the pumps ON for a minimum time (backlash time, τ) at every cycle providing improved linearity.



NOTES:

For the RF synthesizer, the output of the reference input buffer is routed directly (not divided) to the input of the RF phase detector. Whereas for the IF synthesizer, the reference input to the IF phase detector is the output from the reference divider.

τ (backlash time) is the delay that fixes the minimum allowable charge pump activity time.

Figure 6. Phase detector structure with timing.

1.5 RF and IF Charge Pumps

The RF phase detector drives the charge pumps on the PHP and PHI pins, while the IF phase detector drives the charge pump on the PHA pin. Both the RF and IF charge pump current values are determined by the current generated at the R_{SET} pin[1]. The current gain can be further programmed by the CP0, CP1 bits in the C-word, as seen in Table 1.

Table 1. RF and IF charge pump currents

CP1[2]	CP0	I_{PHA}	I_{PHP}	I_{PHP-SU}[3]	I_{PHI}
0	0	$1.5xI_{SET}$	$3xI_{SET}$	$15xI_{SET}$	$36xI_{SET}$
0	1	$0.5xI_{SET}$	$1xI_{SET}$	$5xI_{SET}$	$12xI_{SET}$
1	0	$1.5xI_{SET}$	$3xI_{SET}$	$15xI_{SET}$	0
1	1	$0.5xI_{SET}$	$1xI_{SET}$	$5xI_{SET}$	0

NOTES
1. $I_{SET} = V_{SET}/R_{SET}$: bias current for charge pumps.
2. CP1 = 1 is used to disable the PHI pump.
3. I_{PHP-SU} is the total current at pin PHP during speed up condition.

1.6 Charge Pumps Speed-up Mode

The RF charge pumps will enter speed-up mode when STROBE goes high after A-word has been sent. They will exit speed-up mode on the next falling edge of STROBE. There is no speed-up mode for the IF charge pump.

The charge pump, by default, will automatically go into speed-up mode (which can deliver up to $15*I_{SET}$ for PHP_SU, and $36*I_{SET}$ for PHI), based on the strobe pulse width following the A-word to reduce switching speed for large tuning voltage steps (i.e., large frequency steps). Figure 7 shows the recommended passive loop filter configuration. Note: This charge pump architecture eliminates the need for added active switches and reduces external component count. Furthermore, the programmable charge pump gains provide some programmability to the loop filter bandwidth.

The duration of speed-up mode is determined by the strobe pulse that follows the A-word. Recommended optimal strobe width is equal to the total loop filter capacitance charge time from VCO control voltage level 1 to VCO control voltage level 2. The strobe width must not exceed this charge time. An external data processing unit controls the width of the strobe pulse (e.g., × number of clock cycles).

In addition, charge pumps will stay in speed-up mode continuously while Tspu = 1 (in D-word <D15>). The speed-up mode can also be disabled by programming $T_{dis-spu}$ = 1 (in D-word <D16>).

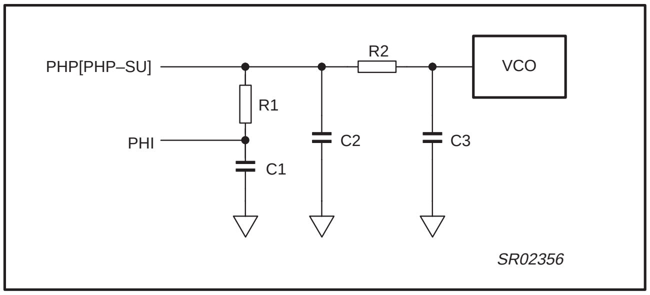


Figure 7. Typical passive 3-pole loop filter.

1.7 Lock Detect

The output LOCK maintains a logic ‘1’ when the IF phase detector (AND/ORed) with the RF phase detector indicates a lock condition. The lock condition for the RF and IF synthesizers is defined as a phase difference of less than ±1 period of the frequency at the input REF_{in+}, REF_{in-}. One counter can fulfill the lock condition when the other counter is powered down. Out of lock (logic ‘0’) is indicated when both counters are powered down.

1.8 Power-down mode

With power applied to the chip, power-down mode can be entered either by hardware (external signal on pin PON) or by software (by programming the PD = Power Down bits (<B10, B9>) in the B-word). The PON signal is exclusively ORed with the PD bits. If PON = 0, then the part is powered up when PD = 1 (<B10, B9>). PON can be used to invert the polarity of the software bits PD. Table 9 of section 2.4.2 illustrates how power-down mode can be implemented.

During power-down mode the 3-wire bus remains active and programming-words may be pre-loaded before switching to power-up mode. If the chip is programmed while in power-down mode, the RF divider ratio N_{RF} is internally presented to the RF divider on the next falling edge of STROBE after STROBE has gone high at the end of the A-word. Power-down mode does not reset the sigma-delta modulator., i.e., power-down mode preserves the state of the sigma-delta modulator (as long as power is applied to the chip).

To take advantage of the register pre-loading capability while the device is in power-down mode, the B-word needs to be sent a second time (i.e., again, after the A-word), with the PD (<B10, B9>) bits now programmed for power-up.

If power-up mode is to be controlled by hardware, the PON signal must be toggled only after the A-word has been sent and STROBE has gone high and then low.

When the synthesizer is reactivated after power-down mode, the IF and reference dividers are synchronized to avoid random phase errors on power-up. There is no power-up synchronization between the RF divider and the reference clock. After power-up, there is a delay of four edges (i.e. 1.5 cycles) of the output clock of the reference divider before the RF phase detector is activated. That means the reference divider must be powered up for the RF phase detector to become active.

When initially applying or reapplying power to the chip, and internal power-up reset pulse is generated which sets the programming-words to their default values and also resets the sigma-delta modulator to its “all-0” state. It is also recommended that the D-word be manually reset to all zeros, following initial power-up, to avoid unknown states.

2.0 SERIAL PROGRAMMING BUS

A simple 3-line bidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLOCK and STROBE. When the STROBE = 0, the clock driver is enabled and on the positive edges of the CLOCK signal, DATA is clocked into temporary shift registers. When the STROBE = 1, the clock is disabled and the data in the shift register is latched into different working registers, depending on the address bits. In order to fully program the circuit, 3 words must be sent in the following order: C, B, and A. An additional word, the D-word, is for test purposes only: all bits in this test word should be initialized to 0 for normal operation. The N value of the B-word is stored temporarily until the A-word is loaded to avoid temporarily false N settings, while the corresponding fractional ratio Kn is not yet active. When a new fractional ratio is loaded through the A-word, the fractional sigma delta modulator is not reset, i.e., it will start the new fractional sequence from the last state of the previously executed sequence. A typical programming sequence is illustrated in Figure 10.

When loading several words in series, the minimum STROBE high time between words must be observed (refer to Figure 8).

Unlike the earlier SA80xx family members, SA8028 has the built-in feature to output the contents of an addressable internal register. For the current SA8028, only the momentary division ratio N (RF divider) can be retrieved through the serial bus. The handshake protocol requires a “request to read” to be sent prior to each “read”, i.e., by sending a D-word with the TreadN-bit (<D11>) set to “high”. Immediately after the transition of “STROBE” from low-to-high, four (4) clock pulses are needed to prepare the data for output and another nine (9) clock pulses are needed to accomplish the serial reading with LSB first. A high-to-low transition of “STROBE” then resets the serial bus to the input mode. The timing diagram is presented in Figure 9. In general, a high-to-low transition of the “STROBE” signal will instantaneously reset the serial bus to the input mode, even when the chip is in the output mode.

Table 2. Serial bus timing requirements (see Figures 8 and 9)

$V_{DD} = V_{DDCP}$ =+3.0 V; T_{amb} = +25 °C unless otherwise specified. (Guaranteed by design.)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	Input rise time	–	10	40	ns
t_f	Input fall time	–	10	40	ns
T_{cy}	Clock period	100	–	–	ns
Enable programming; STROBE					
t_{START}, $t_{START;R}$	Delay to rising clock edge	40	–	–	ns
t_W	Minimum inactive pulse width	$1/f_{COMP}$	–	–	ns
$t_{SU;E}$	Enable set-up time to next clock edge	20	–	–	ns
t_{RESET}	Reset data line to input mode	20	–	–	ns
Register serial input data; DATA (I)					
$t_{SU;DAT}$	Input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	Input data to clock hold time	20	–	–	ns
Register serial output data; DATA (O)					
$t_{SU;DAT;R}$	Input clock to data set-up time	20	–	–	ns

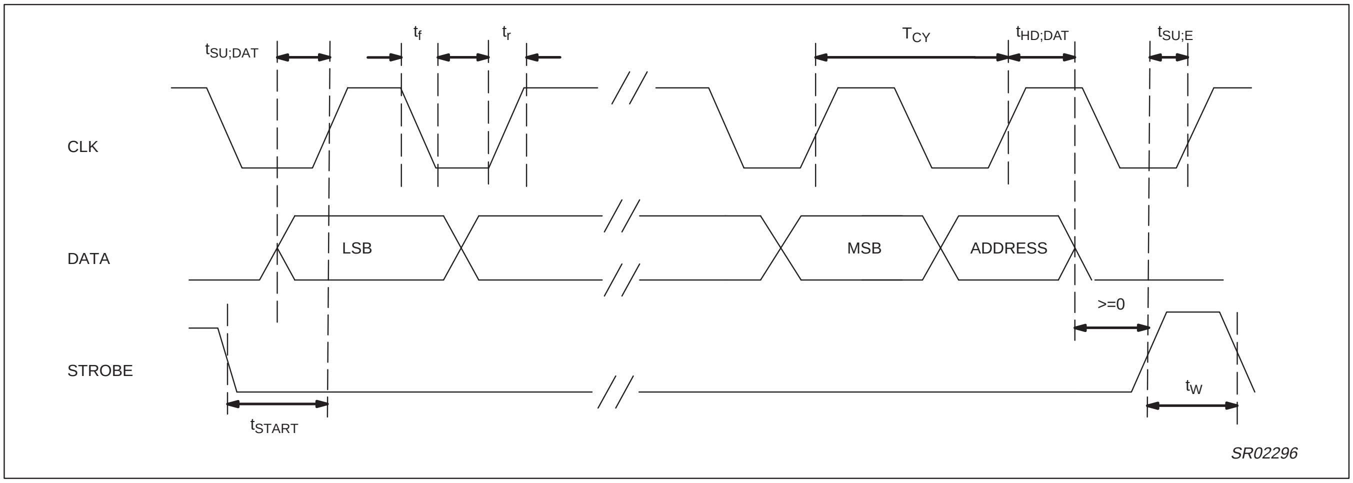


Figure 8. Serial bus “Write” timing diagram.

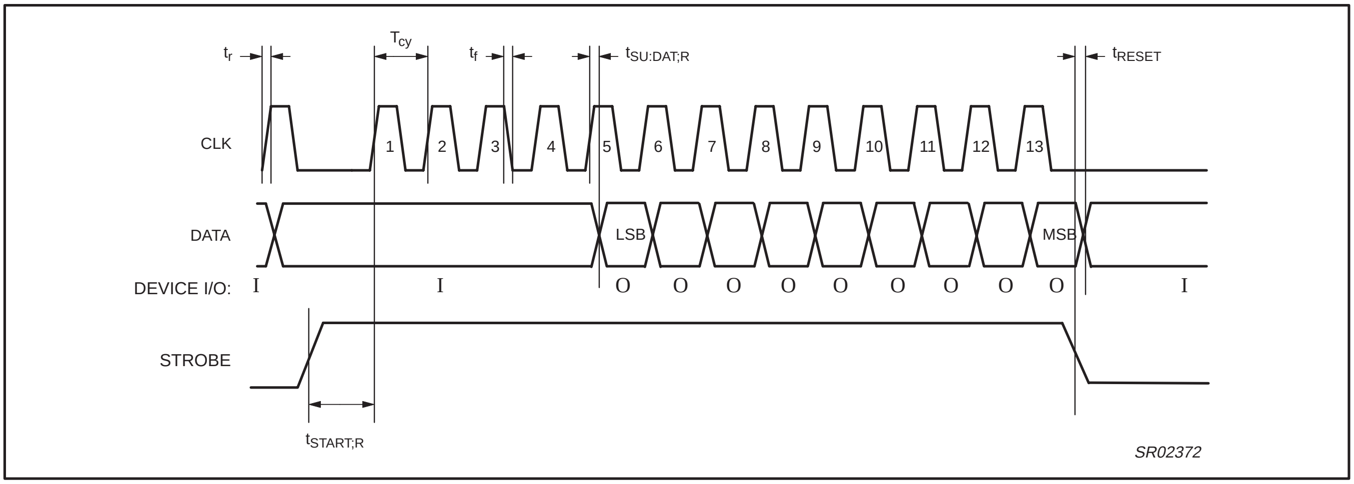


Figure 9. Serial bus “Read” timing diagram.

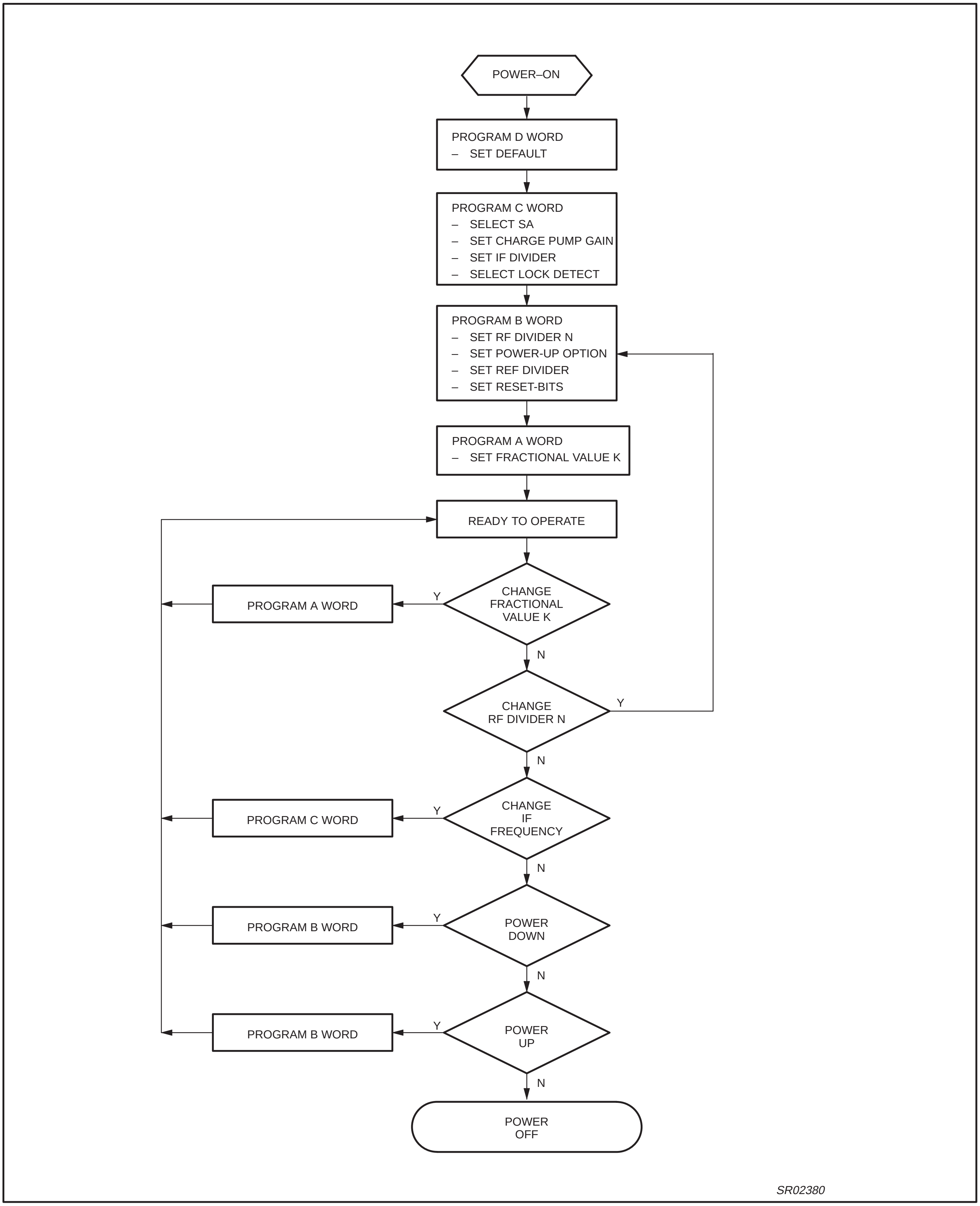


Figure 10. Typical programming sequence

2.1 Data format

Each of the 4 word registers contains 24 programmable bits. Data is serially clocked in on the rising edge of each clock pulse with the LSB first in, and MSB last in.

Table 3. Format of programmed data

LAST IN MSB	SERIAL PROGRAMMING FORMAT						FIRST IN LSB
p23	p22	p21	p20	.. / ..	.. / ..	p1	p0

2.2 Register addressing

Table 4. Register addressing

Bit	<23>	<22>	<21>
A-word address	0	0	x
B-word address	0	1	x
C-word address	1	0	x
D-word address	1	1	0

Notice that the register addresses are the MSB in each word; thus, the last to be clocked into the registers.

2.3 A-word register

Table 5. A-word, length 24 bits

Last IN		<21>	<20>	<19>	<18>	<17>	<16>	<15>	<14>	<13>	<12>	<11>	<10>	<9>	<8>	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
Address		Fractional ratio Kn																					
0	**0**	**K22**	**K21**	**K20**	**K19**	**K18**	**K17**	**K16**	**K15**	**K14**	**K13**	**K12**	**K11**	**K10**	**K9**	**K8**	**K7**	**K6**	**K5**	**K4**	**K3**	**K2**	**K1**
Default :		0	0	0	0	1	1	0	1	0	1	1	0	1	1	1	0	1	0	0	1	1	1
A word address					Fixed to 00.																		
Fractional ratio select					Kn sets the fractional part of the total division ratio. To avoid limit cycles the K0 bit is internally set to “1”																		

2.3.1 The fractional multiplier <A21:A0>

The A-word register is dedicated for programming the RF loop, fractional multiplier (the sigma-delta modulator) which has an effective resolution of 22 bits. The modulator works with 23 bits, Kn<22:0>. However, this K0 bit is set to ‘1’ internally to avoid limit cycles (cycles of less than maximum length). This leaves 22 bits (Kn<22:1>) available for external programming. Refer to Table 6.

Calculating the desired VCO output frequency can be easily accomplished by using the following equation, Equation (1).

$$f_{VCO} = f_{ref}\left(N + \frac{2 \times Kn<22:1> + 1}{2^{23}}\right) \quad (1)$$

where f_{ref} is the reference frequency at the REF input pin and N is the integer multiplier. K_n, once again, is the fractional multiplier.

Example:

Determine the Kn value required for generating a VCO frequency of 2100 MHz with a reference frequency of 19.68 MHz.

$$Kn<22:1> = \frac{\left[\left(\frac{f_{VCO}}{f_{ref}} - N\right) \times 2^{23}\right]}{2}$$

$$Kn<22:1> = \frac{\left[\left(\frac{2100\ MHz}{19.68\ MHz} - 106\right) \times 2^{23}\right]}{2} = 2966702$$

Table 6. Kn values for the fractional divider

⟨A21⟩	⟨A20⟩	⟨A19⟩	⟨A18⟩	⟨A17⟩	⟨A16⟩	⟨A15⟩	⟨A14⟩	⟨A13⟩	⟨A12⟩	⟨A11⟩	⟨A10⟩	⟨A9⟩	⟨A8⟩	⟨A7⟩	⟨A6⟩	⟨A5⟩	⟨A4⟩	⟨A3⟩	⟨A2⟩	⟨A1⟩	⟨A0⟩	Kn
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	4
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	…
1	0	1	1	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	1	1	0	2966702
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	…
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	4194302
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	4194303

2.4 B-word register

Table 7. B-word, length 24 bits

Last IN		<21>	<20>	<19>	<18>	<17>	<16>	<15>	<14>	<13>	<12>	<11>	<10>	<9>	<8>	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
Address		Reference divider ratio Rn										Reset bit	Power Down		RF Divider integer ratio N								
0	**1**	**R9**	**R8**	**R7**	**R6**	**R5**	**R4**	**R3**	**R2**	**R1**	**R0**	**PDref**	**IF**	**RF**	**N8**	**N7**	**N6**	**N5**	**N4**	**N3**	**N2**	**N1**	**N0**
Default:		0	0	0	1	0	1	0	0	0	1	0	1	1	0	0	1	1	0	1	1	0	0
B-word address		Fixed to 01																					
R-Divider		R0..R9, Reference divider values, see section “characteristics” for allowed divider ratios.																					
Reset bit		1 → Pdref : powers down (=resets) the reference divider																					
Power-down		See Truth Table 9																					
N-Divider		Nn sets the integer part of the RF divider ratio, see section “characteristics” for allowed ratios.																					

2.4.1 The RF divider <B8:B0>

Programming the RF divider to obtain the desired VCO output frequency is done by programming the B-word followed by the A-word. The integer divider bits N<8:0> are in the B-word, whereas the fractional divider bits Kn<22:1> are in the A-word. Allowable integer division ratios are shown in Table 8. The N value, from Equation (2), is simply the whole number of times the reference frequency goes into the desired VCO output frequency. Recall that the reference frequency for the RF loop is not reduced prior to the phase detector. In other words, the frequency at the input of the REFin is the comparison frequency.

$$N = \frac{f_{VCO}}{f_{ref}} - \frac{MODULO\left(\frac{f_{VCO}}{f_{ref}}\right)}{f_{ref}} \qquad (2)$$

$$N = \frac{900\ MHz}{19.68\ MHz} - \frac{MODULO\left(\frac{900\ MHz}{19.68\ MHz}\right)}{19.68\ MHz}$$

$$N = 45.7317073170... - \frac{14.4}{19.68} = 45$$

Table 8. Allowable integer values (N) for the RF divider

<B8>	<B7>	<B6>	<B5>	<B4>	<B3>	<B2>	<B1>	<B0>	N
0	0	0	1	0	0	0	0	1	33
—	—	—	—	—	—	—	—	—	…
—	—	—	—	—	—	—	—	—	…
—	—	—	—	—	—	—	—	—	…
—	—	—	—	—	—	—	—	—	…
1	1	1	1	1	1	1	0	1	509

2.4.2 Power–down <B10:B9>

If the chip is programmed while in power-up mode, the loading of the A-word and of the N values in the B-word are synchronized to the RF divider output pulse. The data takes effect internally on the second falling edge of the RF divider output pulse after STROBE has gone high at the end of the A-word. STROBE does not need to be held high until that second falling edge of the RF divider output pulse has occurred.

If the chip is programmed while in power-down mode, this synchronization scheme is disabled. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data, even during power-down.

To take advantage of the program register pre-loading capability while the device is in power-down mode, the B-word needs to be sent a second time (i.e. again, after the A-word), with the PD bits now programmed for power-up. If power-up mode is to be controlled by hardware, the PON signal must be toggled only after the A-word has been sent and STROBE has gone high and then low.

When the synthesizer is reactivated after power-down mode, the IF and reference dividers are synchronized to avoid random phase errors on power-up. There is no power-up synchronization between the RF divider and the reference clock. However, after power-up, there is a delay of four edges (i.e. 1.5 cycles) of the output clock of the reference divider before the RF phase detector is activated. That means the reference divider must be powered up for the RF phase detector to become active.

When initially applying or re-applying power to the chip, an internal power-up reset pulse is generated which sets the programming-words to their default values and also resets the sigma-delta modulator to its “all-0” state. It is also recommended that the D-word be manually reset to all zeros, following initial power-up, to avoid unknown states.

Table 9. Power-down Truth Table

PON	IF <B10>	RF <B9>	IF	RF
0	0	0	OFF	OFF
0	0	1	OFF	ON
0	1	0	ON	OFF
0	1	1	ON	ON
1	0	0	ON	ON
1	0	1	ON	OFF
1	1	0	OFF	ON
1	1	1	OFF	OFF

2.4.3 Programming the IF Reference Divider <B21:B12>

The IF phase detector's reference input is an integer multiple of the frequency at the input of the REFin pin. The reference divider has 10 programmable bits, <B21:B12> for allowable divide ratios, R, from 4 to 1023 when the 3 bit binary SA counter (refer to section 2.5.1) is set to all zeros. Table 10 lists the allowable R values.

Table 10. R Values for the IF Reference Divider

<B21>	<B20>	<B19>	<B18>	<B17>	<B16>	<B15>	<B14>	<B13>	<B12>	R
0	0	0	0	0	0	0	1	0	0	4
0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	1	1	0	6
—	—	—	—	—	—	—	—	—	—	…
1	1	1	1	1	1	1	1	1	0	1022
1	1	1	1	1	1	1	1	1	1	1023

2.5 C-word Register

Table 11. C-word, length 24 bits

Last IN		<21>	<20>	<19>	<18>	<17>	<16>	<15>	<14>	<13>	<12>	<11>	<10>	<9>	<8>	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
Address		IF Divider An														CP		Lock detect		Reset bit	SA		
1	0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	CP1	CP0	L1	L0	Tsigrst	SA2	SA1	SA0
Default:		0	0	0	0	0	1	1	1	0	0	1	0	1	0	1	1	0	0	0	0	0	0

C-word address	Fixed to 10
A-Divider	A0..A13, IF divider values , see section "characteristics for allowed for divider ratios.
Charge pump current Ratio	CP1, CP0: Charge pump current ratio, see table of charge pump currents.
Lock detect	See Table 13.
Reset bit	1 → Tsigrst : resets the sigma-delta modulator after each loading of an A-word. (It is held in the reset state between the first and second falling edge of the RF divider output pulse after STROBE has gone high at the end of the A-word.)
IF comparison select	SA Comparison divider select for IF phase detector

2.5.1 Programming the SA Counter <C2:C0>

The 3 bit SA register determines which of the 5 divider outputs (refer to table 11) is selected as the IF phase detector's input (see Figure 5).

Table 12. IF phase comparator frequency

<C2>	<C1>	<C0>	Divide Ratio	IF Phase Comparator Frequency
0	0	0	R	f_{ref} [1] / R
0	0	1	R * 2	f_{ref} / (R * 2)
0	1	0	R * 4	f_{ref} / (R * 4)
0	1	1	R * 8	f_{ref} / (R * 8)
1	0	0	R * 16	f_{ref} / (R * 16)

NOTES:
1. f_{ref} is the input frequency at the REFin pin.

2.5.2 Programming the Reset Bits <B11>, <C3>

The reset bits offer extra flexibility. The default value for bits <B11>, <C3> are all zeros. Bit <B11> disables the IF reference divider and allows for extra savings of approximately 200 μA when set to '1'. However, this bit must initially be set to '0' during any power-up sequence. The RF phase detector is activated after a delay of four edges of the reference divider output clock. Bit <C3> resets the sigma-delta modulator after each loading of an A-word. It is held in the reset state between the first and second falling edge of the RF divider output pulse after STROBE has gone high at the end of the A-word.

2.5.3 Programming the Lock Detect <C4:C5>

Lock detection is available only for the RF and IF phase detector. A ‘0’ in bit <C4:C5> is used for TTL, while a ‘1’ in bit <C4:C5> is used for RTL.

Table 13. Lock detect select

L1	L0	Select
0	0	RF/IF (push/pull)[1]
0	1	RF/IF (open drain)
1	0	RF (push/pull)
1	1	IF (push/pull)

NOTE:
1. Combined RF_IF lock detect signal present at the lock pin (push/pull).

2.5.4 Programming the Charge Pump Gain <C7:C6>

The RF phase detector drives the charge pumps on the PHP and PHI pins, while the IF phase detector drives the charge pump on the PHA pin. The current generated at the R_{SET} pin determines both the RF and IF charge pump current values in conjunction with the current gain programmed by the CP0, CP1 bits in the C–word, as seen in Table 1. For more information on charge pump speed-up mode, refer to section 1.6.

2.5.5 Programming the IF Divider for the IF Loop <C21:C8>

The divider is a fully programmable counter. The allowable divide ratios, A, are from 128 to 16383, bits <C21:C8>. Table 14 shows all the possible values that can be programmed into the C-word for the IF divider.

Table 14. Allowable Values (A) for the IF Divider

C21	C20	C19	C18	C17	C16	C15	C14	C13	C12	C11	C10	C9	C8	A
0	0	0	0	0	0	1	0	0	0	0	0	0	0	128
0	0	0	0	0	0	1	0	0	0	0	0	0	1	129
0	0	0	0	0	0	1	0	0	0	0	0	1	0	130
—	—	—	—	—	—	—	—	—	—	—	—	—	—	…
1	1	1	1	1	1	1	1	1	1	1	1	1	0	16382
1	1	1	1	1	1	1	1	1	1	1	1	1	1	16383

2.6 D-word Register

The D-word is for test purposes only. All bits in this test word should be initialized to 0 for normal operation. When initially applying or re-applying power to the chip, an internal power-up reset pulse if generated which sets the programming-words to their default values and which resets the sigma-delta modulator to its “all-0” state. It is also recommended that the D-word be manually reset to all zeros, following initial power-up, to avoid unknown states.

Table 15. D-word, length 24 bits

Last IN		<21>	<20>	<19>	<18>	<17>	<16>	<15>	<14>	<13>	<12>	<11>	<10>	<9>	<8>	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
Address			Synthesizer Test bits																				
1	1	0	–	–	–	–	Tdis-spu	Tspu	–	–	–	TreadN	–	–	–	–	–	–	–	–	–	–	–
Default			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D word address	Fixed to 110.
Tdis-spu	Speed-up mode disabled. **NOTE:** All other test bits must be set to 0 for normal operation.
Tspu: Speed up	Speed-up mode always on. **NOTE:** All other test bits must be set to 0 for normal operation.
TreadN	Used to “request to read” bit settings from bits <B21:12>. For more information on reading out the N value, refer to Section 2.0, Serial Programming Bus.

3.0 Typical Performance Characteristics

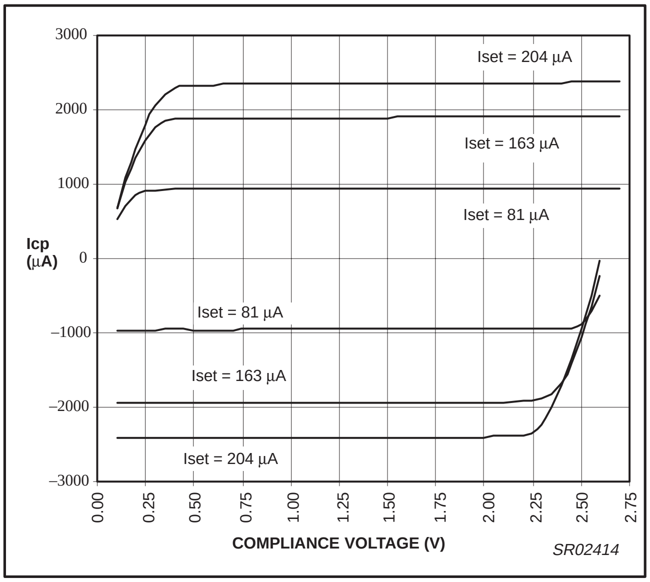


Figure 11. PHI_SU charge pump output vs. Iset (CP = 01_12x, V_{DD} = 3.0 V, Temp = 25 °C)

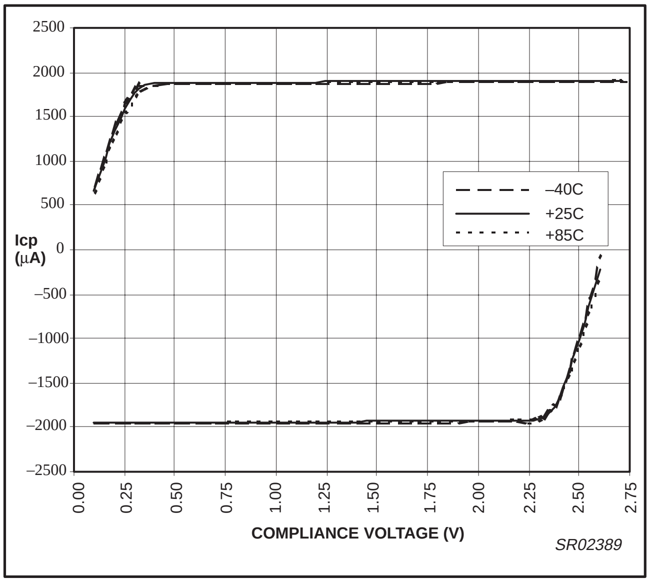


Figure 12. PHI_SU charge pump output vs. temperature (CP = 01_12x, V_{DD} = 3.0 V, Iset = 163 μA)

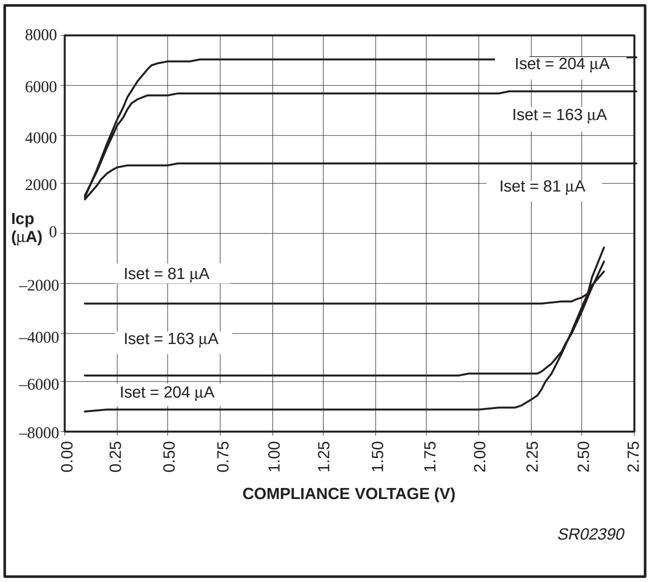


Figure 13. PHI_SU charge pump output vs. Iset (CP = 00_36x, V_{DD} = 3.0 V, Temp = 25 °C)

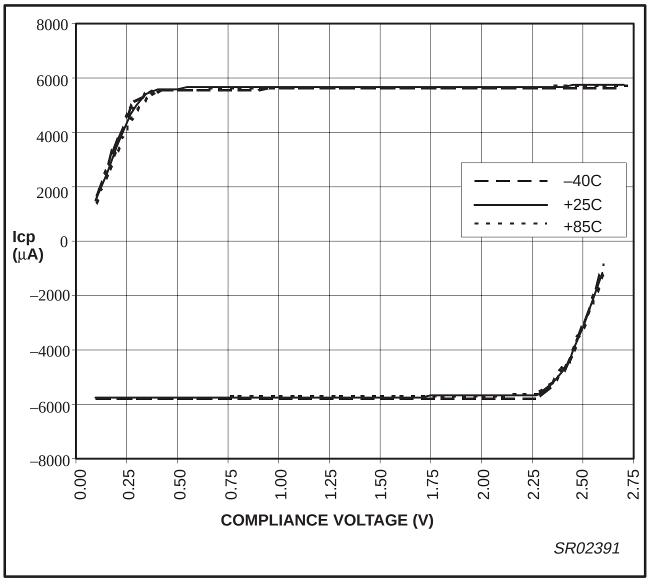


Figure 14. PHI_SU charge pump output vs. temperature (CP = 00_36x, V_{DD} = 3.0 V, Iset = 163 μA)

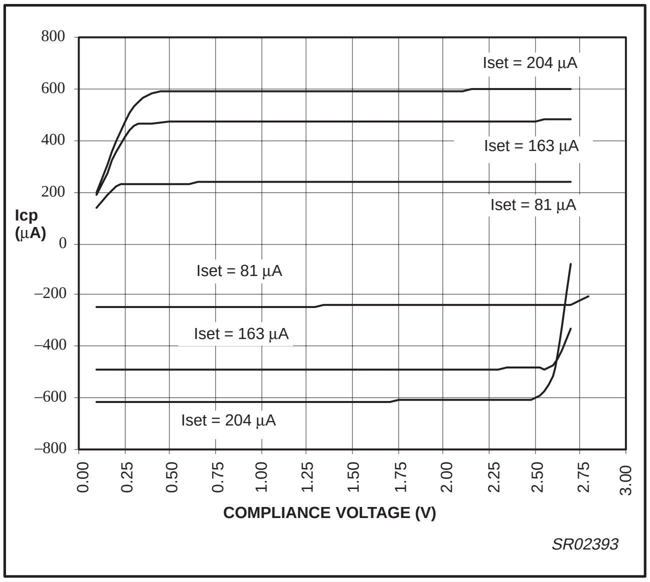


Figure 15. PHP charge pump output vs. Iset (CP = 10_3x, V_{DD} = 3.0 V, Temp = 25 °C)

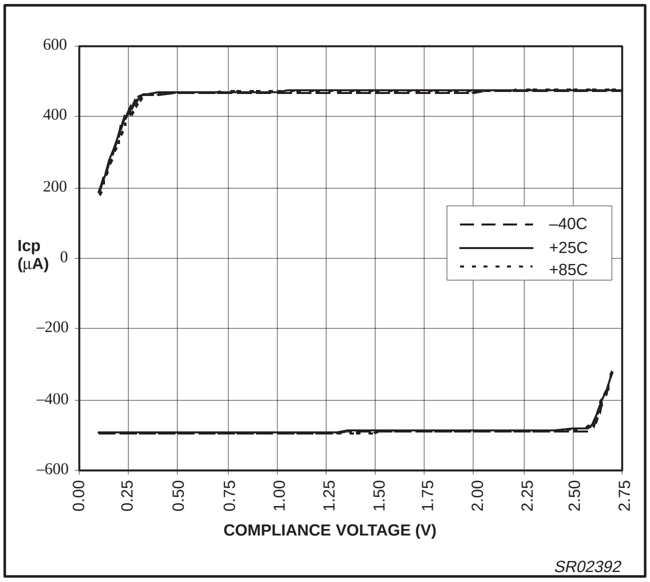


Figure 16. PHP charge pump output vs. temperature (CP = 10_3x, V_{DD} = 3.0 V, Iset = 163 µA)

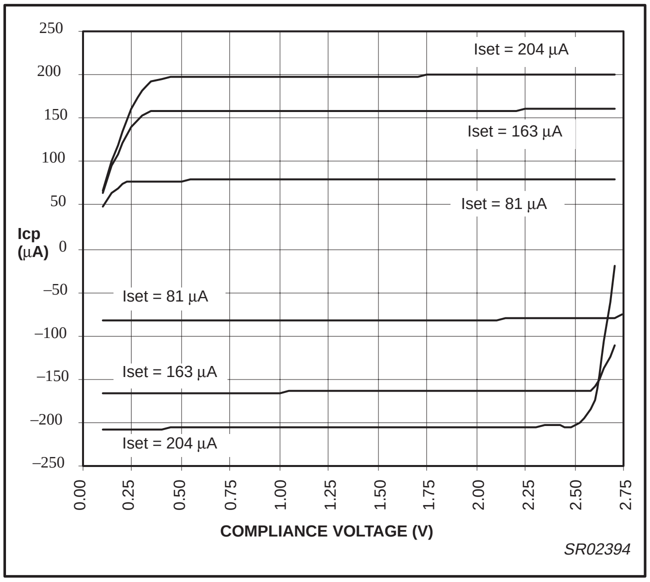


Figure 17. PHP charge pump output vs. Iset (CP = 11_1x, V_{DD} = 3.0 V, Temp = 25 °C)

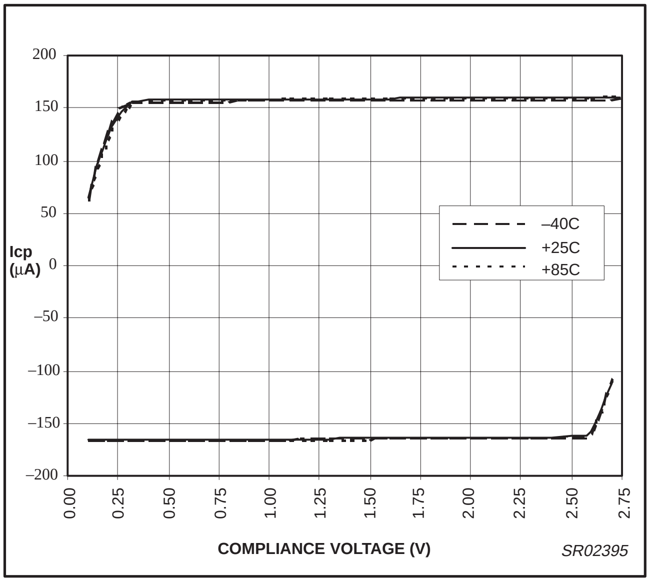


Figure 18. PHP charge pump output vs. temperature (CP = 11_1x, V_{DD} = 3.0 V, Iset = 163 µA)

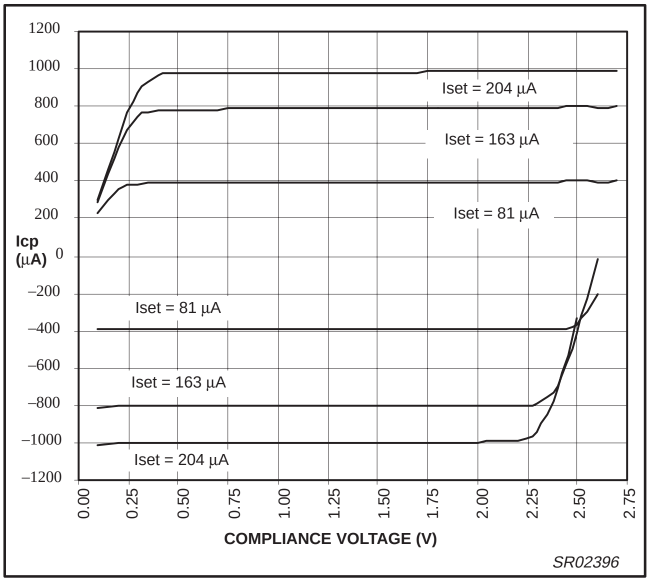


Figure 19. PHP_SU charge pump output vs. Iset (CP = 01_5x, V_{DD} = 3.0 V, Temp = 25 °C)

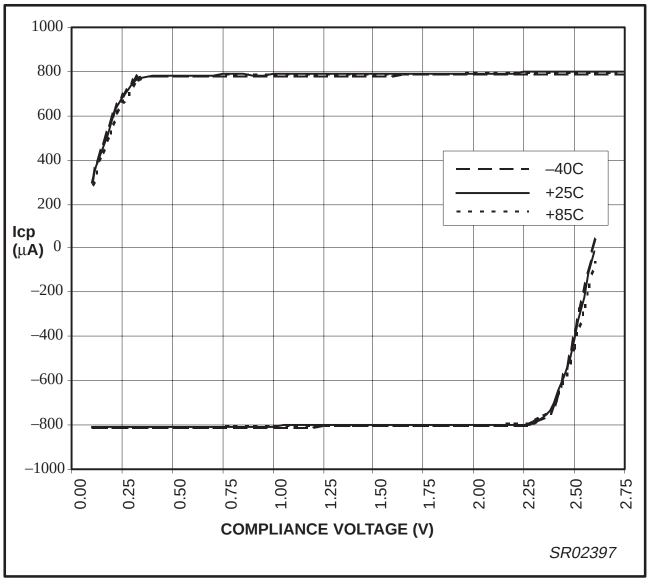


Figure 20. PHP_SU charge pump output vs. temperature (CP = 01_5x, V_{DD} = 3.0 V, Iset = 163 µA)

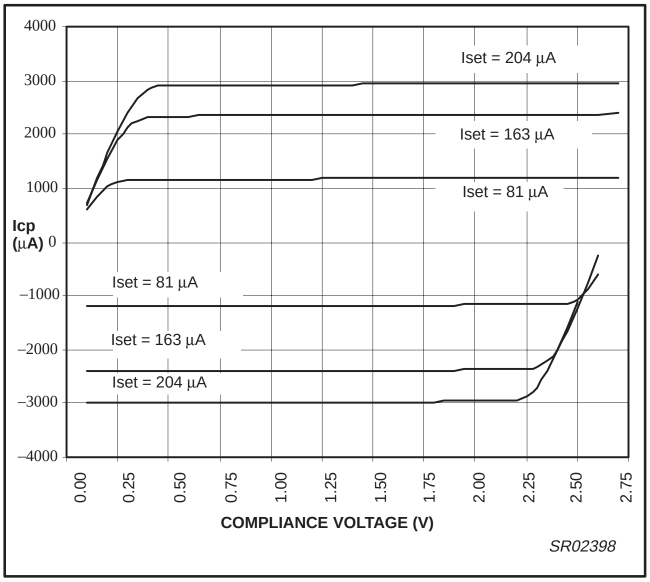


Figure 21. PHP_SU charge pump output vs. Iset (CP = 00_15x, V_{DD} = 3.0 V, Temp = 25 °C)

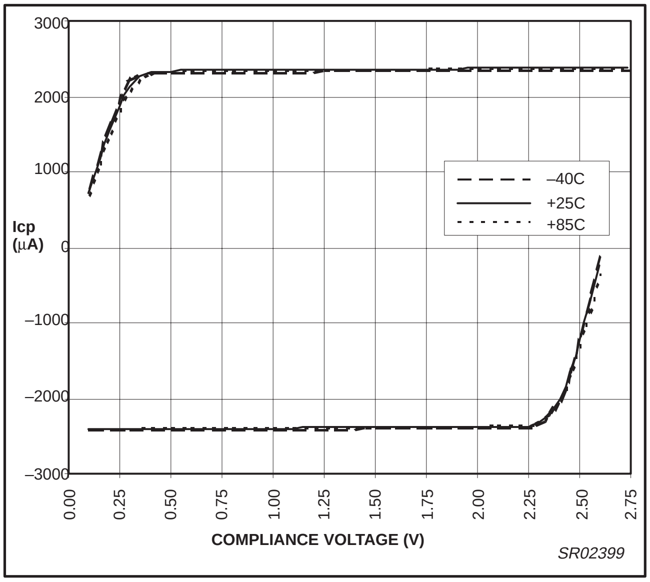


Figure 22. PHP_SU charge pump output vs. temperature (CP = 00_15x, V_{DD} = 3.0 V, Iset = 163 µA)

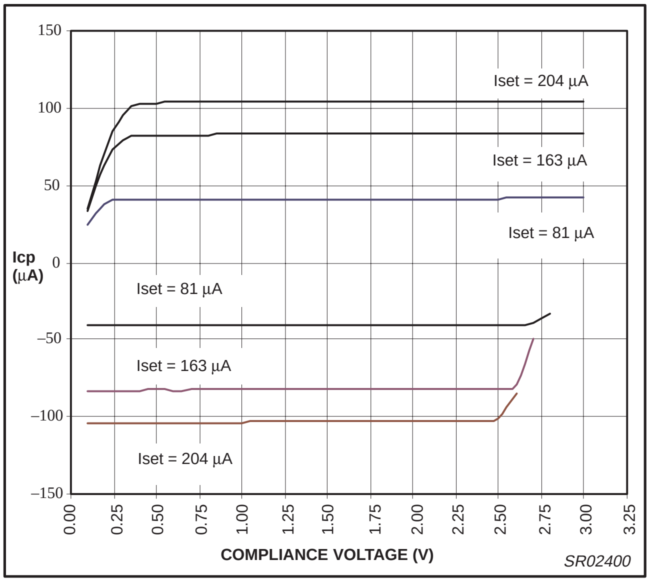


Figure 23. PHA charge pump output vs. Iset (CP = 11_0.5x, V_{DD} = 3.0 V, Temp = 25 °C)

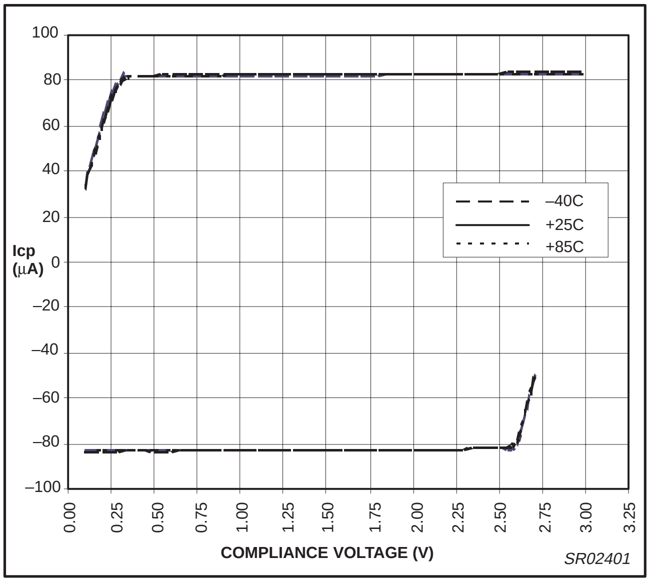


Figure 24. PHA charge pump output vs. temperature (CP = 11_0.5x, V_{DD} = 3.0 V, Iset = 163 µA)

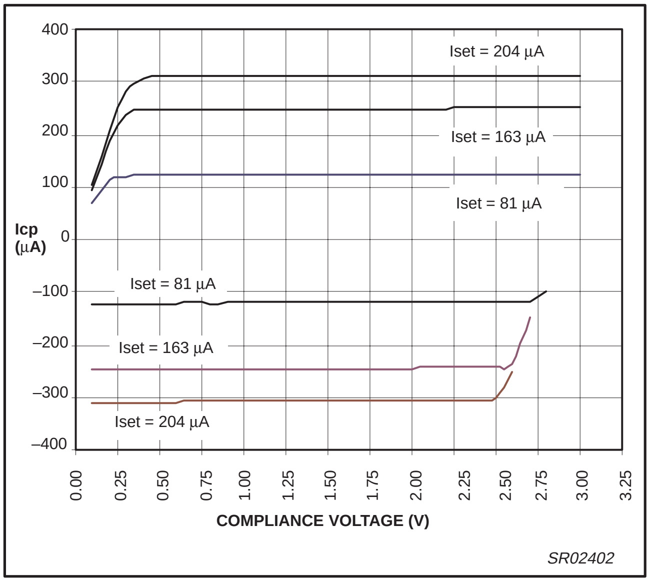


Figure 25. PHA charge pump output vs. Iset (CP = 10_1.5x, V_{DD} = 3.0 V, Temp = 25 °C)

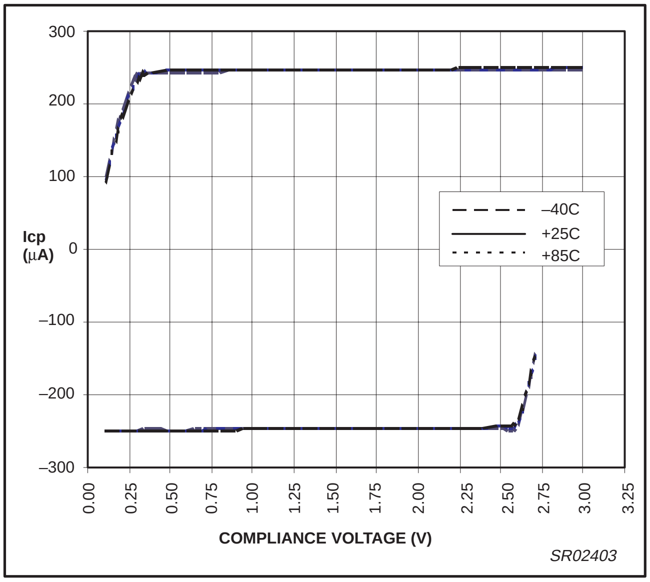


Figure 26. PHA charge pump output vs. temperature (CP = 10_1.5x, V_{DD} = 3.0 V, Iset = 163 µA)

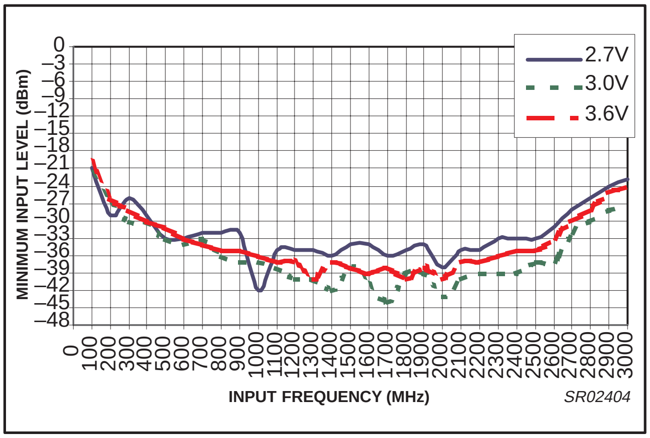


Figure 27. RF (main) divider input sensitivity vs. frequency and supply voltage (Temp = 25 °C, Iset = 164 µA, N = 509)

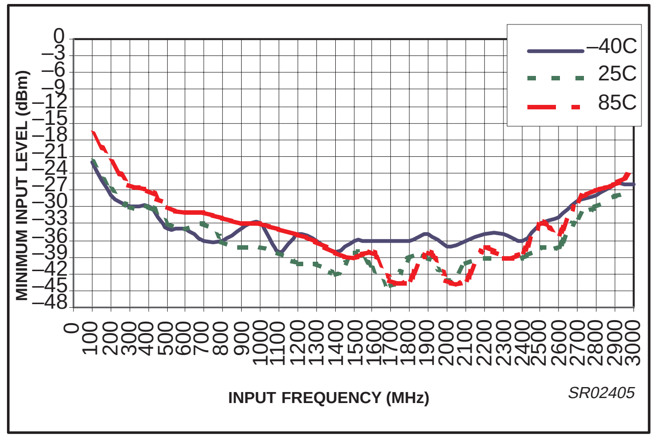


Figure 28. RF (main) divider input sensitivity vs. frequency and temperature (V_{CC} = 3.0 V, Iset = 164 µA, N = 509)

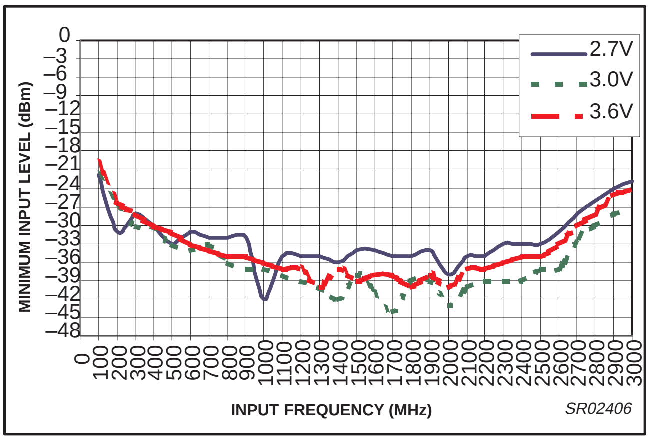


Figure 29. RF (main) fractional divider input sensitivity vs. frequency and supply voltage (Temp = 25 °C, Iset = 164 µA, N = 509.5)

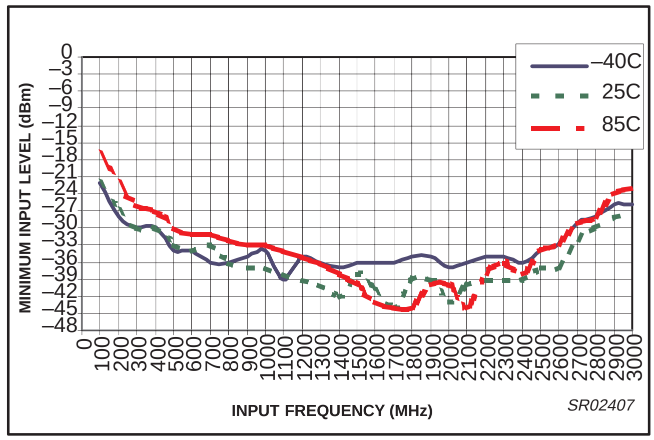


Figure 30. RF (main) fractional divider input sensitivity vs. frequency and temperature (V_{CC} = 3.0 V, Iset = 164 µA, N = 509.5)

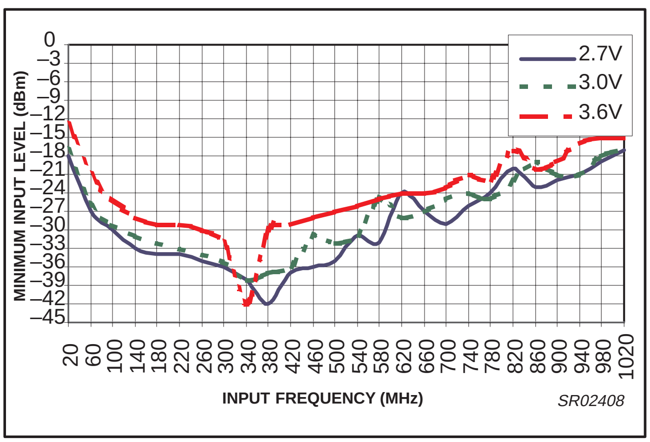


Figure 31. IF (aux) divider input sensitivity vs. frequency and supply voltage (Temp = 25 °C, Iset = 164 µA, divider ratio = 16383)

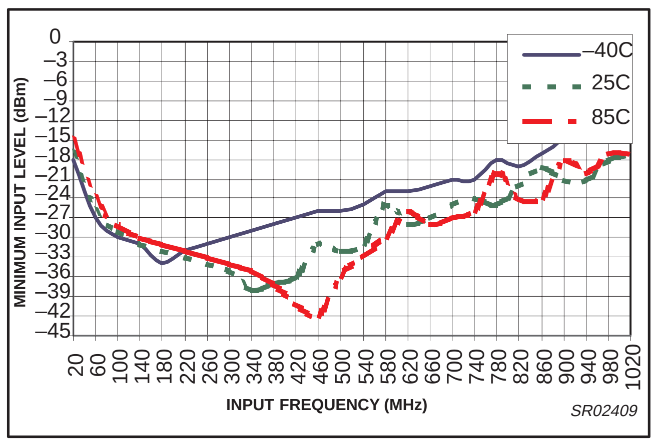


Figure 32. IF (aux) divider input sensitivity vs. frequency and temperature (V_{CC} = 3.0 V, Iset = 164 µA, divider ratio = 16383)

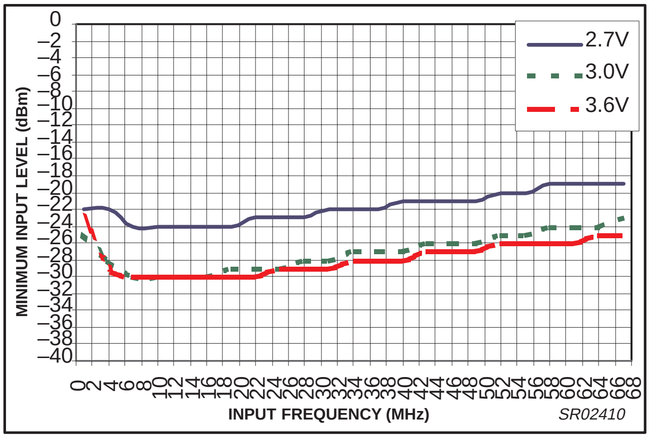


Figure 33. Reference divider input sensitivity vs. frequency and supply voltage (Temp = 25 °C, Iset = 164 µA, divider ratio = 1023)

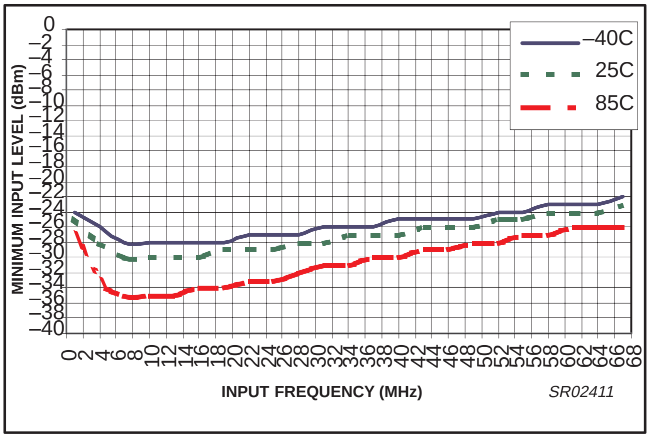


Figure 34. Reference divider input sensitivity vs. frequency and temperature (V_{CC} = 3.0 V, Iset = 164 µA, divider ratio = 1023)

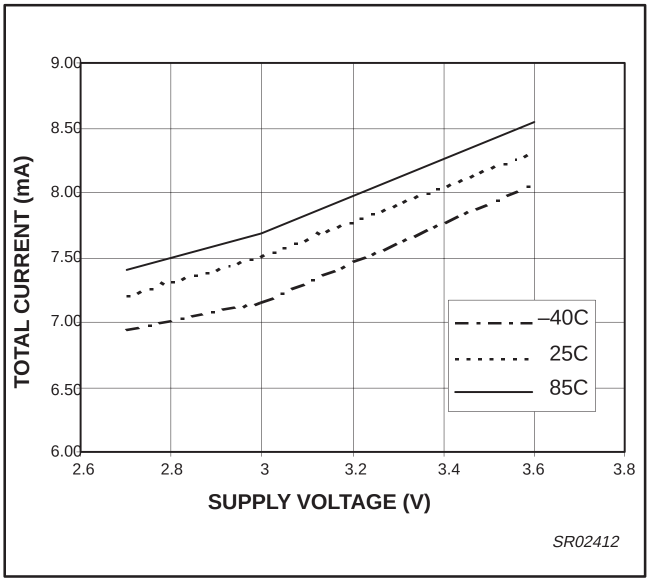
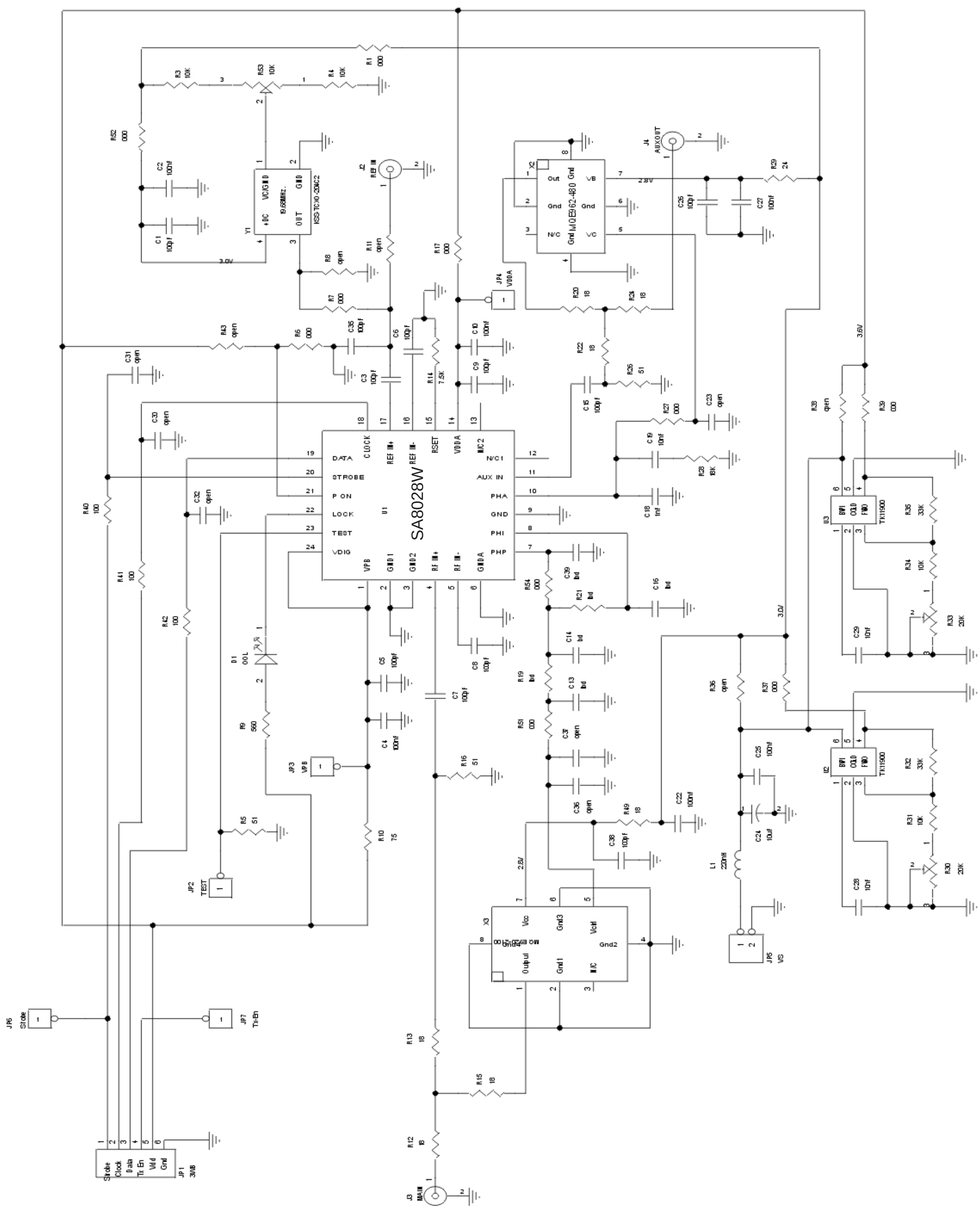
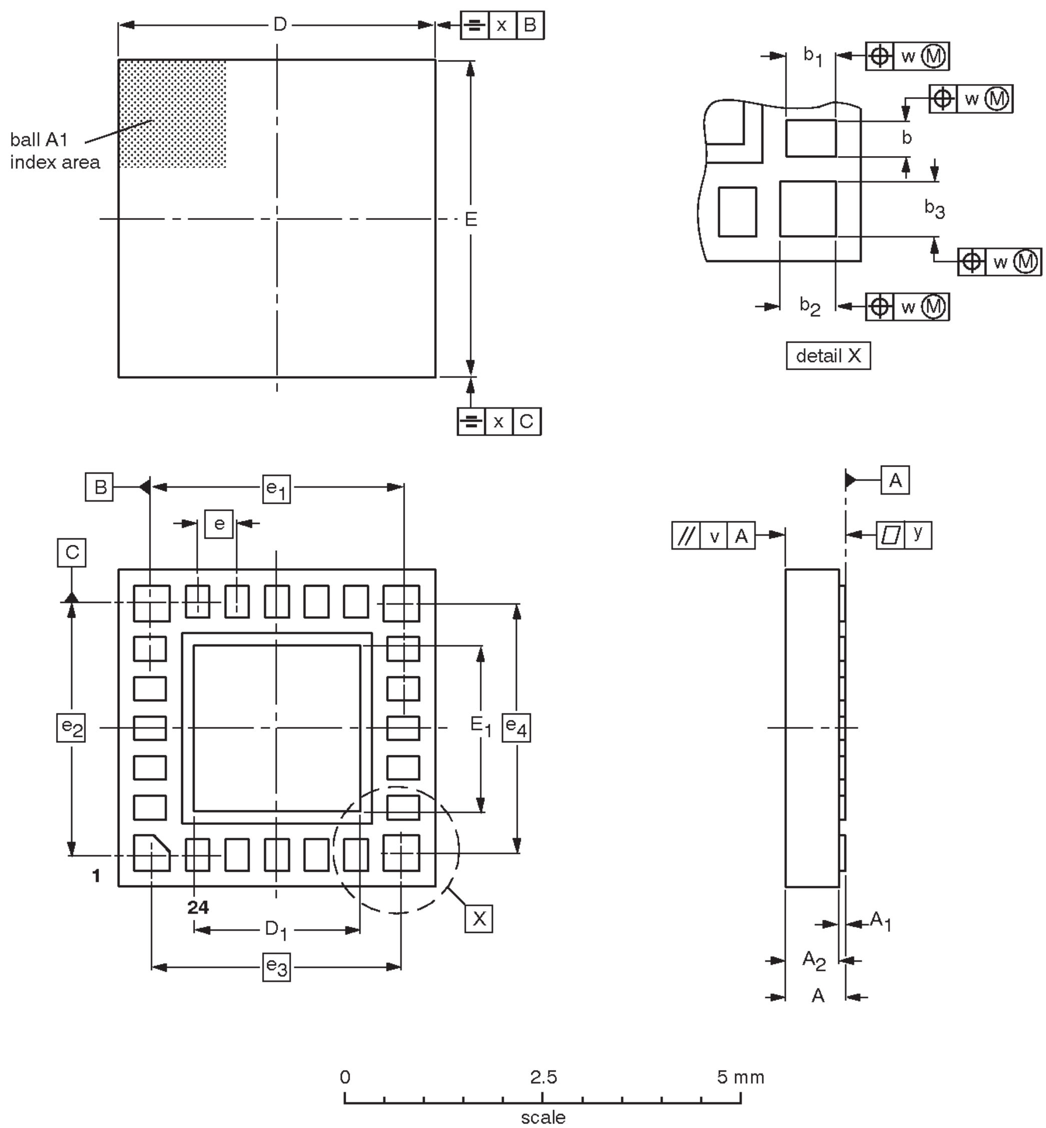


Figure 35. Total supply current vs. temperature (Iset = 163 µA Fcomp = 20 MHz)

4.0 Application Schematic



HBCC24: plastic, heatsink bottom chip carrier; 24 terminals; body 4 x 4 x 0.65 mm SOT564-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	b_1	b_2	b_3	D	D_1	E	E_1	e	e_1	e_2	e_3	e_4	v	w	x	y
mm	0.80	0.10 0.05	0.70 0.60	0.35 0.20	0.50 0.30	0.50 0.35	0.50 0.35	4.1 3.9	2.2 2.0	4.1 3.9	2.2 2.0	0.5	3.2	3.2	3.15	3.15	0.2	0.15	0.15	0.05

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT564-1		MO-217				~~00-02-01~~ 00-08-28

NOTES

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Data sheet status [1]	Product status [2]	Definitions
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