DATA SHEET

DIGITAL dcc COMPACT CASSETTE

SAA2012
Adaptive allocation and scaling for record processing in DCC systems

Product specification
Supersedes data of February 1993
File under Integrated Circuits, Miscellaneous

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Philips Semiconductors

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Adaptive allocation and scaling for record processing in DCC systems

SAA2012

FEATURES

- Stereo or 2-channel mono encoding
- Status may be read continuously
- Microcontroller interface
- I^2S interfaces
- Allocation algorithm including optional emphasis correction (for 44.1 kHz)
- Reduced power consumption
- 4 V nominal operating voltage capability.

GENERAL DESCRIPTION

Performing the Adaptive Allocation and Scaling function in the Precision Adaptive Sub-band Coding (PASC) system, the SAA2012 is intended for use in conjunction with the stereo filter and codec (SAA2002).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2012GP	44	QFP; note 1	plastic	SOT205AG

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the "*Quality Reference Pocketbook*" are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM

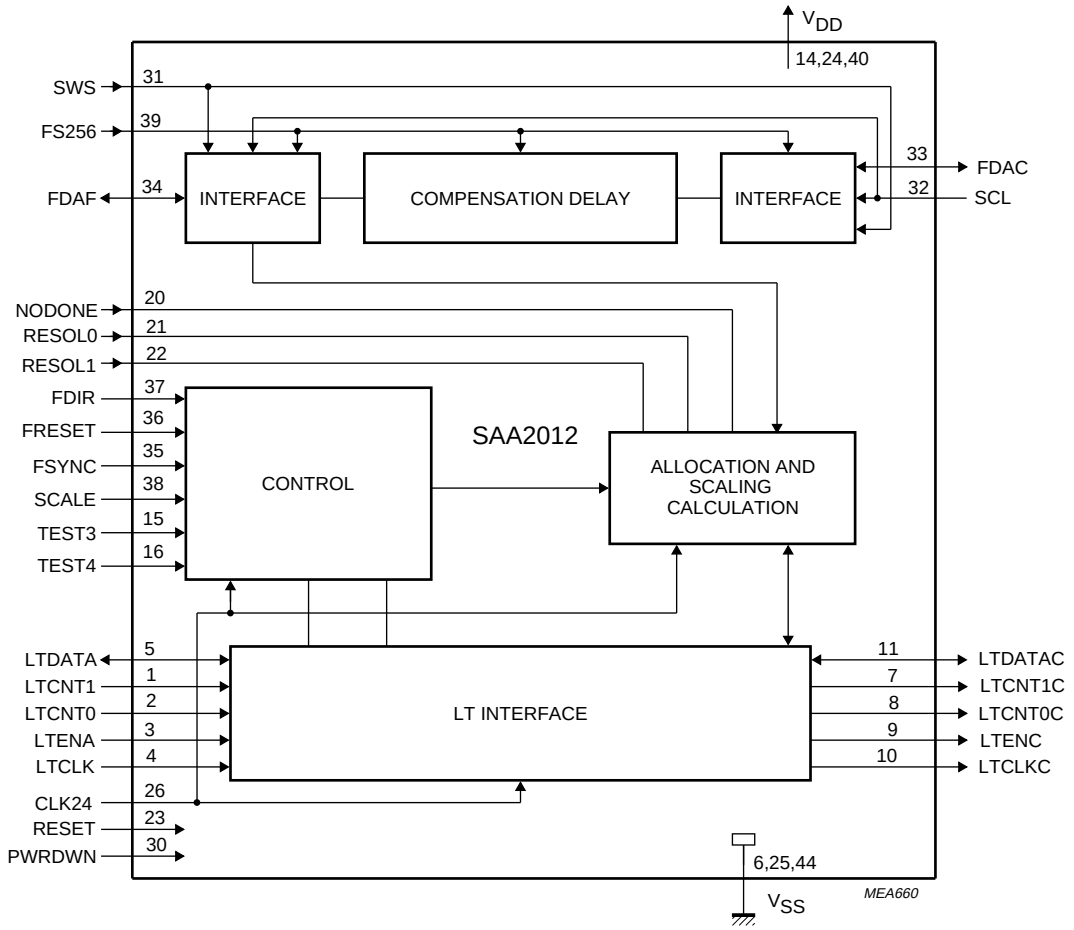


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LTCNT1	1	mode control 1, microcontroller interface input
LTCNT0	2	mode control 0, microcontroller interface input
LTENA	3	enable microcontroller interface input
LTCLK	4	bit clock microcontroller interface input
LTDATA	5	data, microcontroller interface (3-state input/output)
V_{SS}	6	supply ground (0 V)
LTCNT1C	7	control 1, microcomputer interface, SAA2002 side output
LTCNT0C	8	control 0, microcomputer interface, SAA2002 side output
LTENC	9	enable microcontroller interface, SAA2002 side output
LTCLKC	10	bit clock; microcontroller interface, SAA2002 side output
LTDATAC	11	data; microcontroller interface, SAA2002 side (3-state input/output)
TEST1	12	test 1 output; do not connect
TEST2	13	test 2 output; do not connect
V_{DD}	14	supply voltage (+5 V)
TEST3	15	test 3 mode input; to be connected to V_{DD}
TEST4	16	test 4 mode input; to be connected to V_{DD}
TEST5	17	test 5 input; to be connected to V_{SS}
TEST6	18	test 6 input; to be connected to V_{SS}
TEST7	19	test 7 input; to be connected to V_{SS}
NODONE	20	no done state selection input
RESOL0	21	resolution selection 0 input
RESOL1	22	resolution selection 1 input
RESET	23	active HIGH reset input
V_{DD}	24	supply voltage (+5 V)
V_{SS}	25	supply ground (0 V)
CLK24	26	24.576 MHz processing clock input
TEST8	27	test 8 input; to be connected to V_{SS}
TEST9	28	test 9 input; to be connected to V_{SS}
TEST10	29	test 10 input; to be connected to V_{SS}
PWRDWN	30	SLEEP mode input
SWS	31	word selection input; filtered - I^2S-interface
SCL	32	bit clock input; filtered - I^2S-interface
FDAC	33	filtered data - I^2S-interface; SAA2002 side (3-state input/output)
FDAF	34	filtered data - I^2S-interface; SAA2002 side (3-state input/output)
FSYNC	35	sub-band synchronization on input; filtered - I^2S-interface
FRESET	36	reset signal input from SAA2002
FDIR	37	direction input of the I^2S-interface
SCALE	38	scale factor index select (note 1)
FS256	39	system clock input; sample frequency $\times$ 256
V_{DD}	40	supply voltage (+5 V)

SYMBOL	PIN	DESCRIPTION
n.c.	41	not connected
n.c.	42	not connected
n.c.	43	not connected
V_{SS}	44	supply ground (0 V)

Note

1. The SCALE input must be set LOW for use with the SAA2002. If operation with the SAA2001/2021 combination is required the SCALE input must be set HIGH.

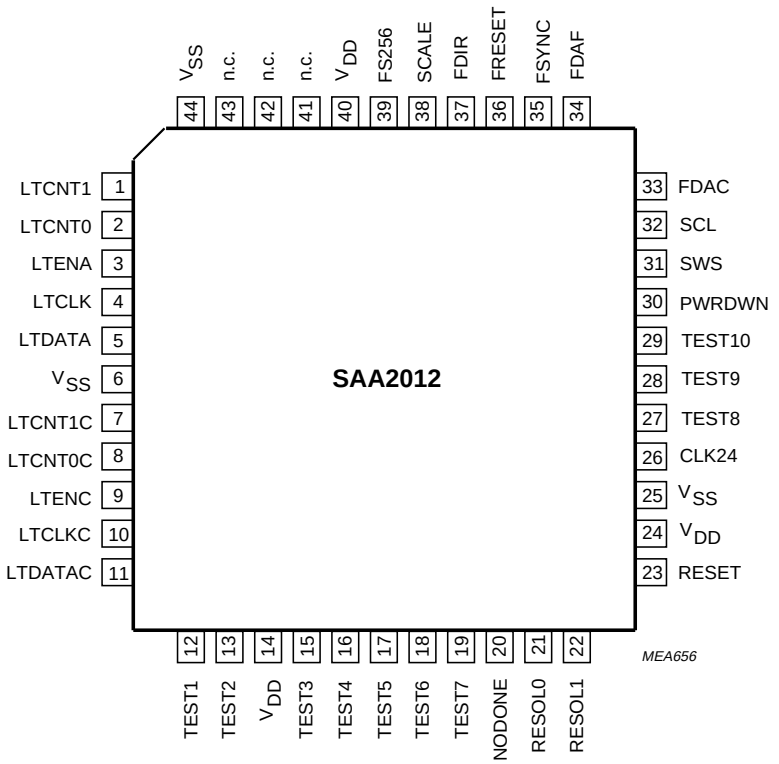


Fig.2 Pin configuration.

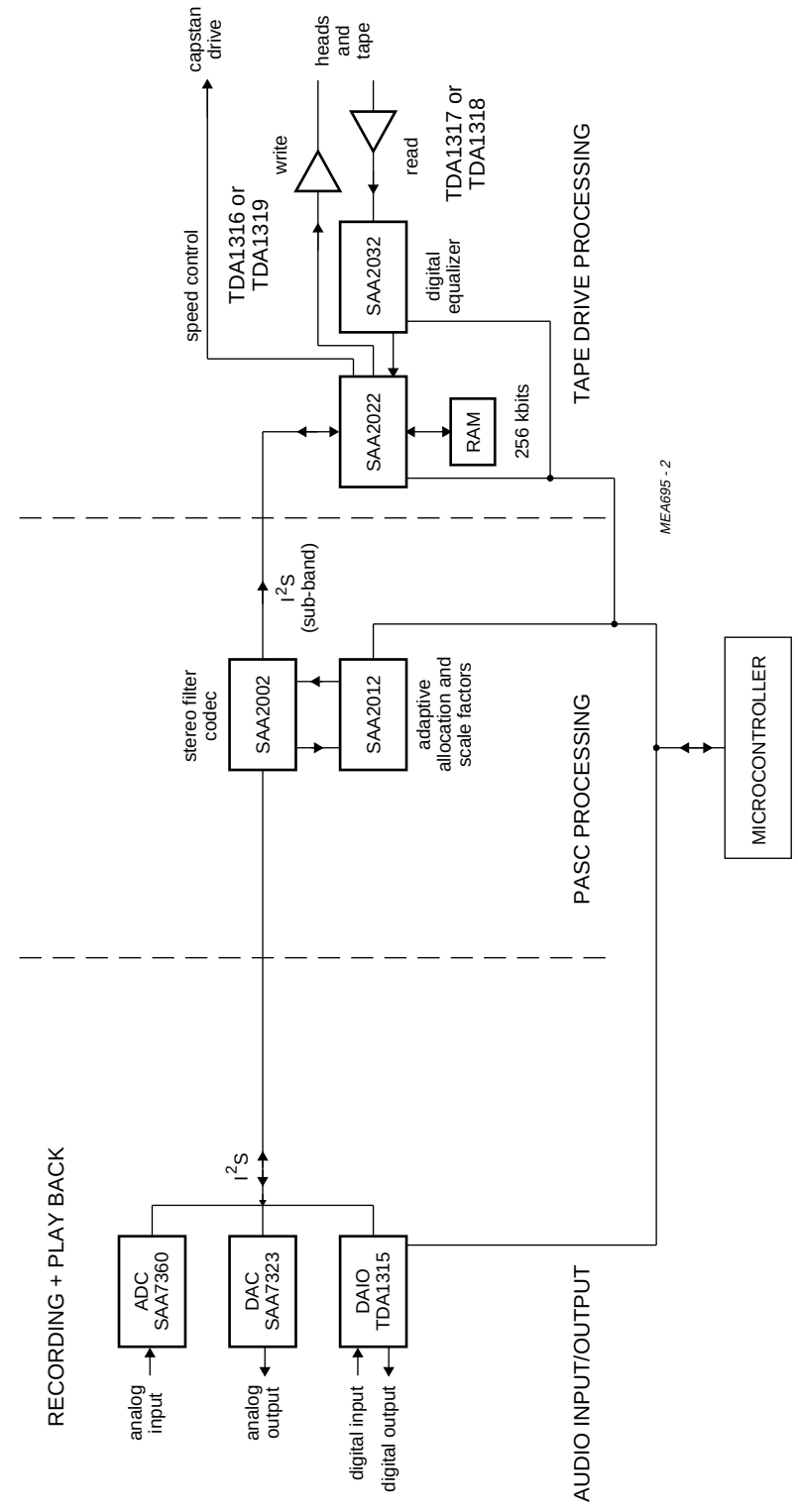


Fig.3 DCC data flow diagram.

FUNCTIONAL DESCRIPTION

PASC

Precision Adaptive Sub-band Coding achieves highly efficient digital encoding with a bit-rate of 384 kbits/s. It utilizes a system producing sub-band samples from an incoming digital audio signal. This relies upon the audibility of signals above a given level and upon high amplitude signals masking those of lower amplitude. Although each sub-band signal is of approximately 750 Hz bandwidth, it possesses considerable overlap with those adjacent to it.

During the process of encoding, the PASC processor analyses the broadband audio signal at sampling frequency (f_s) by splitting it into 32 sub-band signals at a sampling frequency ($f_s/32$).

The PASC signal consists of frames conveying the information corresponding to 384 sub-band samples. These also include a synchronization pattern identifying the start of each new frame. The allocation information for the 32 sub-bands is transferred as 4-bit values. If the amplitude of a sub-band signal is below the masking threshold it will be omitted from the PASC signal.

The duration of a PASC frame depends upon sampling frequency and is adjusted to 384 divided by f_s.

Adaptive Allocation and Scaling

The PASC system calculates the masking power of the sub-band signals and adds the masking threshold. Sub-band signals with power below this threshold denote information to be discarded. Non-masked signals are coded using floating point notation in which a mantissa corresponds in length to the difference between peak power and masking threshold. The process is repeated for every PASC frame and is known as the Adaptive Allocation of the available capacity.

Encoding mode

Signal FDIR sets the data flow direction on the Filtered-I^2S-interface. In the encoding mode (FDIR = LOW) the device will accept samples from FDAF. These will be delayed by a number of sample periods depending upon the setting of the SCALE input. In the event of operation with the SAA2002 (SCALE = 0) this delay will be 480 SWS periods. This will ensure alignment of the data with the computed allocations.

After the delay the samples will be presented on FDAC (pin 33). The circuit also performs all the calculations required to build the allocation table which is used in the codec (SAA2002).

When used with the SAA2002 the calculated scale factor indices are sent via the LT interface. These operations are performed for every frame of the sub-band codec.

In order to synchronize with the codec and utilize the correct tables for the calculations the SAA2012 frequently requests the status of the codec. It monitors the bit-rate, sample frequency, operation mode and the emphasis information and uses the ‘ready-to-receive’ bit of the codec to determine the moment of the transfer of allocation information.

Decoding Mode

In the decoding mode (FDIR = HIGH) the SAA2012 will take samples from FDAC which will be presented on the FDAF after a delay of 160 SWS periods. The LT interface between microcontroller and codec (SAA2002) will only be affected by the ‘ready-to-receive’ bit from the codec (SAA2002).

Microcontroller Interface Operation

Information on the interface between microcontroller and codec (SAA2002) will flow in a regular sequence synchronized with the codec (SAA2002):

- With every FSYNC the SAA2012 will read the status of the codec (SAA2002).
- Following the calculation of the allocation and scale factors the SAA2012 will send the first allocation information unit (16-bits). It will then continuously read the codec (SAA2012) status to ascertain when it is able to receive further allocation information units. When the transfer of these units is complete the SAA2012 will send settings and (for SCALE = 0) scale factor indices.
- The extended settings will be sent to the codec as soon as possible after reception from the microcontroller.

The microcontroller communicates with the SAA2012 in a similar fashion:

- Status can be read continuously. The SAA2012 will output a copy of the codec (SAA2002) status on the LTDATA line except for the ‘ready-to-receive’ bits which are generated by the SAA2012. These indicate whether the SAA2012 is ready to receive the next settings or extended settings.
- Settings can be sent following every occasion that the ‘ready-to-receive’ bit ‘S’ changes to logic 1.
- Extended settings can be sent following each occasion that the ‘ready-to-receive’ bit ‘E’ changes to logic 1.

Mode Control

Operation is controlled by the FRESET and FDIR signals. FRESET causes a general reset. The FDIR signal is sampled at the falling edge of the FRESET signal to determine the operation mode:

- FDIR = logic 1 decoding mode, SAA2012 in feed-through mode
- FDIR = logic 0 encoding mode, SAA2012 in calculation mode.

Figure 4 shows the timing diagram for FRESET and FDIR.

Resolution Selection

The (SAA2012) is designed for operation with input devices (ADCs) which may possess a different sample resolution capability, i.e. audio sample inputs into the sub-band filters. RESOL0 (pin 21) and RESOL1 (pin 22) may be utilized to adjust the allocation information calculation to the resolution of the samples.

With the instance of NODONE (pin 20) being HIGH, all available bits in the bit-pool will be allocated. If NODONE is LOW, no bits will be allocated to the sub-bands with energy levels below the theoretical threshold for the selected resolution. For encoding in accordance with the DCC standard NODONE must be HIGH.

Table 1 Resolution selection.

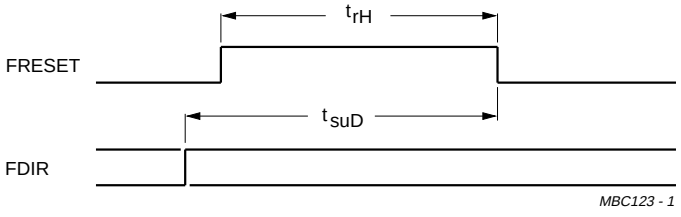
RESOL1	RESOL0	RESOLUTION
0	0	16 bits
0	1	18 bits
1	0	14 bits
1	1	15 bits

Sleep mode switching

When the potential on the RESET pin (pin 23) is held HIGH for at least $5T_{clk24}$ clock periods, the device will be reset after which it will operate in its decoding mode.

The sleep mode is activated when the PWRDWN pin (pin 30) is held HIGH. The 3-state buffers will be set to a high impedance while the normal outputs will retain the state attained prior to this mode being entered. This mode can only be used if other associated circuits react accordingly. The sleep mode is de-activated by a reset action.

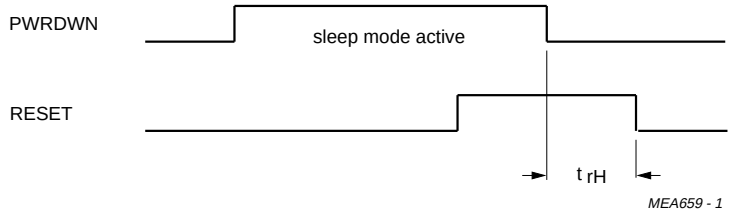
Operation for the sleep mode switching is shown in Fig.5.



$t_{rH} > 5T_{clk24}$ = 210 ns (for CLK = 24.576 MHz) minimum time; FRESET = HIGH.

$t_{suD} < 0$ ns minimum set-up time; FDIR to FRESET = LOW.

Fig.4 Timing of FRESET and FDIR.



$t_{rH} > 5T_{clk24}$ = 210 ns (for CLK = 24.576 MHz) minimum time; RESET = HIGH.

Fig.5 Sleep mode switching.

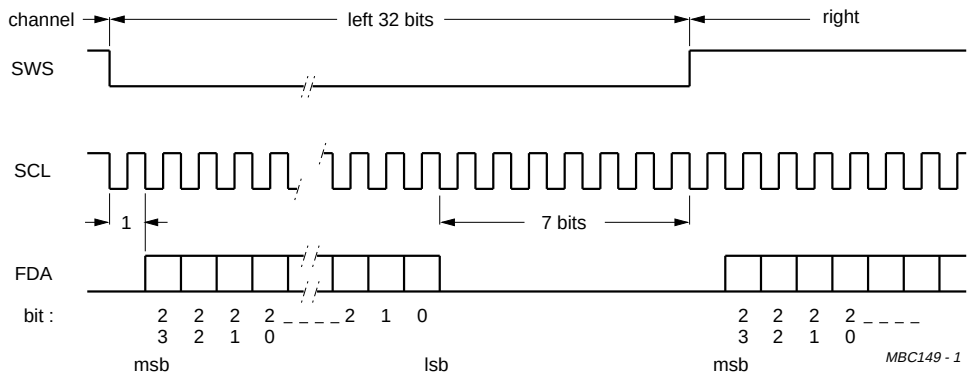


Fig.6 Format for transferring filtered data.

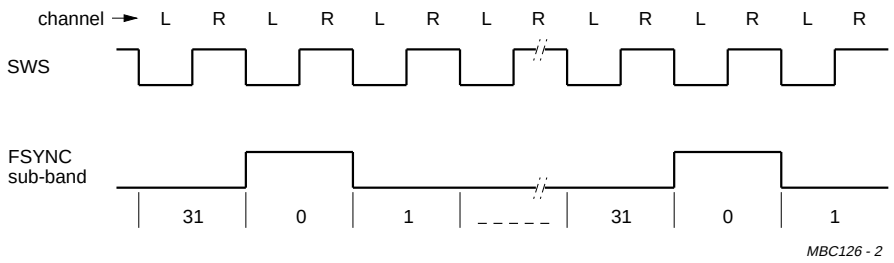


Fig.7 FSYNC relative to SWS.

Filtered-I²S-Interfaces

Interfaces with the sub-band filter and codec (SAA2002) consist of the signals shown in Table 2.

Table 2 The filtered-I²S-interface.

SIGNAL	TYPE	DESCRIPTION	FREQUENCY
SWS	input	word selection	f_s
SCL	input	bit clock	$64f_s$
FDAF	bi-directional	filtered data to/from the filter section of SAA2002	–
FDAC	bi-directional	filtered data to/from the codec section of SAA2002	–
FSYNC	input	filter synchronization	$f_s/32$
FRESET	input	reset	–
FDIR	input	filtered - I²S-interface direction of data flow	–

The format for transferring filtered data is shown in Fig.6.

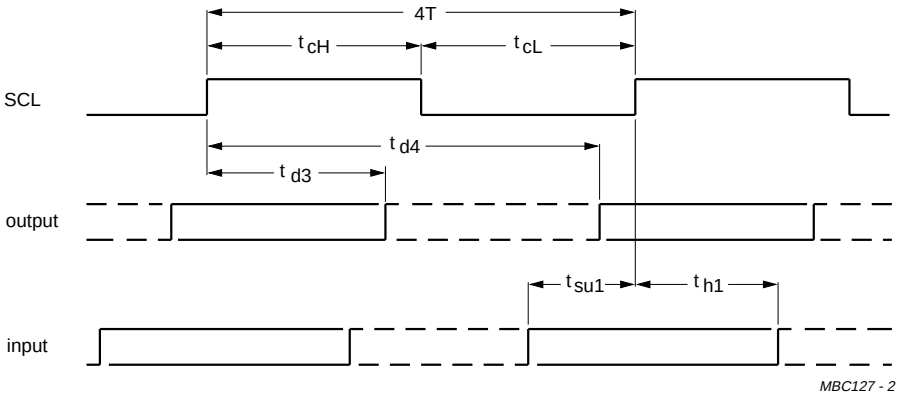
Input frequency (f_i) must be provided as system clock. This frequency is used by the interfaces with the SAA2002.

The frequency of the SWS signal (pin 31) is equal to the sample frequency (f_s). Bit clock SCL (pin 32) is 64 times f_s; thus each SWS period contains 64 data bits, 48 of which are actually used in data transfer. The half period when SWS is logic 0 is used to transfer left-channel information, when SWS is logic 1 transfer of right-channel data is allowed.

The 24-bit samples are transferred with the most significant bit first. This bit is transferred during the bit clock period, one bit time after the change in SWS.

FSYNC signal is provided for the purposes of synchronization and indicates the portion of the SWS period during which the samples of sub-band 0 are transferred.

The relationship between FSYNC and the SWS is logic 0 data transfer period is shown in Fig.7



OUTPUT applies to FDAF and FDAC in the output mode.

INPUT applies to FDAF and FDAC in the input mode, SWS and FSYNC.

T = 1 f_s 256 cycle time.

$t_{Hc} \geq T + 35$ ns minimum HIGH time SCL.

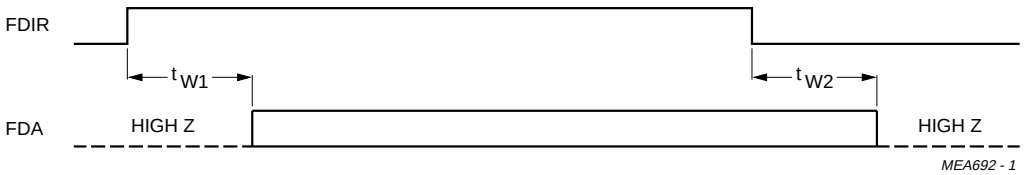
$t_{Lc} \geq T + 35$ ns minimum LOW time SCL.

$t_{d3} \geq 2T - 10$ ns hold time output after SCL HIGH.

$t_{d4} \leq 3T + 60$ ns delay time output after SCL HIGH.

$t_{su1} \geq 20$ ns set-up time input before SCL HIGH.

$t_{h1} \geq T + 35$ ns hold time input after SCL HIGH.



$t_{W1} \geq 3T$ minimum time high impedance to FDA enabled.

$t_{W2} \geq 2T + 35$ ns maximum time FDA enabled to high impedance.

Fig.8 Filtered-I^2S interface timing.

Microcontroller Interface

Two microcontroller interfaces are provided; one for connection to the microcontroller interface of the SAA2002, the other to connect to the system controller. Information is conveyed via the SAA2012 which executes monitoring and extracts signals (e.g. settings and synchronization) essential to its operation. It also sends allocation information to the SAA2002. However, the SAA2012 does not monitor the external settings bits from the microcontroller (see “Extended settings (LTCNT1(C) = LTCNT0(C) = logic 0)”).

Table 3 SAA2012 Interface with microcontroller.

SIGNAL	TYPE	DESCRIPTION
LTCLK	input	bit clock
LTDATA	bi-directional	data
LTCNT0	input	control line 0
LTCNT1	input	control line 1
LTENA	input	enable

The SAA2012 is a slave on this interface which is active only when the enable signal LTENA (pin 3) is logic 1. This allows connection of this interface to other devices. Only the enable signal is not common to all devices.

Table 4 SAA2012 Interface with SAA2002.

SIGNAL	TYPE	DESCRIPTION
LTCLK	output	bit clock
LTDATAC	bi-directional	data
LTCNT0C	output	control line 0
LTCNT1C	output	control line 1
LTENC	output	enable

The SAA2012 is master on this interface and provides all signals with the exception of the data in the instance of status transfer from SAA2002 to SAA2012.

Information conveyed via these interfaces is transferred in 8 or 16-bit serial units with the type of information designated by the control lines LTCNT1C and LTCNT0C.

A transfer of information begins when the master sets the control lines for the required action. It then sets the LTENA/C line to logic 1. Once this signal is established the slave determines the kind of action required and prepares for the transfer of data.

When the master supplies the LTCLK/C signals, data is transferred either to or from the slave in units of 8-bits; the least significant bit (LSB) is always transferred first. A transfer of 16-bits is made in two, 8-bit units with the most significant 8-bit (MSB) unit first. In between the two 8-bit units the LTENA/C signals remain logic 1.

An example of information transfer via SAA2012 interfaces is shown in Fig.9.

Table 5 SAA2012 interface control lines functions.

LTCNT1(C)	LTCNT0(C)	MODE	FROM	TO	TRANSFER OF
0	0	extended settings	microcontroller	SAA2002	8 bits
0	1	allocation; note 1	SAA2012	SAA2002	16/48 $\times$ 16 bits
1	0	settings	microcontroller	SAA2002	16 bits
1	1	status	codec	microcontroller	8 or 16 bits

Note

1. This mode only on the interface between SAA2012 and SAA2002.
   If SCALE = logic 1 then 16 $\times$ 16-bits.
   If SCALE = logic 0 then 48 $\times$ 16-bits.

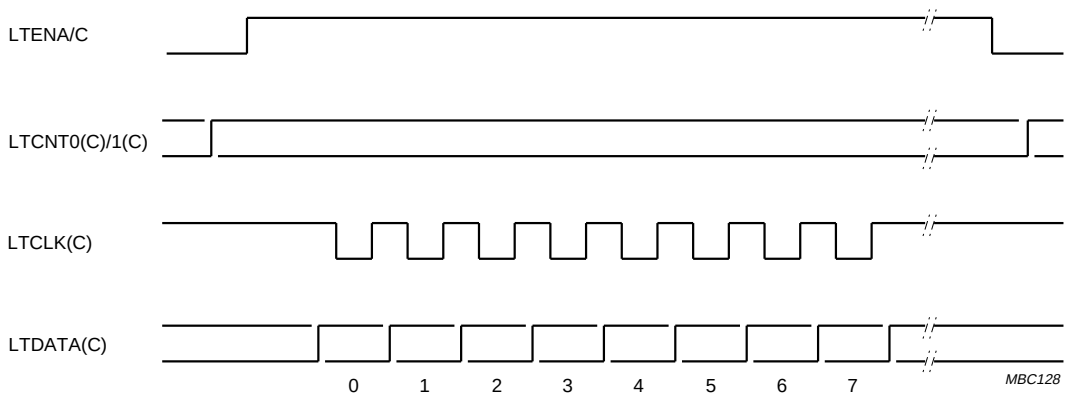
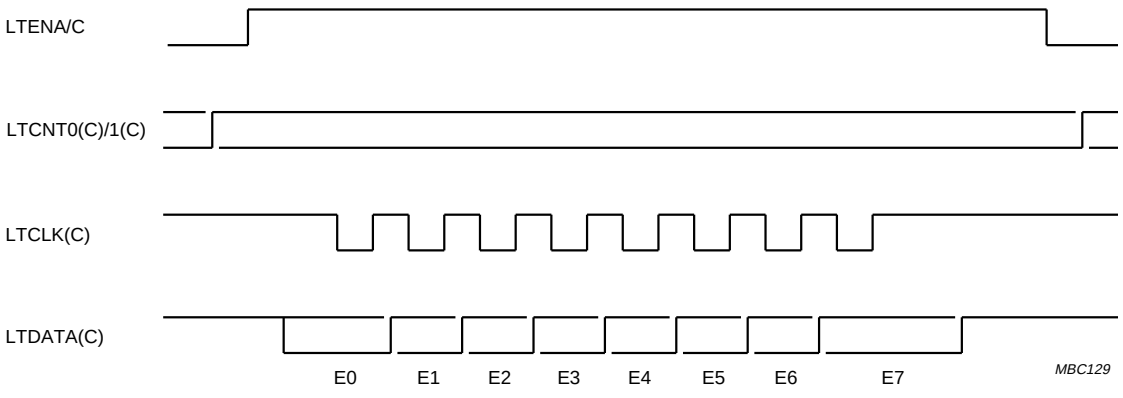


Fig.9 Example of information transfer via SAA2012 interfaces.



Refer to the SAA2002 description for the meaning of these bits as they pass SAA2012 unchanged.

Fig.10 Extended settings LTCNT1(C) and LTCNT0(C).

Extended settings (LTCNT1(C) = LTCNT0(C) = logic 0)

Eight information bits, generated by the microcontroller, are transferred in this mode. The SAA2012 will transfer these bits to the SAA2002 as soon as possible but does not monitor this information.

The relationship of the extended settings is shown in Fig.10.

Allocation and SCALING information (LTCNT1(C) = logic 0, LTCNT0(C) = logic 1)

In the encoding mode (FDIR = logic 0) the SAA2012 will transfer allocation information to the SAA2002. This will occur once for every SAA2002 frame.

The information will consist of 16 transfers each of 16-bits. To synchronize the SAA2012 operation with that of the SAA2002, following the first 16-bit transfer of allocation data the SAA2012 checks the SAA2002 status to ensure it is ready to receive the remainder of the allocation information. Transfer of allocation data is completed by sending settings. Between 16-bit transfers the LTENC line returns to logic 0 as shown in Fig.11.

The order in which the bits occur on the interface during allocation information transfer is shown in Fig.12.

The 4-bit sub-band allocation unit contains the number of bits allocated to the sub-band minus 1. A value of 0000 indicates no bits allocated to that sub-band.

With stereo encoding, left and right channels are designated **L** and **R**. This changes to channels I or II for 2-channel mono mode. If SCALE = logic 0 the transfer of allocation information will be followed by the transfer of scale factors. Each 16-bit transfer contains two scale factor indices.

The following algorithm shows the process of information transfer:

```
COUNT = 0
SEND ALLOCATION (COUNT)
REPEAT
READ STATUS
UNTIL
READY-TO-RECEIVE
FOR COUNT = 1 to 15
DO
SEND ALLOCATION (COUNT)
SEND SETTINGS
IF SCALE = 0
THEN
FOR COUNT = 0 to 31
DO
SEND SCALE FACTORS (COUNT)
```

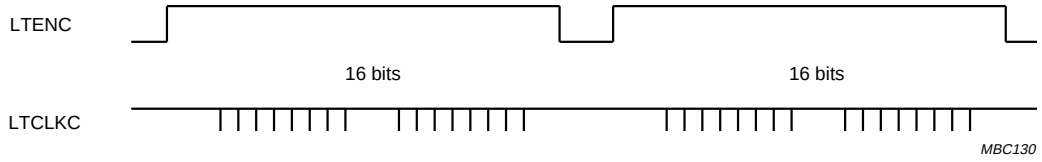


Fig.11 LTENC behaviour for 16-bit transfers.

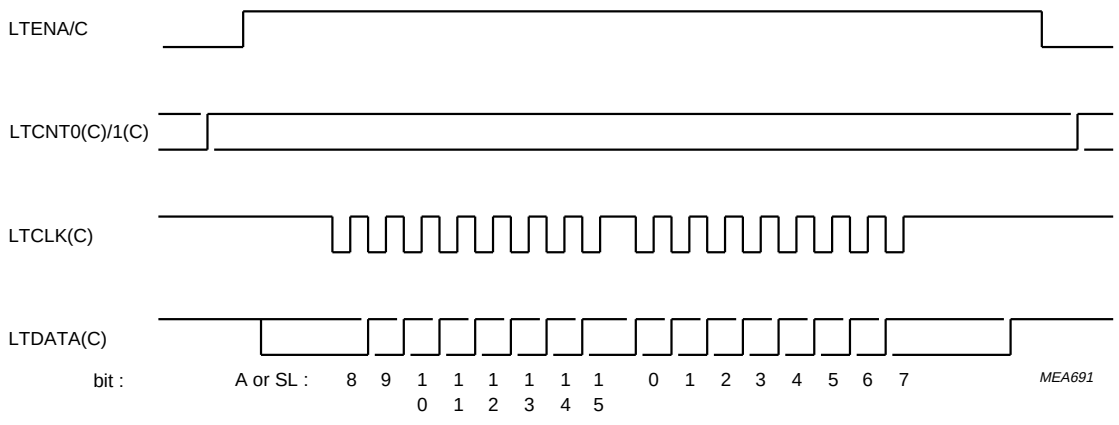


Fig.12 The order of interface bits during allocation information transfer.

Table 6

BITS				CHANNEL	SUB-BAND
MSB			LSB		
A15	A14	A13	A12	L	2 × COUNT
A11	A10	A9	A8	R	2 × COUNT
A7	A6	A5	A4	L	(2 × COUNT) + 1
A3	A2	A1	A0	R	(2 × COUNT) + 1

Table 7

BITS			CHANNEL	CONTENTS
MSB		LSB		
SL15	SL14	–	–	00
SL13	SL12 - SL11 - SL10 - SL9	SL8	L	SCALE FACTOR (COUNT)
SL7	SL6	–	–	00
SL5	SL4 - SL3 - SL2 - SL1	SL0	R	SCALE FACTOR (COUNT)

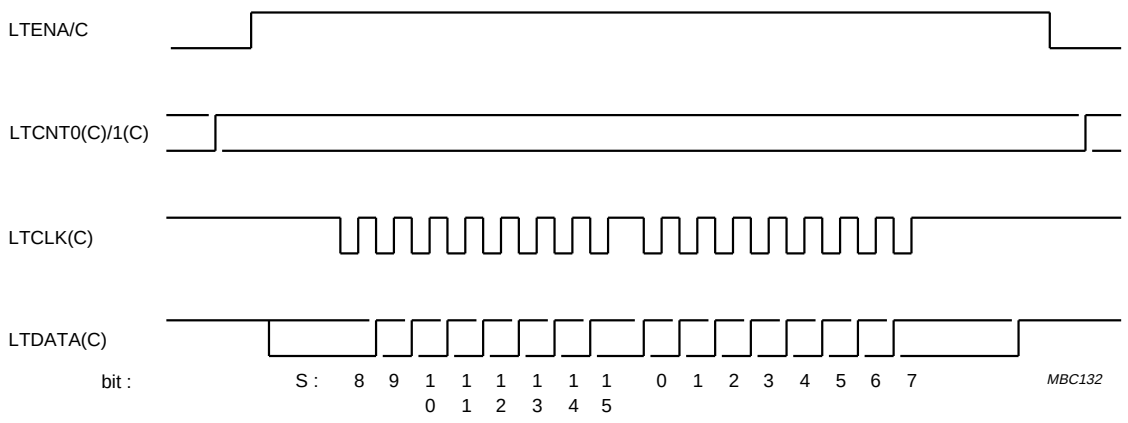


Fig.13 The order of bits on the interface.

Settings (LTCNT1(C) = logic 1, LTCNT0(C) = logic 0)

Without using the information, the SAA2012 transfers microcontroller settings to the SAA2002.

Prior to sending settings, the microcontroller would utilize the SAA2012 status readings to ensure its readiness to accept and convey the data.

Following reception of the settings the SAA2012 will cause the ready-to-receive bit to be logic 0 until the settings have been sent to the SAA2002. The microcontroller can only send this data when this bit is logic 1.

The order of bits on the interface is shown in Fig.13.

Table 8 Microprocessor settings applied to the SAA2002 via the SAA2012.

BITS				NAME	FUNCTION	VALID IN
MSB			LSB			
S15	S14	S13	S12	bit-rate index	bit-rate indication	encode
S11	–	–	S10	sample frequency	44.1, 48 or 32 kHz indication	encode
S9	–	–	–	DECODE	1 = decode; 0 = encode	encode/decode
S8	–	–	–	external 256f_s	1 = external; 0 = internal	encode/decode
S7	–	–	–	2-channel mono	1 = (2-channel mono); 0 = stereo	encode
S6	–	–	–	MUTESFC	1 = mute; 0 = no mute	encode/decode
S5	–	–	–	not used	–	encode/decode
S4	–	–	–	CH I	1 = channel I; 0 = channel II	decode
S3	–	–	S2	Tr0 - Tr1	transparent bits	encode
S1	–	–	S0	EMPHASIS	emphasis indication	encode

Status (LTCNT1(C) = LTCNT0(C) = logic 1)

The SAA2002 and SAA2012 operation may be checked by reading these bits. All, except the ready-to-receive bits, are generated by the SAA2002.

The bit rate index shows the bit rate of the sub-band signal in units of 32 kbits/s. The SAA2012 is designed for bit rates of 384, 256, 192 and 128 kbits/s only.

Table 9 Order of SAA2002 bits as they appear on the interface (see also Fig.14).

BITS				NAME	FUNCTION	VALID IN
MSB			LSB			
T15	T14	T13	T12	bitrate index	bit-rate indication	encode/decode
T11	–	–	T10	sample frequency	44.1, 48 or 32 kHz indication	encode/decode
T9	–	–	–	ready-to-receive S	1 = ready; 0 = not ready	encode/decode
T8	–	–	–	ready-to-receive E	1 = ready; 0 = not ready	encode/decode
T7	–	–	T6	MODE	sub-band signal mode ID	encode/decode
T5	–	–	–	SYNC	synchronization indicator	decode
T4	–	–	–	CLKOK	1 = OK; 0 = not OK	encode/decode
T3	–	–	T2	Tr0 - Tr1	transparent bits	encode/decode
T1	–	–	T0	EMPHASIS	emphasis indication	encode/decode

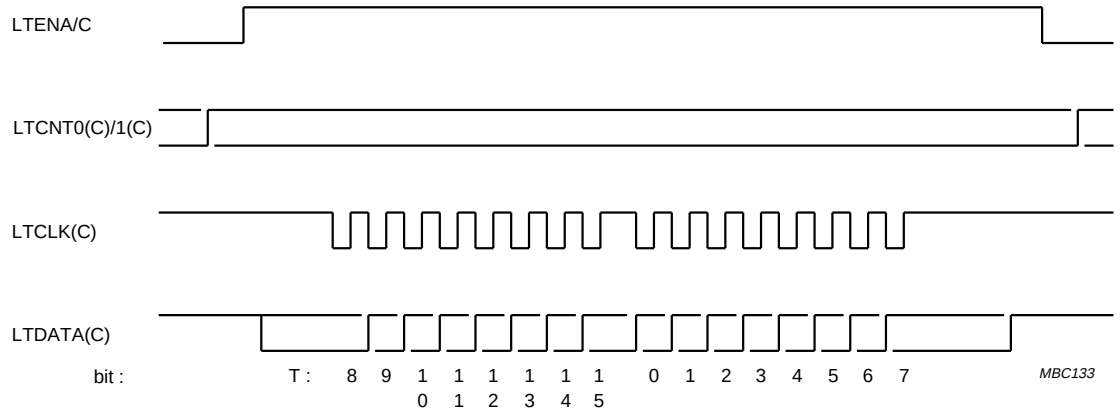


Fig.14 The order of appearance of bits on the interface.

Table 10 Sample frequency indication.

MSB	LSB	f_s	REMARK
0	0	44.1 kHz	default value
0	1	48 kHz	
1	0	32 kHz	
1	1	–	do not use

Table 11 MODE indication.

MSB	LSB	MODE	OUTPUT
0	0	stereo	L and R
0	1	joint stereo	L and R
1	0	2-channel mono	I or II as selected
1	1	1-channel mono	mono, no selection

With EMPHASIS activated (S1 = T1 = logic 0 and S0 = T0 = logic 1) only bit rates 384 and 256 kbits/s can be used.

A ready-to-receive **S** or **E** indicates whether or not the SAA2012 can receive new settings or extended settings respectively from the microcontroller and should be checked prior to sending new information.

The SAA2012 can only be used to encode stereo (mode 00) signals and 2-channel mono (mode 10) signals.

During the decoding mode this bit indicates if the operation of the SAA2002 is in synchronization with the PASC signal. If not the SAA2002 cannot perform the decoding.

CLKOK indicates whether or not the f_{s256} clock corresponds with the specified sample frequency.

EMPHASIS indication may be used to apply correct de-emphasis. During the encoding 50/15 μs mode the SAA2012 will correct the calculated allocation if emphasis is applied for a 44.1 kHz sampling frequency.

Frequency Range Limitation

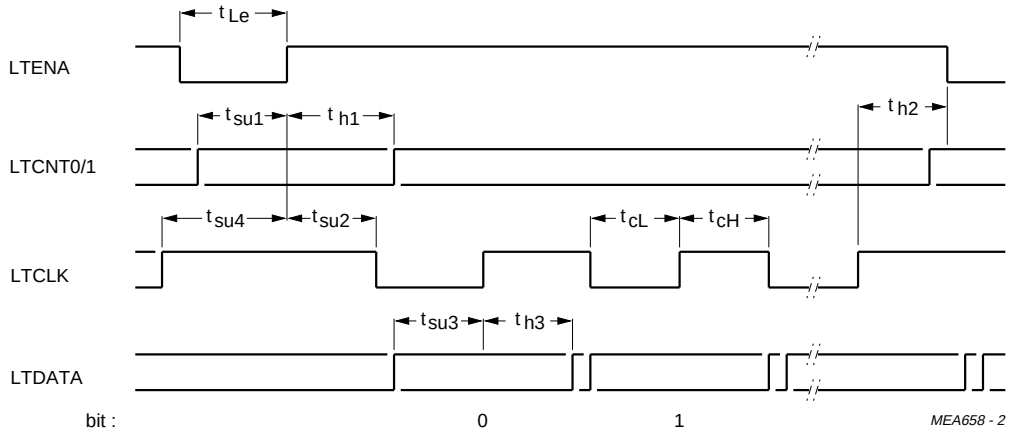
In encode mode the frequency range will be limited at lower rates. This is implemented by making the samples of higher frequency sub-bands equal to 0 before the allocation calculation. This automatically ensures that these sub-bands do not get any bits allocated.

Table 12 shows the sub-bands affected and the resulting frequency range.

The transfer of either 8-bits or 16-bits is permitted for the transfer of status information. When only 8-bits are transferred, these will always form the first byte and may be used in checking the ready-to-receive bit.

Table 12 The sub-bands affected and the resulting frequency range.

BIT RATE	f_s	SUB-BANDS SET TO LOGIC 0	FREQUENCY
256 kbits/s	48 kHz	29, 30, 31	>21750 Hz
192 kbits/s	48 kHz	20, 21, 22, ..., 31	>15000 Hz
	44.1 kHz	22, 23, 24, ..., 31	>15159 Hz
128 kbits/s	48 kHz	12, 13, 14, ..., 31	>9000 Hz
	44.1 kHz	13, 14, 15, ..., 31	>8957 Hz
	32 kHz	20, 21, 22, ..., 31	>10000 Hz



t_{Le} > 210 ns minimum LOW time LTENA prior to transfer.

t_{su1} > 50 ns set-up time LTCNT0, 1 before LTENA HIGH.

t_{h1} > 210 ns hold time LTCNT0/1 after LTENA HIGH.

t_{su2} > 210 ns set-up time LTENA before LTCLK LOW.

t_{h2} > 210 ns hold time LTENA after LTCLK HIGH.

t_{cL} > 210 ns minimum LOW time LTCLK.

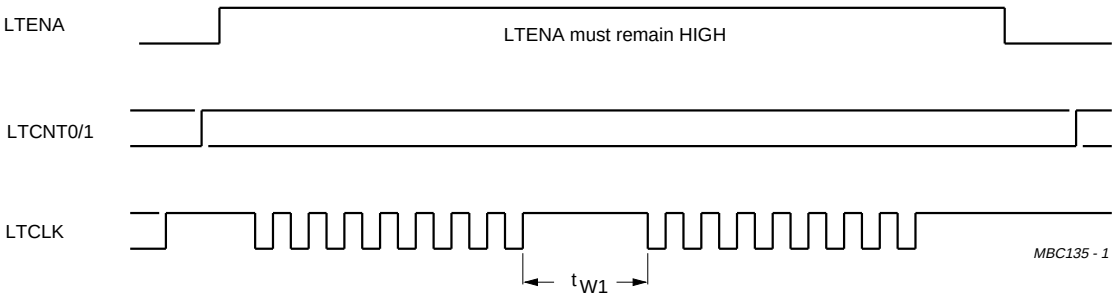
t_{cH} > 210 ns minimum HIGH time LTCLK.

t_{su3} > 210 ns set-up time LTDATA before LTCLK HIGH.

t_{h3} > 50 ns hold time LTDATA after LTCLK HIGH.

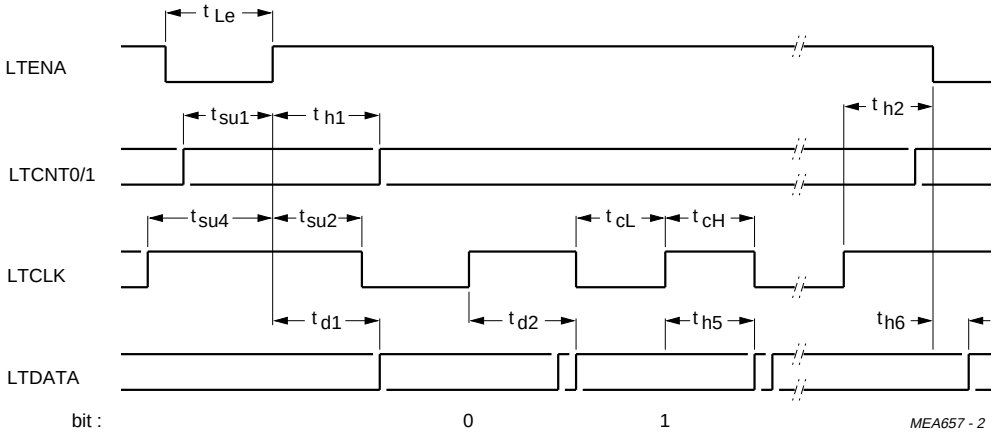
t_{su4} > 210 ns set-up time LTCLK before LTENA HIGH.

Fig.15 Microcontroller to SAA2012 timing.



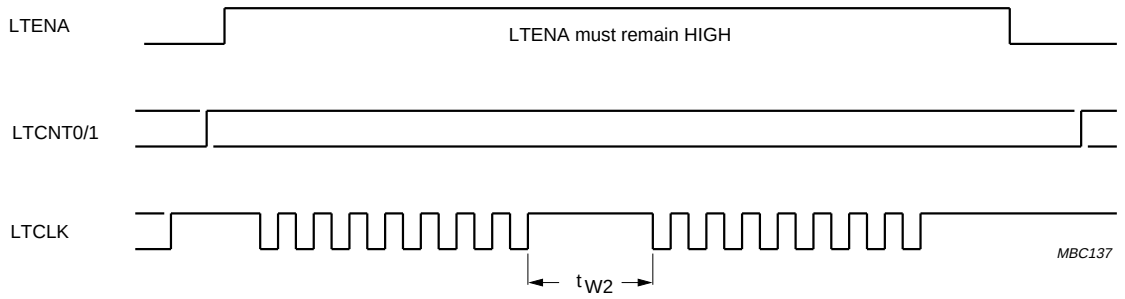
t_{W1} > 550 ns minimum time between two 8-bit transfers.

Fig.16 16-bit transfers.



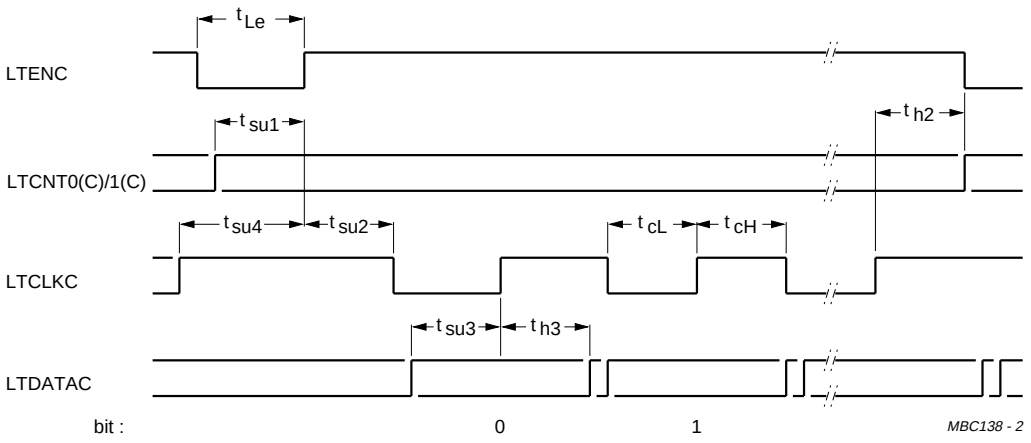
t_{Le} > 210 ns minimum LOW time LTENA prior to transfer.
t_{su1} > 50 ns set-up time LTCNT0/1 before LTENA HIGH.
t_{h1} > 210 ns hold time LTCNT0(C)/1(C) after LTENA HIGH.
t_{su2} > 210 ns set-up time LTENA before LTCLK LOW.
t_{h2} > 210 ns hold time LTENA before LTCLK HIGH.
t_{cL} > 210 ns minimum LOW time LTCLK.
t_{cH} > 210 ns minimum HIGH time LTCLK.
t_{d1} < 385 ns maximum delay LTDATA after LTENA HIGH.
t_{d2} < 385 ns maximum delay LTDATA after LTCLK HIGH.
t_{h5} > 145 ns hold time LTDATA after LTCLK HIGH.
t_{su4} > 210 ns set-up time LTCLK before LTENA HIGH.
t_{h6} > 0 ns hold time LTDATA after LTENA LOW.

Fig.17 SAA2012 to microcontroller timing.



t_{W2} > 550 ns minimum time between two 8-bit transfers.

Fig.18 16-bit transfers.



t_{Le} > 400 ns minimum LOW time LTENA prior to transfer.

t_{su1} > 400 ns set-up time LTCNT0(C)/1(C) before LTENC HIGH.

t_{su2} > 200 ns set-up time LTENC before LTCLKC LOW.

t_{h2} > 400 ns hold time LTENC before LTCLK HIGH.

t_{cL} > 210 ns minimum LOW time LTCLKC.

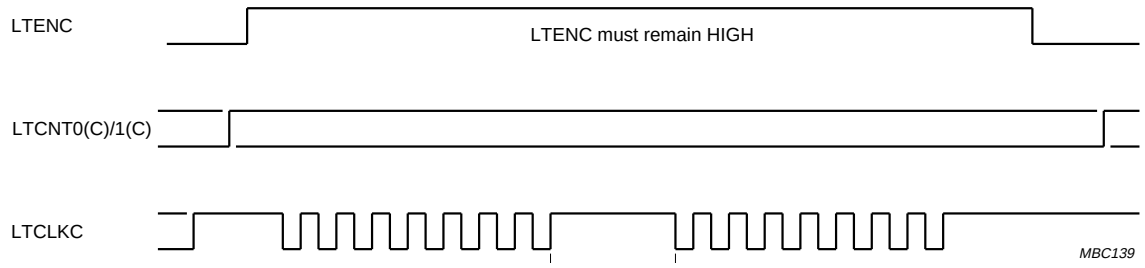
t_{cH} > 210 ns minimum HIGH time LTCLKC.

t_{su3} > 210 ns set-up time LTDATAC before LTCLKC HIGH.

t_{h3} > 160 ns hold time LTDATAC after LTCLKC HIGH.

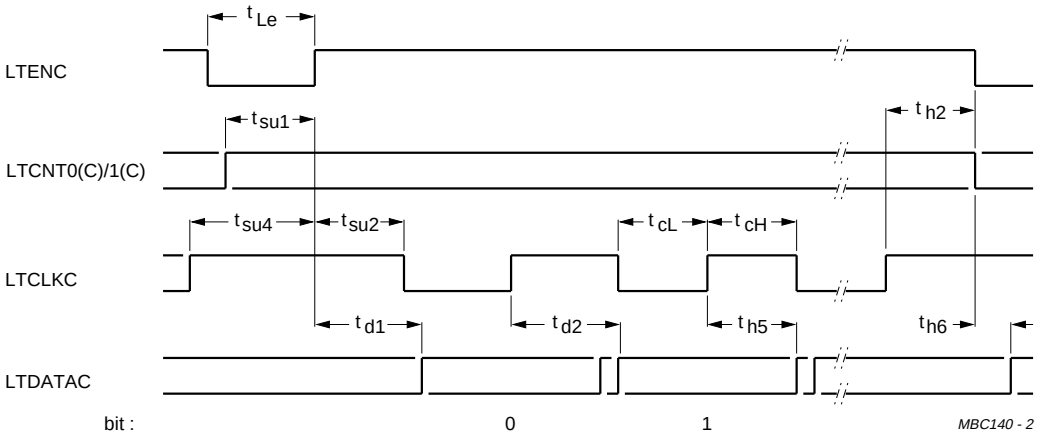
t_{su4} > 900 ns set-up time LTCLKC before LTENC HIGH.

Fig.19 SAA2012 to SAA2002 timing.



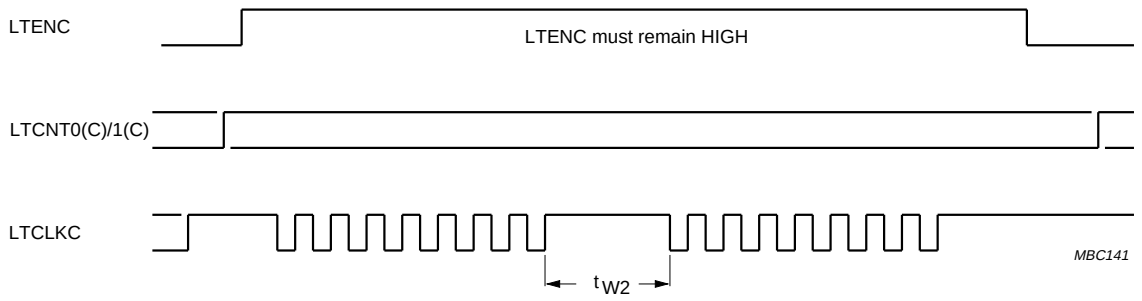
t_{W2} > 600 ns minimum time between two 8-bit transfers.

Fig.20 16-bit transfers.



t_{Le} > 400 ns minimum LOW time LTENC prior to transfer.
t_{su1} > 400 ns set-up time LTCNT0(C)/1(C) before LTENC HIGH.
t_{su2} > 200 ns set-up time LTENC before LTCLKC LOW.
t_{h2} > 400 ns hold time LTENC before LTCLKC HIGH.
t_{cL} > 210 ns minimum LOW time LTCLKC.
t_{cH} > 210 ns minimum HIGH time LTCLKC.
t_{d1} < 300 ns maximum delay LTDATAC after LTENC HIGH.
t_{d2} < 300 ns maximum delay LTDATAC after LTCLKC HIGH.
t_{su4} > 900 ns set-up time LTCLKC before LTENC HIGH.
t_{h5} > 160 ns hold time, after LTCLKC HIGH.
t_{h6} > 0 ns hold time LTDATAC after LTENC LOW.

Fig.21 SAA2002 to SAA2012 timing.



t_{W2} > 600 ns minimum time between two 8-bit transfers.

Fig.22 16-bit transfers.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	+6.5	V
V_I	input voltage	note 1	–0.5	V_{DD} + 0.5	V
I_{DD}	supply current		–	100	mA
I_I	input current		–	±10	mA
I_O	output current		–	±40	mA
P_{tot}	total power dissipation		–	550	mW
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es1}	electrostatic handling	note 2	–1500	+1500	V
V_{es2}	electrostatic handling	note 3	–70	+70	V

Notes

1. Input voltage should not exceed 6.5 V unless otherwise specified.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

DC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.8	5.0	5.5	V
I_{DD}	operating supply current	V_{DD} = 3.8 V	–	15	17	mA
		V_{DD} = 5 V	–	23	25	mA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_I	input current		–	–	10	µA
Outputs						
V_{OL}	LOW level output voltage	note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	note 1	V_{DD} – 0.5	–	–	V
3-state outputs						
I_{OZ}	3-state OFF state current	V_I = 0 to 5.5 V	–	–	10	µA

Note

1. Maximum load current for LTDATA, LTCNT1C, LTCNT0C, LTENC, LTCLKC, TEST1, TEST2, FDAC and FDAF = 2 mA; for LTDATAC = 3 mA.

AC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

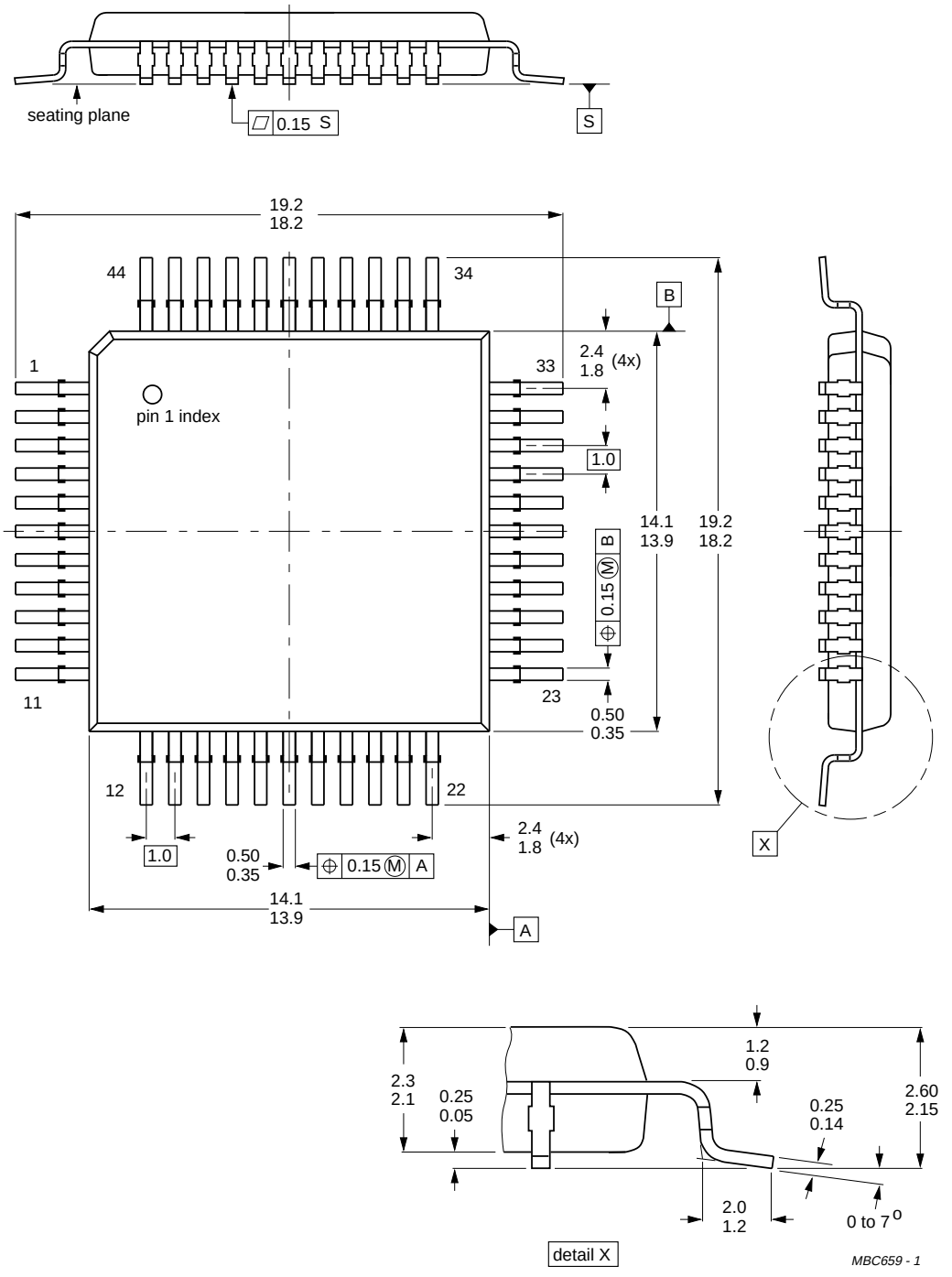
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock CLK24						
f_s	sample frequency		23	24.576	26	MHz
Clock FS256						
f_s	sample frequency		–	–	13	MHz
Inputs FSYNC, SWS, LTCNT1, LTCNT0, LTENA, LTCLK, LTDATA, LTDATAC, FDAF, FDAC, SCL and SWS						
C_I	input capacitance		–	–	10	pF
INPUT SET-UP TIME						
t_{su}	set-up time of inputs referenced to CLK24 rising edge	note 1	15	–	–	ns
t_{su}	set-up time of inputs referenced to $256f_s$ rising edge	note 2	15	–	–	ns
INPUT HOLD TIME						
t_h	hold time of inputs referenced to CLK24 rising edge	note 1	20	–	–	ns
t_h	hold time of inputs referenced to $256f_s$ rising edge	note 2	10	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs LTDATA, LTDATAC, LTCNT1C, LTCNT0C, LTENC, LTCLKC, FDAF and FDAC						
C_o	output capacitance		–	–	10	pF
t_d	output delay referenced to CLK24 rising edge	C_L = 25 pF; note 3	–	–	45	ns
t_d	output delay referenced to 256f_s rising edge	C_L = 25 pF; note 4	–	–	30	ns
3-state outputs						
t_{PHZ}	disable time HIGH-to-Z	C_L = 25 pF	–	–	65	ns
t_{PLZ}	disable time LOW-to-Z	C_L = 25 pF	–	–	65	ns
t_{PZH}	enable time Z-to-HIGH	C_L = 25 pF	–	–	65	ns
t_{PZL}	enable time Z-to-LOW	C_L = 25 pF	–	–	65	ns

Notes

1. Inputs FSYNC, SWS, LTCNT1, LTCNT0, LTENA, LTCLK, LTDATA and LTDATAC.
2. Inputs FDAF, FDAC, SCL and SWS.
3. Outputs LTDATA, LTDATAC, LTCNT1C, LTCNT0C, LTENC and LTCLK.
4. Outputs FDAF and FDAC.

PACKAGE OUTLINE



Dimensions in mm.

Fig.23 44-lead quad flat-pack; plastic (SOT205AG).

SOLDERING

Plastic quad flat-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress rating only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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