DATA SHEET

SAA7207H
Reed Solomon decoder IC

Product specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

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Reed Solomon decoder IC SAA7207H

FEATURES

- (204, 188 and 17) Digital Video Broadcasting (DVB) compliant Reed Solomon (RS) codes
- Automatic synchronization of bytes, blocks and frame
- Convolutional de-interleaving (I = 12)
- Energy dispersal de-randomizing
- Contained in a 44-pin quad flat package
- I²C-bus interface
- 6 quasi-bidirectional ports
- Boundary scan facility.

APPLICATIONS

- Forward Error Correction (FEC) for digital TV distribution according to the DVB standard.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	operational supply voltage	4.75	5.00	5.25	V
$I_{DD(tot)}$	total supply current	–	65	–	mA
T_{CLK}	input clock period	–	31.5	–	ns

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7207H/C1	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM

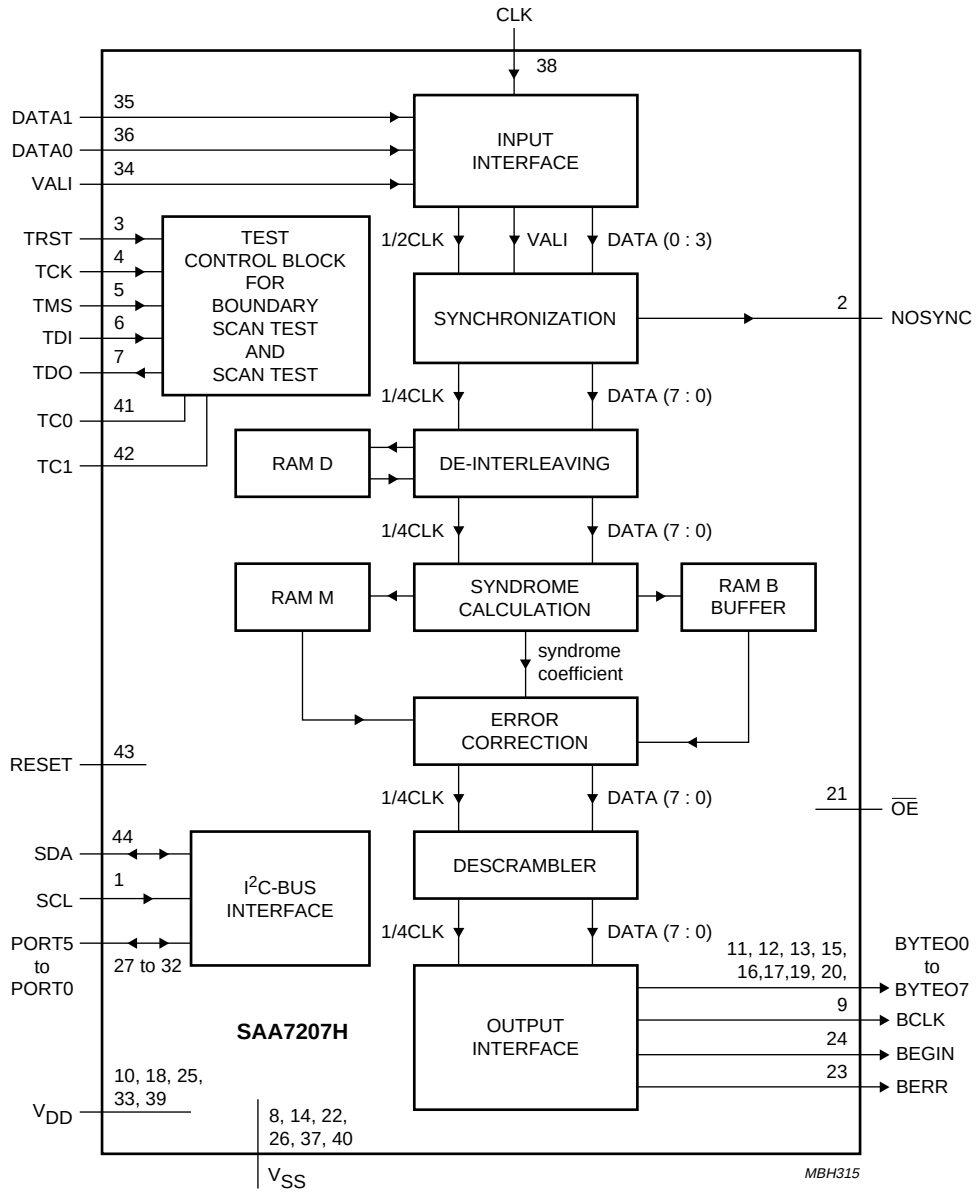


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
SCL	1	I	serial clock input (I^2C-bus)
NOSYNC	2	O	not synchronized output (1 = not synchronized)
TRST	3	I	boundary scan test reset (0 = active)
TCK	4	I	boundary scan test clock
TMS	5	I	boundary scan test mode select (1 = BST select)
TDI	6	I	boundary scan test data input
TDO	7	O	boundary scan test data output
V_{SS}	8	–	ground
BCLK	9	O*(1)	byte clock output
V_{DD}	10	–	positive supply voltage
BYTEO0	11	O*(1)	output data byte 0 (LSB)
BYTEO1	12	O*(1)	output data byte 1
BYTEO2	13	O*(1)	output data byte 2
V_{SS}	14	–	ground
BYTEO3	15	O*(1)	output data byte 3
BYTEO4	16	O*(1)	output data byte 4
BYTEO5	17	O*(1)	output data byte 5
V_{DD}	18	–	positive supply voltage
BYTEO6	19	O*(1)	output data byte 6
BYTEO7	20	O*(1)	output data byte 7 (MSB)
$\overline{OE}$	21	I	output enable not (active LOW; 1 = O*(1) high impedance)
V_{SS}	22	–	ground
BERR	23	O*(1)	block error output (1 = uncorrectable block)
BEGIN	24	O*(1)	begin of block output (1st byte of block is output)
V_{DD}	25	–	positive supply voltage
V_{SS}	26	–	ground
PORT5	27	I/O	quasi-bidirectional port 5
PORT4	28	I/O	quasi-bidirectional port 4
PORT3	29	I/O	quasi-bidirectional port 3
PORT2	30	I/O	quasi-bidirectional port 2
PORT1	31	I/O	quasi-bidirectional port 1
PORT0	32	I/O	quasi-bidirectional port 0
V_{DD}	33	–	positive supply voltage
VALI	34	I	valid input (1 = data is valid)
DATA1	35	I	input data 1 (MSB)
DATA0	36	I	input data 0 (LSB)
V_{SS}	37	–	ground
CLK	38	I	master clock input (also acting as input data clock)
V_{DD}	39	–	positive supply voltage
V_{SS}	40	–	ground

SYMBOL	PIN	I/O	DESCRIPTION
TC0	41	I	test mode control input 0 (0 = application mode)
TC1	42	I	test mode control input 1 (0 = application mode)
RESET	43	I	master reset input (1 = active)
SDA	44	I/O	bidirectional serial data port (I^2C-bus)

Note

1. When $\overline{OE}$ is active (pin 21 = HIGH), all O* outputs become high impedance.

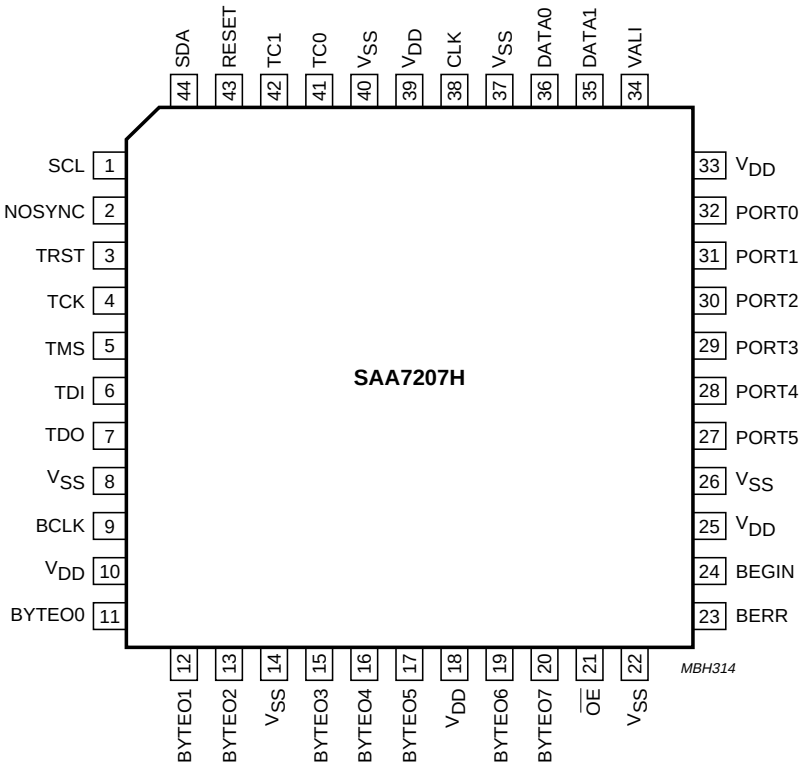


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Input interface (see Fig.3)

The received input data stream is a sequence which is interpreted as a stream of bytes. The bits are assumed to be non-byte aligned and sent in MSB to LSB order. New data may be present at the input pins on each rising edge of the master clock input (CLK). Valid data is indicated by VALI = HIGH. When VALI = LOW the data is not valid and will be neglected. There are no limitations imposed on valid/non-valid sequences. The Quadrature Amplitude Modulation (QAM) of the input data is given in Table 1.

Table 1 Quadrature amplitude modulation; note 1

SLOT	QUADRATURE AMPLITUDE MODULATION(2)														
	256 QAM			64 QAM			32 QAM			16 QAM			4 QAM		
	DATA1	DATA0	VALI	DATA1	DATA0	VALI	DATA1	DATA0	VALI	DATA1	DATA0	VALI	DATA1	DATA0	VALI
0	S_{n-1} [7]	S_{n-1} [6]	1	S_{n-1} [5]	S_{n-1} [4]	1	S_{n-1} [4]	S_{n-1} [3]	1	S_{n-1} [3]	S_{n-1} [2]	1	S_{n-1} [1]	S_{n-1} [0]	1
1	S_{n-1} [5]	S_{n-1} [4]	1	S_{n-1} [3]	S_{n-1} [2]	1	S_{n-1} [2]	S_{n-1} [1]	1	S_{n-1} [1]	S_{n-1} [0]	1	X	X	0
2	S_{n-1} [3]	S_{n-1} [2]	1	S_{n-1} [1]	S_{n-1} [0]	1	X	X	0	X	X	0	X	X	0
3	S_{n-1} [1]	S_{n-1} [0]	1	X	X	0	X	X	0	X	X	0	X	X	0
4	S_n [7]	S_n [6]	1	S_n [5]	S_n [4]	1	S_{n-1} [0]	S_n [4]	1	S_n [3]	S_n [2]	1	S_n [1]	S_n [0]	1
5	S_n [5]	S_n [4]	1	S_n [3]	S_n [2]	1	S_n [3]	S_n [2]	1	S_n [1]	S_n [0]	1	X	X	0
6	S_n [3]	S_n [2]	1	S_n [1]	S_n [0]	1	S_n [1]	S_n [0]	1	X	X	0	X	X	0
7	S_n [1]	S_n [0]	1	X	X	0	X	X	0	X	X	0	X	X	0

Notes

1. X = don’t care.
2. The numbers given in parenthesis refer to the bit numbers.

Synchronization (see Fig.4)

The input stream is interpreted as a stream of bytes consisting of blocks which;

- Have a fixed 204 byte length
- Start with 1 synchronization byte.

Both de-interleaving and Reed Solomon decoding are based on this block structure. Energy dispersal descrambling is based on frames consisting of 8 blocks. The first block of a frame has a sync byte of B8H, and the remaining 7 blocks have a sync byte of 47H.

Consequently, there are 2 synchronization processes:

1. Synchronization process 1: handles byte alignment and block synchronization. It is based on a state machine running from state 0 (out of sync) to state 6 (fully synchronized).
2. Synchronization process 2: handles frame synchronization for de-scrambling. It is based on the detection of a B8H sync byte (after Reed Solomon correction). Whenever such a sync byte is detected at the beginning of a correct/corrected block, a free running 'block of frame counter' is synchronized/resynchronized.

With reference to note 2 in Fig 4, BERR is asserted at the beginning of each new RS word (rising edge of BEGIN). NOSYNC = 0 when 6 consecutive sync bytes have been detected. BERR = 0 when the beginning of a frame has been detected (de-scrambler lock) and not more than 8 bytes were wrong. When more than 8 bytes are wrong, the BERR stays at logic 1 during the length of the word.

De-interleaving (see Fig.5)

Input data is interleaved, conforming a convolutional interleaving scheme. If we describe a Reed Solomon block as a 0 to 203 one dimensional byte array then;

- Interleaving means that byte N of each block (N = 0 to 203) has been delayed by exactly D1 blocks (D1 = N mod 12)
- So to de-interleave byte N of each block (N = 0 to 203) has to be delayed by D2 blocks [D2 = (203-N) mod 12].

Reed Solomon decoder

The IC contains a high throughput Reed Solomon decoder consisting of three fully pipelined hardware units that execute finite field computations on de-interleaved input data blocks with lengths of 204 bytes.

Each of the units is dedicated to one of the following decoder algorithm stages;

1. Power sum polynomial (syndrome) calculation
2. Execution of the Euclidean algorithm to find the error locator polynomial and the error evaluator polynomial
3. Execution of a Chien search to find the roots of the error locator polynomial. For each root the error value is calculated (Forney algorithm) and stored in memory.

Code generator polynomial:
g (X) = (X + L0), (X + L1), (X + L2) to (X + L15)
where L = 02H

Field generator polynomial:
$p(X) = X8 + X4 + X3 + X2 + 1$

Error correction

The error correction unit corrects the errors as calculated by the Reed Solomon unit if, and only if, they are correctable. If not, the block is sent to the output unmodified (i.e. as received). If 'Transport Error Indicator' (TEI = first bit after sync byte) modification is enabled the error flag is set in all uncorrectable blocks.

In all cases the 16 parity bytes are stripped (the output is set to zero; BCLK is stopped) from the block reducing it to 188 bytes length.

De-randomizing

The energy dispersal descrambling algorithm is based on a 15 bit shift register which is initialised upon the arrival of the Least Significant Bit (LSB) of the first byte of each frame. De-scrambling is disabled for all sync bytes.

Output interface (see Fig.6)

The output data stream consists of a sequence of bytes (BYTEO 7 is the MSB). A new byte is present at the output pins at each rising edge of the byte clock. The BEGIN output is asserted for the first byte of a block and negated elsewhere. The BERR output is asserted during uncorrectable and/or unsynchronized blocks and negated during correct/corrected blocks.

Mode of operation

Table 2 Mode of operation for boundary scan test

PIN	INTERNAL CONNECTION	APPLICATION MODE (REED SOLOMON)	BOUNDARY SCAN TEST
TC0	pull-down	logic 0 or open-circuit	logic 0 or open-circuit
TC1	pull-down	logic 0 or open-circuit	logic 0 or open-circuit
TRST	pull-up	logic 0[1]	logic 1 or open-circuit
TMS	pull-up	open-circuit	input
TCK	none	open-circuit	input
TDI	pull-up	open-circuit	input

Note

1. The safest way to deactivate the Boundary Scan Test (BST) circuitry is to set TRST to logic 0.

Control, monitoring and extension port interface

An I^2C-bus slave transmitter interface is included to provide the possibilities for a host to send control data and/or read monitoring information. For details of the interface protocol and timing on the I^2C-bus see *"The I^2C-bus and how to use it"*; 12NC number 9398 393 40011.

Table 3 Slave address

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	1	0	1	0	0	1	X[1]

Note

1. When X = 1 = read; when X = 0 = write.

Table 4 Write (R/$\overline{W}$ = 0)

BYTE	LOGIC LEVEL		DESCRIPTION[1]
1st byte	0	0	output data Port 5 to Port 0
2nd byte[2]	ERF[3]	0	mode control Port 5 to Port 0

Notes

1. Output data bits for port 5 to port 0; mode control bits for Port 5 to Port 0 (1 = input, 0 = output).
2. Sending the 2nd byte will force the IC to reset.
3. When ERF = 1 the error flag is set for uncorrectable blocks; when ERF = 0 the error flag is always left unmodified; default: ERF = 1, mode control = 111111 (default = default value after a hardware reset).

Table 5 Read (R/$\overline{W}$ = 1)

BYTE	LOGIC LEVEL		DESCRIPTION
1st byte	0	0	input data Port 5 to Port 0[1]
2nd byte	S[2]	–	bits 22 to 16 of CorrCount
3rd byte	–	–	bits 15 to 8 of CorrCount
4th byte	–	–	bits 7 to 0 of CorrCount

Notes

1. Input data bits for Port 5 to Port 0.
2. When S = 0 it is in sync status; when S = 1 it is in no sync status.

The CorrCount is an estimation for the Byte Error Rate (BER) of the channel. This estimation is good for a high signal-to-noise ratio (SNR); then all uncorrected blocks will not have more than 9 errors. The CorrCount is incremented by 1 for each corrected byte. Each uncorrectable or unsychronized block will increment the CorrCount by 9. The CorrCount will saturate at '7FFFFFH' so that value actually means 'counter overflow'.

A CorrCount reset is caused by the following:

- A hardware or software reset
- Reading the 4th byte.

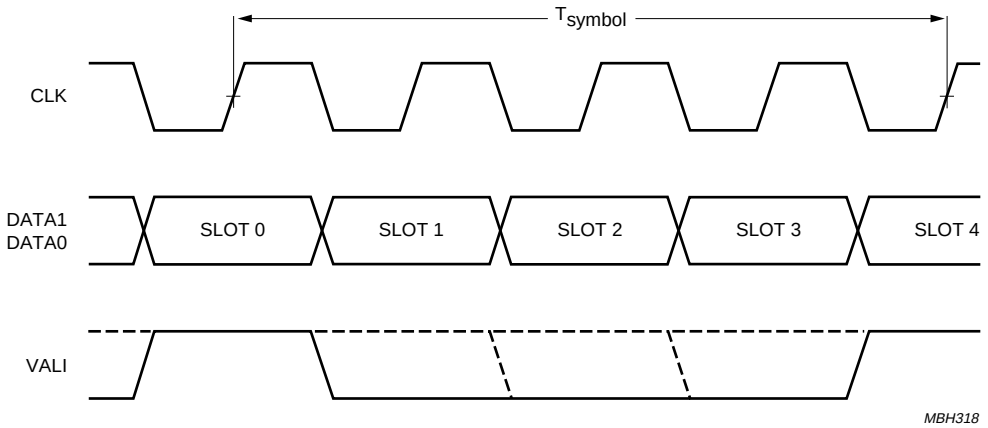
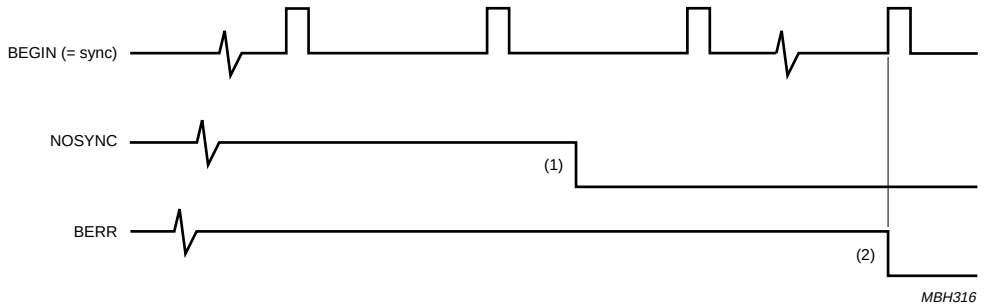


Fig.3 Input Interface.



(1) De-interleaver lock (sync process 1).
(2) Descrambling lock (sync process 2) and the condition that not more than 8 byte errors have occurred.

Fig.4 Synchronization timing.

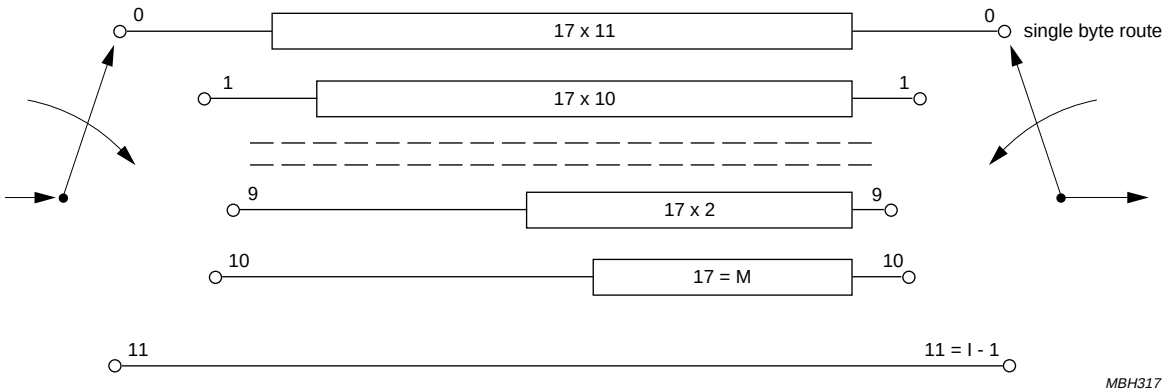


Fig.5 De-interleaver (I = 12).

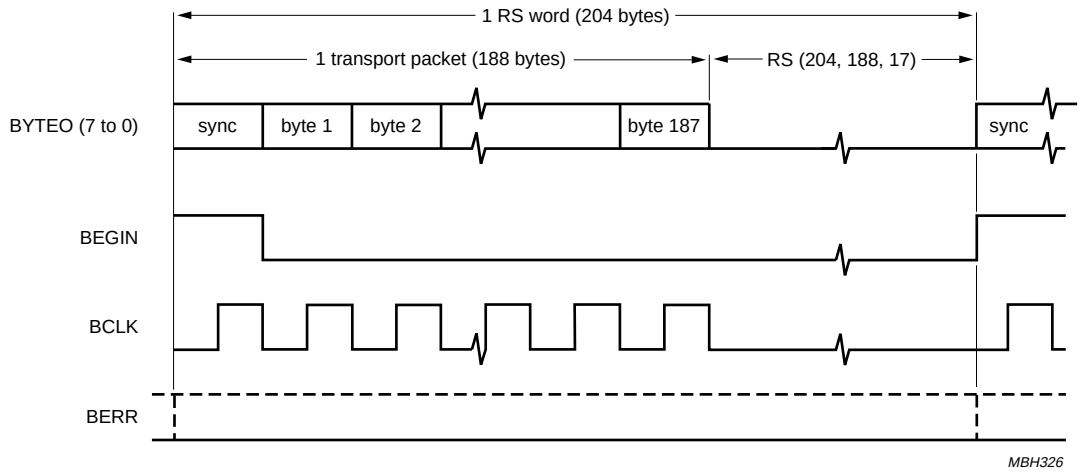


Fig.6 Output Interface timing.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.3	+6.0	V
V_i	input voltage	0	V_{DD}	V
I_i	input current	–10	+10	mA
I_o	output current	–20	+20	mA
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	0	70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

Every pin withstands the ESD test in accordance with MIL-STD-883C category B (2000 V). Every pin withstands the ESD test in accordance with Philips Semiconductors Machine Model; 0 Ω, 200 pF (200 V)

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{thj\text{-}a}$	thermal resistance from junction to ambient in free air	61	K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; see notes 1 and 2; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital inputs: pins 35, 36 and 34 (DATA1, DATA0 and VALI); see Fig.7						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	5	ns
$t_{SU;DAT}$	set-up time		7	–	–	ns
$t_{HD;DAT}$	hold time		5	–	–	ns
C_{li}	input capacitance		–	5	–	pF
Digital outputs: pins 11 to 13, 15 to 17, 19, 20, 24 and 23 (BYTEO0 to BYTEO7, BEGIN and BERR); see Fig.8						
V_{OL}	LOW level output voltage		0	–	$0.1V_{DD}$	V
V_{OH}	HIGH level output voltage		$0.9V_{DD}$	–	V_{DD}	V
t_d	delay time	C_L = 30 pF	$2T_{CLK} - 30$	–	–	ns
$t_{HD;DAT}$	hold time	C_L = 30 pF	$2T_{CLK} - 30$	–	–	ns
C_L	load capacitance		–	–	30	pF
Clock input: pin 38 (CLK)						
t_{CLK}	cycle time		–	31.5	–	ns
t_w	pulse width	40 : 60 duty	12	–	19	ns
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	5	ns
Clock output: pin 9 (BCLK)						
t_{BCLK}	BCLK cycle time		$4T_{CLK}$	–	–	ns
$t_{ow(BCLK)}$	BCLK pulse width		$2T_{CLK} - 15$	–	$2T_{CLK} + 15$	ns

Notes

1. Detailed timing of the RESET, NOSYNC, Port 0 to Port 5 and test pins is assumed not to be relevant for the application.
2. For a proper RESET procedure the RESET pin should be HIGH during at least 5 rising edges of the CLK pin.

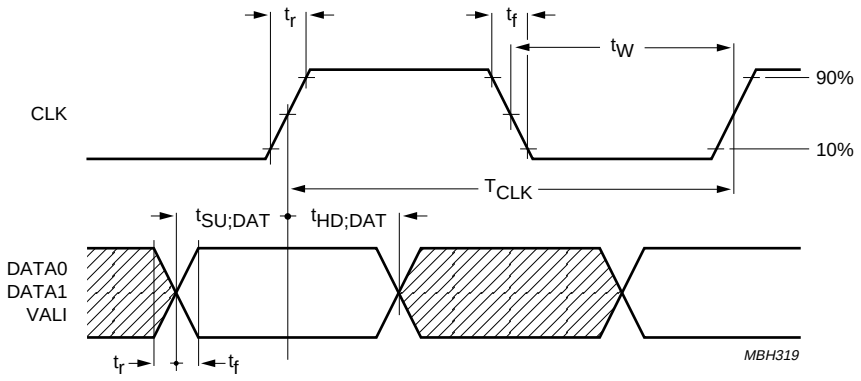


Fig.7 Input data timing waveforms.

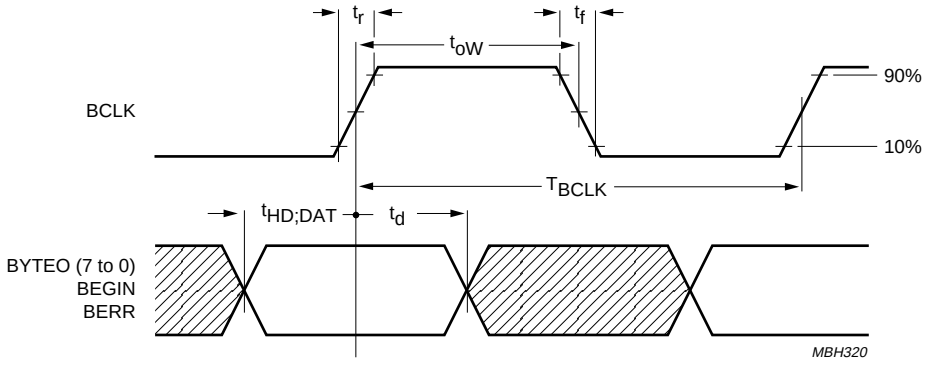


Fig.8 Output data timing waveforms.

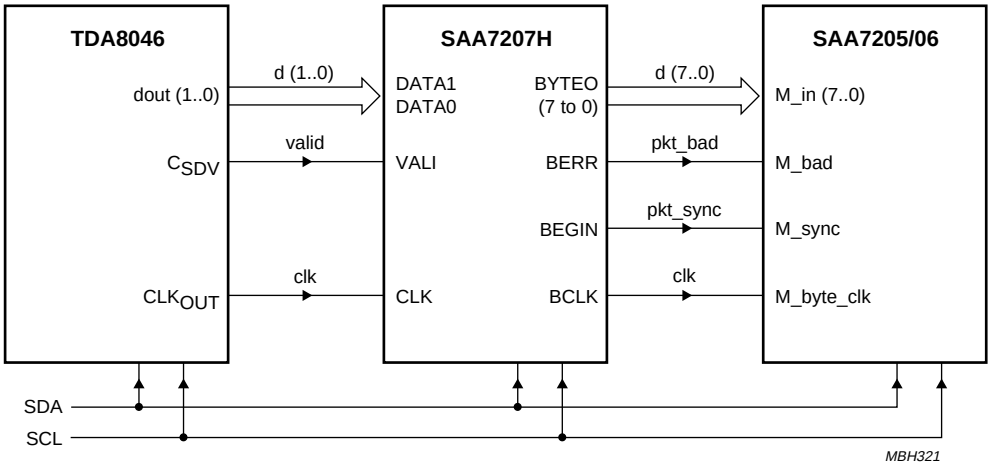
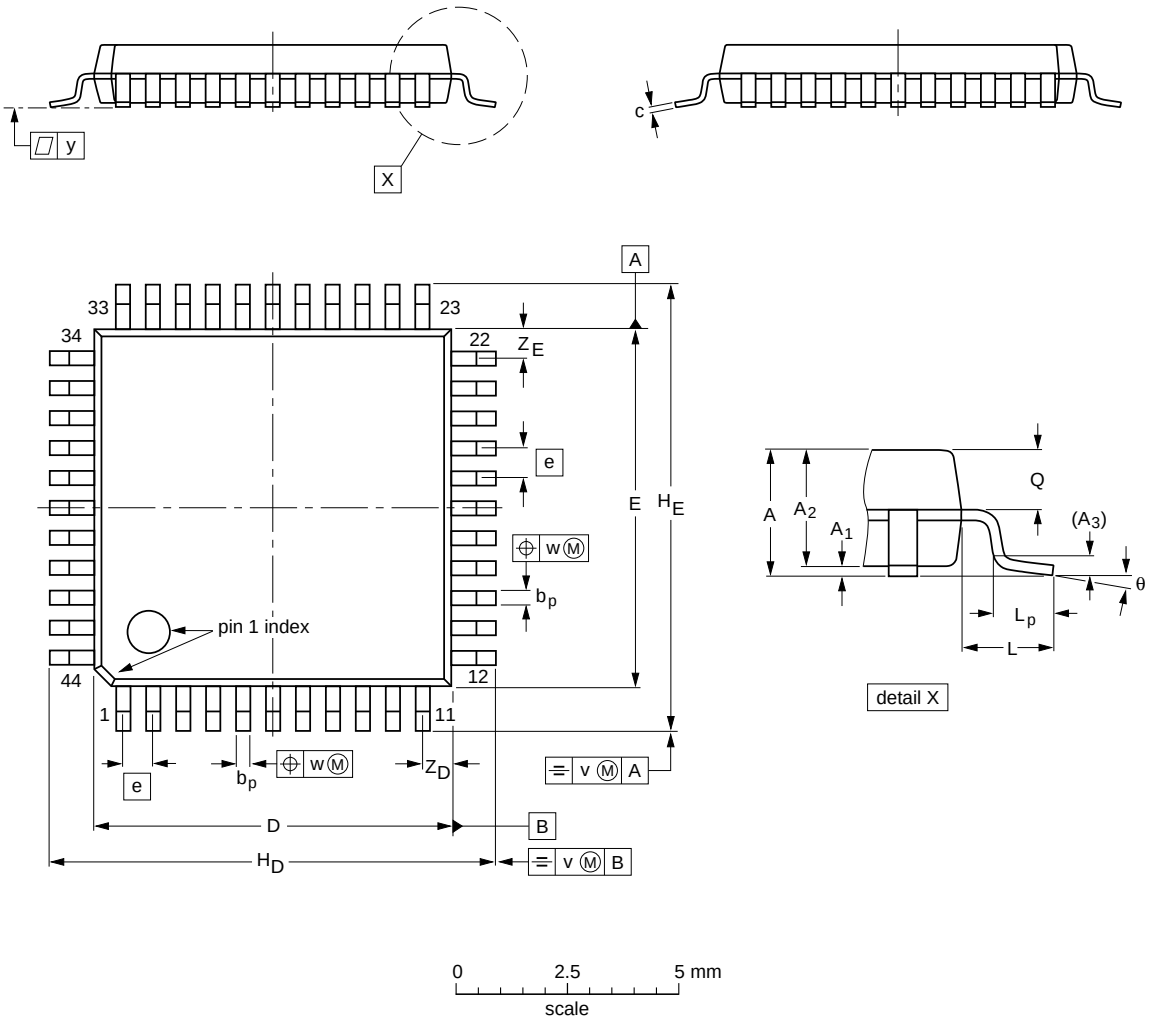


Fig.9 Application diagram.

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.