DATA SHEET

SAA8110G
Digital Signal Processor (DSP) for cameras

Preliminary specification
File under Integrated Circuits, IC02

1997 Jun 13

Philips
Semiconductors

PHILIPS

Digital Signal Processor (DSP) for cameras

SAA8110G

FEATURES

- High precision digital processing with 9 or 10 bit input
- Different types of CCDs (PAL, NTSC and CIF) (progressive, interlaced and non-interlaced)
- Black offset preprocessing (including optical black offset control)
- RGB-separation (with contour and white clip signals generation)
- RGB-processing (colour space matrix, black control, knee and gamma)
- RGB-to-YUV conversion (including down-sampling filters)
- White balance control
- Y-processing (contour processing, false colour detector, filters and noise reduction)
- UV-processing (false colour correction and noise reduction)
- Digital output formatter (including CIF-formatter, DTV2, D1)
- Analog output preprocessing (including PAL/NTSC-encoder and DACs)
- Measurement engine (prepared for auto-exposure and auto-white balance features)
- Miscellaneous functions (e.g. switched mode power supply pulse generator, control DAC)
- VH-reference and window timing
- Serial interface (selectable I^{2}C-bus or 80C51 UART interface)
- Mode control (including power management).

APPLICATIONS

- Desktop video applications
- Surveillance systems
- Video-phone systems.

GENERAL DESCRIPTION

The SAA8110G is designed for desktop video applications (teleconferencing, video grabbing), surveillance and video-phone systems.

The SAA8110G may be applied together with an analog front-end (TDA8786 including CDS/AGC/ADC), a timing generator and a microcontroller as shown in Figs 18 and 19. Other configurations are also possible.

The CCD-sensor can be of PAL, NTSC or CIF type (with complementary mosaic colour filter). The maximum number of active pixels is limited to 800 samples/line. The 10-bits digital input may have a pixel frequency of up to 14.318 MHz.

The SAA8110G output data is available in a digital and an analog output format. Two digital output formats are selectable: DTV2 (CCIR-601 at the input pixel frequency) and D1 (CCIR-656 at twice the input pixel frequency). It is also possible to generate the CIF and QCIF formats as subsets from the processed CCD-image. The analog output is available in one of four formats: RGB, YUV, YC or CVBS. The SAA8110G includes a digital PAL/NTSC-encoder and 3 DACs for this purpose.

Two types of serial interface are selectable: a fast 400 kHz I^{2}C-bus interface or a 80C51 UART interface (with bit rates from 1 Mbit/s up to 3.75 Mbit/s depending on the system clock used). The power dissipation of the SAA8110G can be optimized for each application using the built-in power management function.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA8110G	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		3	5	5.25	V
V_{DDA}	analog supply voltage		3	5	5.25	V
V_{IL}	LOW level digital input voltage		0	–	$0.3V_{DDD}$	V
V_{IH}	HIGH level digital input voltage		$0.6V_{DDD}$	–	V_{DDD}	V
V_{OL}	LOW level digital output voltage	I_{OL} = –20 μA	–	–	0.5	V
V_{OH}	HIGH level digital output voltage	I_{OH} = 20 μA	V_{DDD} – 0.1	–	–	V
$I_{DDD(tot)}$	total digital supply current	f_{clk} = 14.3 MHz; V_{DDD} = 5 V	–	180	200	mA
		f_{clk} = 14.3 MHz; V_{DDD} = 3.3 V	–	80	100	mA
$I_{DDA(tot)}$	total analog supply current	f_{clk} = 14.3 MHz; V_{DDA} = 5 V	–	30	40	mA
		f_{clk} = 14.3 MHz; V_{DDA} = 3.3 V	–	22	35	mA
T_{amb}	operating ambient temperature		0	–	75	°C
I_{DMD}	supply current in digital output mode	f_{clk} = 14.3 MHz; V_{DDD} = 5 V; note 1	–	185	–	mA
		f_{clk} = 14.3 MHz; V_{DDD} = 3.3 V	–	85	–	mA

Note

1. When digital mode is selected, V_{DDA} supply pins can be connected to ground.

BLOCK DIAGRAM

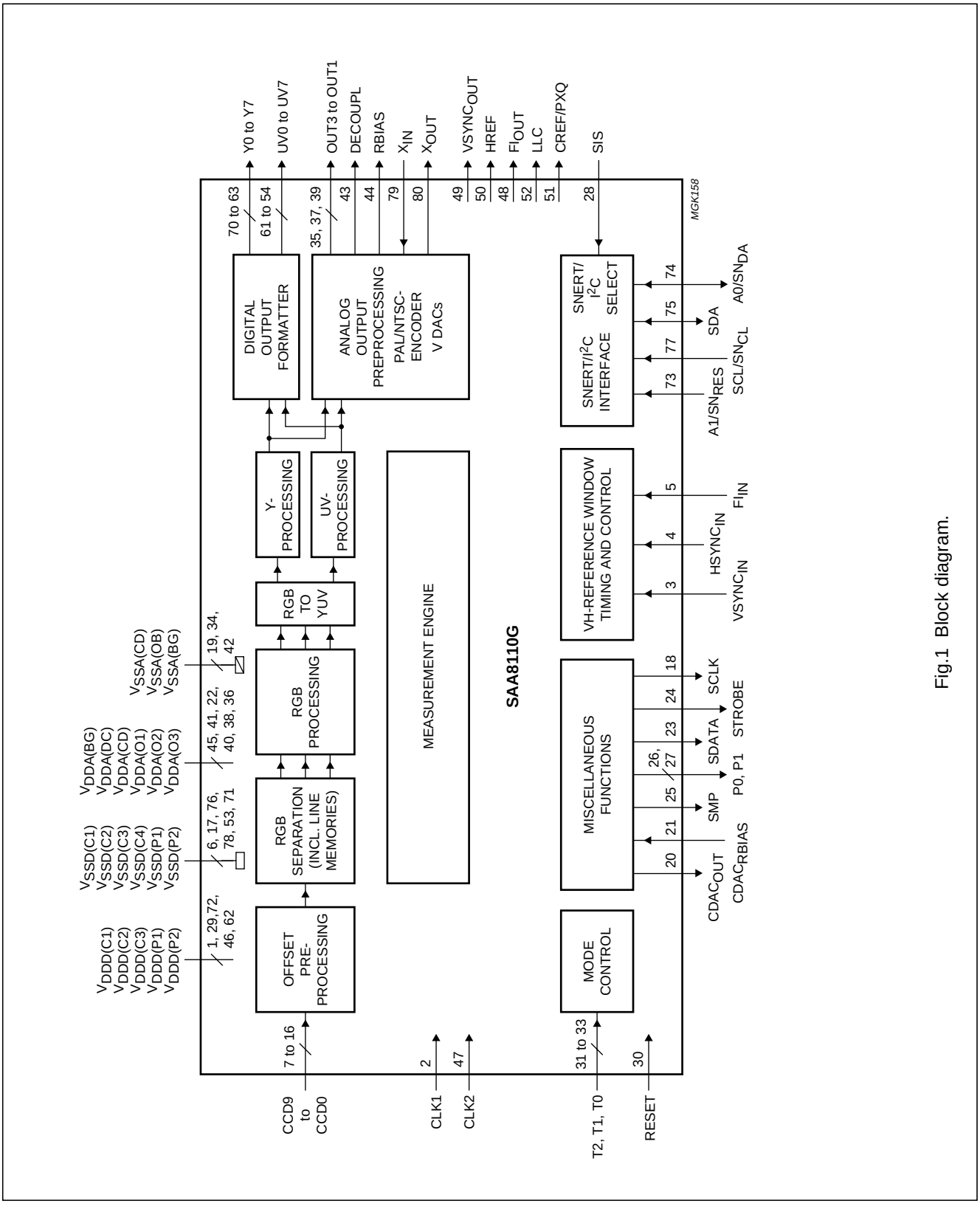


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
$V_{DDD(C1)}$	1	I	digital supply 1 for digital core and CLK1 related peripherals
CLK1	2	I	system- or pixel clock
$VSYNC_{IN}$	3	I	vertical synchronization input
$HSYNC_{IN}$	4	I	horizontal synchronization input
FI_{IN}	5	I	field identification signal input
$V_{SSD(C1)}$	6	I	digital ground 1 for digital core and CLK1 related peripherals
CCD9	7	I	(preprocessed) AD-converted CDD-signal bit 9 (MSB)
CCD8	8	I	(preprocessed) AD-converted CDD-signal bit 8
CCD7	9	I	(preprocessed) AD-converted CDD-signal bit 7
CCD6	10	I	(preprocessed) AD-converted CDD-signal bit 6
CCD5	11	I	(preprocessed) AD-converted CDD-signal bit 5
CCD4	12	I	(preprocessed) AD-converted CDD-signal bit 4
CCD3	13	I	(preprocessed) AD-converted CDD-signal bit 3
CCD2	14	I	(preprocessed) AD-converted CDD-signal bit 2
CCD1	15	I	(preprocessed) AD-converted CDD-signal bit 1
CCD0	16	I	(preprocessed) AD-converted CDD-signal bit 0 (LSB)
$V_{SSD(C2)}$	17	I	digital ground 2 for digital core and CLK1 related peripherals
SCLK	18	O	serial clock to TDA8786
$V_{SSA(CD)}$	19	I	analog ground for control DAC
$CDAC_{OUT}$	20	O	output control DAC
$CDAC_{RBIAS}$	21	I	pin to connect external bias resistor for control DAC
$V_{DDA(CD)}$	22	I	analog supply for control DAC
SDATA	23	O	serial data to TDA8786
STROBE	24	O	strobe to TDA8786
SMP	25	O	switch mode pulse for DC-DC
P0	26	O	quasi-static control output pin 0
P1	27	O	quasi-static control output pin 1
SIS	28	I	SNERT/I^2C-bus select input signal
$V_{DDD(C2)}$	29	I	digital supply 2 for digital core and CLK1 related peripherals
RESET	30	I	reset input
T2	31	I	test mode control signal bit 2
T1	32	I	test mode control signal bit 1
T0	33	I	test mode control signal bit 0
$V_{SSA(OB)}$	34	I	analog ground for the three output buffers
OUT3	35	O	output buffer 3 (R, V or CVBS)
$V_{DDA(O3)}$	36	I	analog supply for output buffer OUT3
OUT2	37	O	output buffer 2 (B, U or C)
$V_{DDA(O2)}$	38	I	analog supply for output buffer OUT2
OUT1	39	O	output buffer 1 (G or Y)
$V_{DDA(O1)}$	40	I	analog supply for output buffer OUT1

SYMBOL	PIN	I/O	DESCRIPTION
$V_{DDA(DC)}$	41	I	analog supply for analog core of triple DAC
$V_{SSA(BG)}$	42	I	analog ground for to band gap
DECOUPL	43	O	pin to be used for external decoupling of band gap
RBIAS	44	O	external bias resistor connection for band gap
$V_{DDA(BG)}$	45	I	analog supply for band gap
$V_{DDD(P1)}$	46	I	digital supply 1 for CLK2 related peripherals
CLK2	47	I	output clock (CLK2 frequency is 2 × CLK1 frequency)
FI_{OUT}	48	O	field identification output pulse
$VSYNC_{OUT}$	49	O	vertical synchronization output
HREF	50	O	horizontal reference output for YUV-port
CREF/PXQ	51	O	clock/pixel qualifier output for YUV-port
LLC	52	O	line-locked system clock output
$V_{SSD(P1)}$	53	I	digital ground 1 for CLK2 related peripherals
UV7	54	O	multiplex chrominance UV bit 7 (MSB)
UV6	55	O	multiplex chrominance UV bit 6
UV5	56	O	multiplex chrominance UV bit 5
UV4	57	O	multiplex chrominance UV bit 4
UV3	58	O	multiplex chrominance UV bit 3
UV2	59	O	multiplex chrominance UV bit 2
UV1	60	O	multiplex chrominance UV bit 1
UV0	61	O	multiplex chrominance UV bit 0 (LSB)
$V_{DDD(P2)}$	62	I	digital supply for CLK2 related peripherals
Y7	63	O	luminance Y or multiplexed YUV bit 7 (MSB)
Y6	64	O	luminance Y or multiplexed YUV bit 6
Y5	65	O	luminance Y or multiplexed YUV bit 5
Y4	66	O	luminance Y or multiplexed YUV bit 4
Y3	67	O	luminance Y or multiplexed YUV bit 3
Y2	68	O	luminance Y or multiplexed YUV bit 2
Y1	69	O	luminance Y or multiplexed YUV bit 1
Y0	70	O	luminance Y or multiplexed YUV bit 0 (LSB)
$V_{SSD(P2)}$	71	I	digital ground 2 for to CLK2 related peripherals
$V_{DDD(C3)}$	72	I	digital supply 3 for digital core and CLK1 related peripherals
$A1/SN_{RES}$	73	I	I^2C-bus address select pin A1 or SNERT reset input
$A0/SN_{DA}$	74	I	I^2C-bus address select pin A0 or SNERT data input/output
SDA	75	I	I^2C-bus data input/output
$V_{SSD(C3)}$	76	I	digital ground 3 for digital core and CLK1 related peripherals
SCL/SN_{CL}	77	I	I^2C-bus clock/SNERT clock input
$V_{SSD(C4)}$	78	I	digital ground 4 for digital core and CLK1 related peripherals
X_{IN}	79	I	input crystal oscillator for subcarrier lock applications
X_{OUT}	80	O	output crystal oscillator for subcarrier lock applications

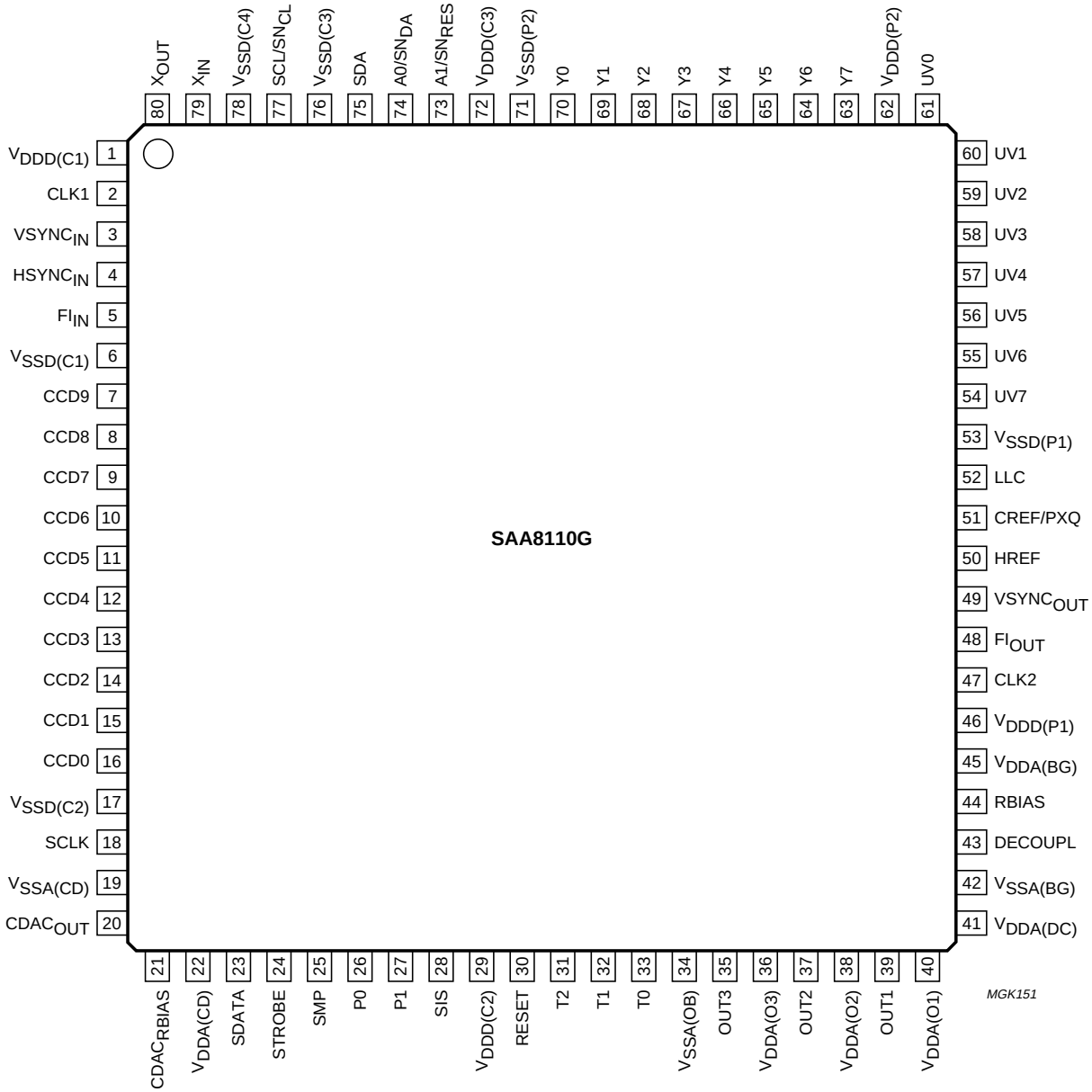


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Black offset preprocessing

The input data is clamped within the optical black pixel area of the CCD. The size of the digital clamp window is 16 pixels by 128 lines (i.e. TDA8786). It is possible to differentiate black levels for odd/even lines, pixels and fields. This comes in addition to the analog preprocessing clamp which is active on the clamp pulse generated by the external timing circuit. The analog clamp is included in the TDA8786.

RGB separation

PAL/NTSC sensors generate interlaced data adding offset in the complementary colour pixels. The RGB separation block with its two line memories generates the three components Y, 2R – G, and 2B – G for each input data corresponding to a pixel value of the CCD. Then the triplet R, G, B is derived. This block also delivers some contour and white clip information.

RGB processing

The RGB processing includes several features:

- Colour space matrix depending on CCD type to be suitable with different sensor colour filters
- Gain correction for R and B signals for white balance control
- Black offset
- Adjustable knee
- Adjustable gamma function.

The knee function is applied to all three RGB signals. Its shape is continuously adjustable by changing the slope and the knee offset point.

To compensate for the non-linear response of display devices, a gamma correction is applied to R, G and B signals. It may be adjustable from linear to a 0.35 power coefficient.

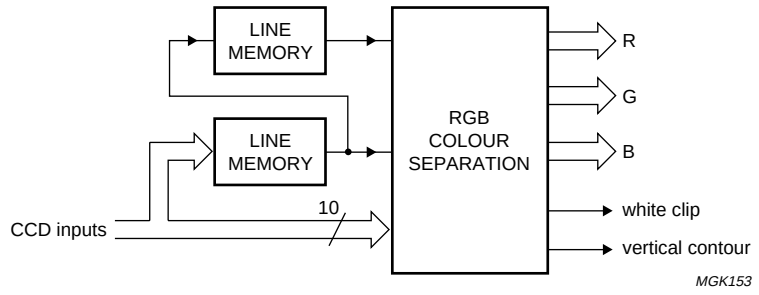


Fig.3 RGB separation diagram.

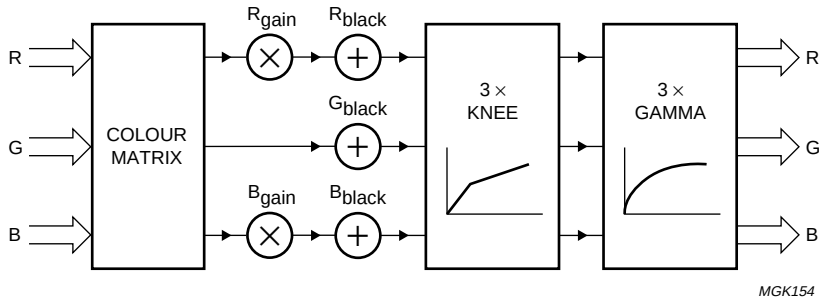


Fig.4 RGB processing.

RGB-to-YUV block

After RGB processing, the channels are separated in a luminance and two colour difference path:
Y = 0.299 R + 0.597 G + 0.114 B, U = 0.49 (B – Y) and V = 0.88 (R – Y) . It also contains two down-sampling filters for U and V signals.

Y-processing

The luminance component includes several features:

- Contour correction allowing an increase of the luminance transitions for a sharper picture
- Black stretch function for contrast enhancement in dark scenes
- False colour detector used by the UV-processing block to enable the colour killer
- Filters and noise reduction by coring (only in the high frequency part of the signal).

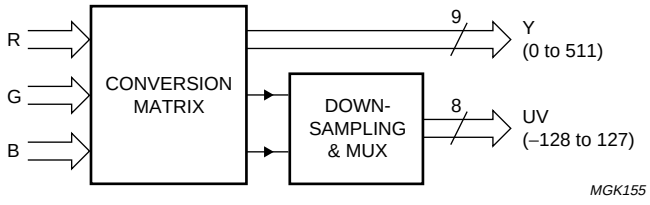


Fig.5 RGB-to-YUV conversion.

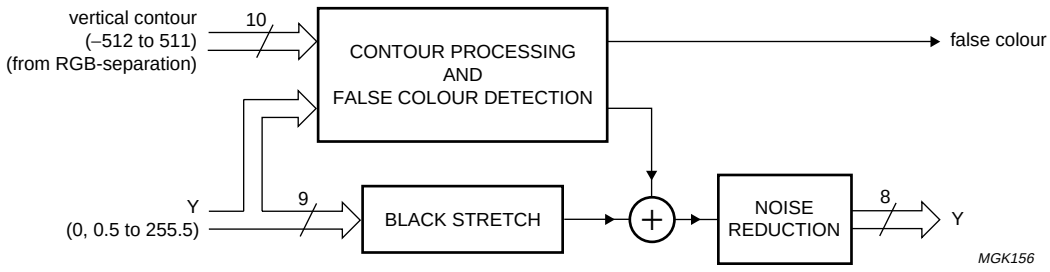


Fig.6 Y processing.

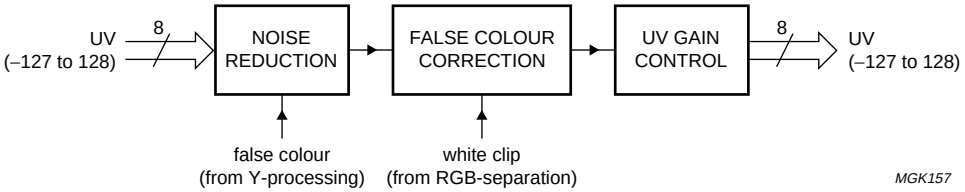


Fig.7 UV-processing.

UV-processing

The chrominance component includes several features:

- Noise reduction for high frequencies
- False colour correction: a colour killer cuts the false colour components in the UV signals
- UV-gain control used to set the correct UV levels for PAL/NTSC encoding.

As the colour filter saturation levels may be different in the CCD, the white clip is used in the UV-processing to suppress colour errors in case of high exposure**.**

Digital output formatter

This block contains several features:

- Generation of a synchronous clock LLC (twice the clock frequency)
- Generation of three synchronization signals (HREF, CREF and VS)
- Synchronization of the output data to the output clock LLC
- Generation of a CIF/QCIF output format for several type of sensors (see Table 1)
- Selection of the required digital output format (8-bit multiplexed YUV standard D1/CCIR 656, including the generator of SAV/EAV codes or 16-bit multiplexed YUV 4 : 2 : 2 standard DTV2/CCIR601).

Note that the D1 frequency data rate is twice the DTV2 frequency data rate.

Moreover, using a high resolution PAL and NTSC CCDs, it is possible to generate the following formats by means of cutting or down-sampling.

- CIF 352 × 288 at 25 frame/second and CIF 352 × 240 at 30 frame/second
- QCIF 176 × 144 at 25 frame/second and QCIF 176 × 120 at 30 frame/second.

Table 1 CIF/QCIF output format for different sensor types

INPUT FORMAT	OUTPUT FORMAT	
PAL/NTSC-sensor	CIF	‘full screen’
	CIF	‘zoom-by-2’
	QCIF	‘full screen’
	QCIF	‘zoom-by-2’
	QCIF	‘zoom-by-4’
CIF	QCIF	‘full screen’
	QCIF	‘zoom-by-2’

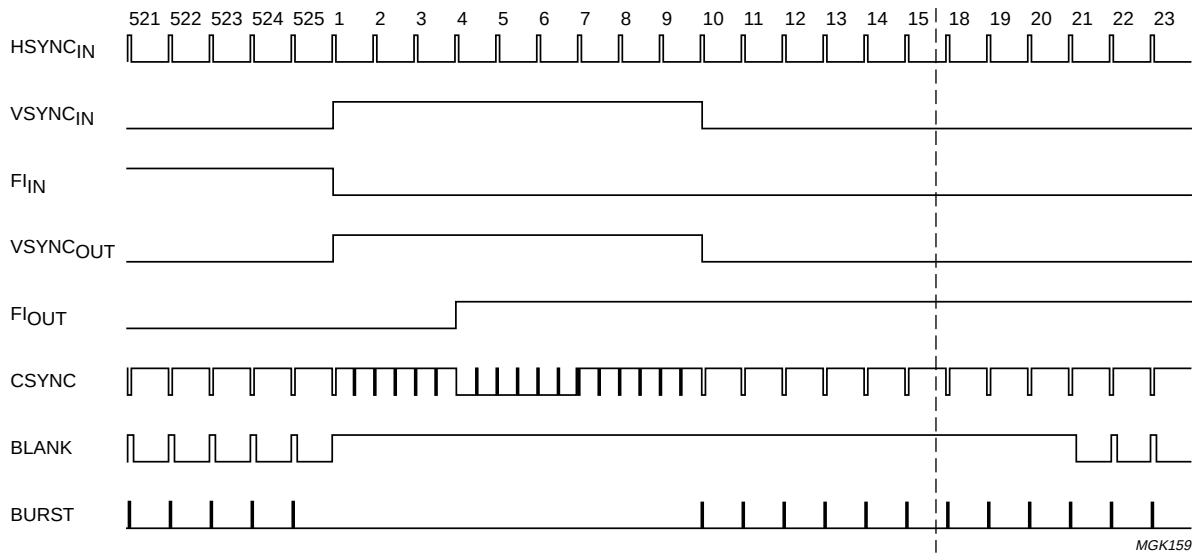


Fig.8 Vertical timing NTSC odd field.

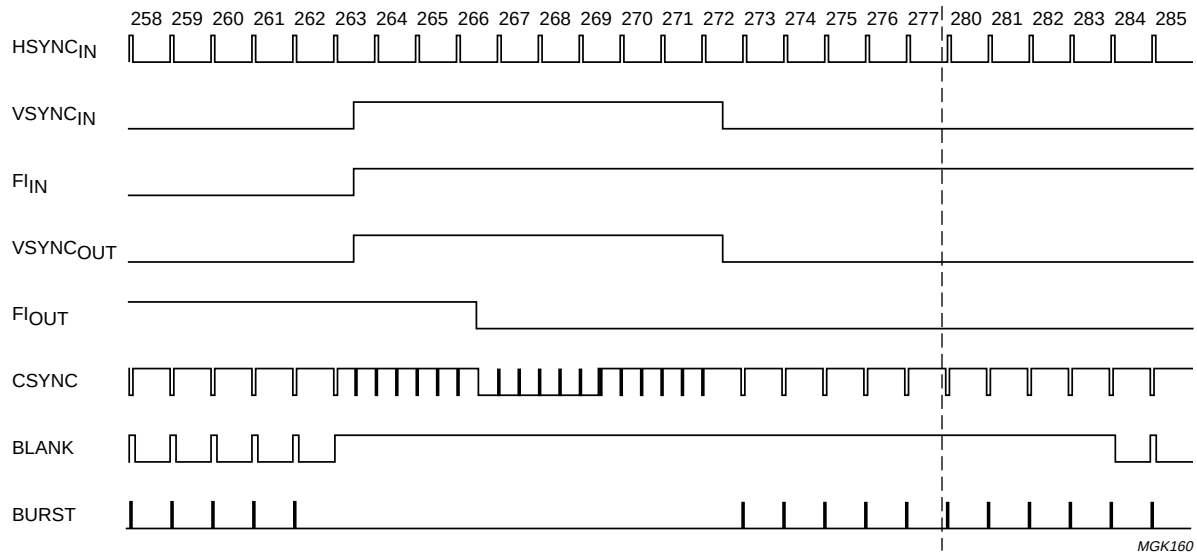
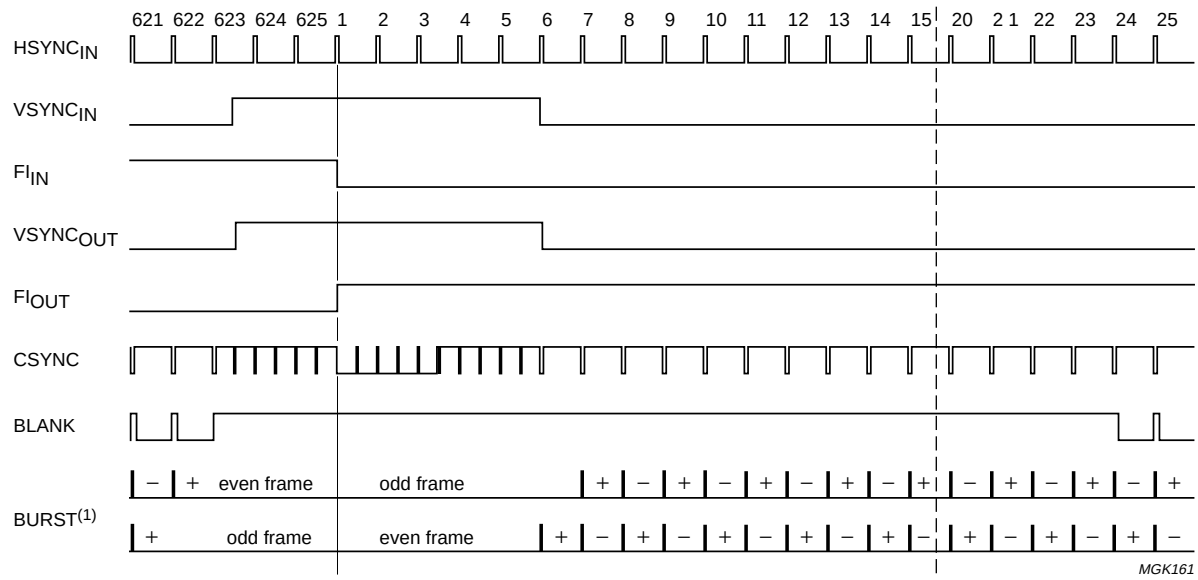
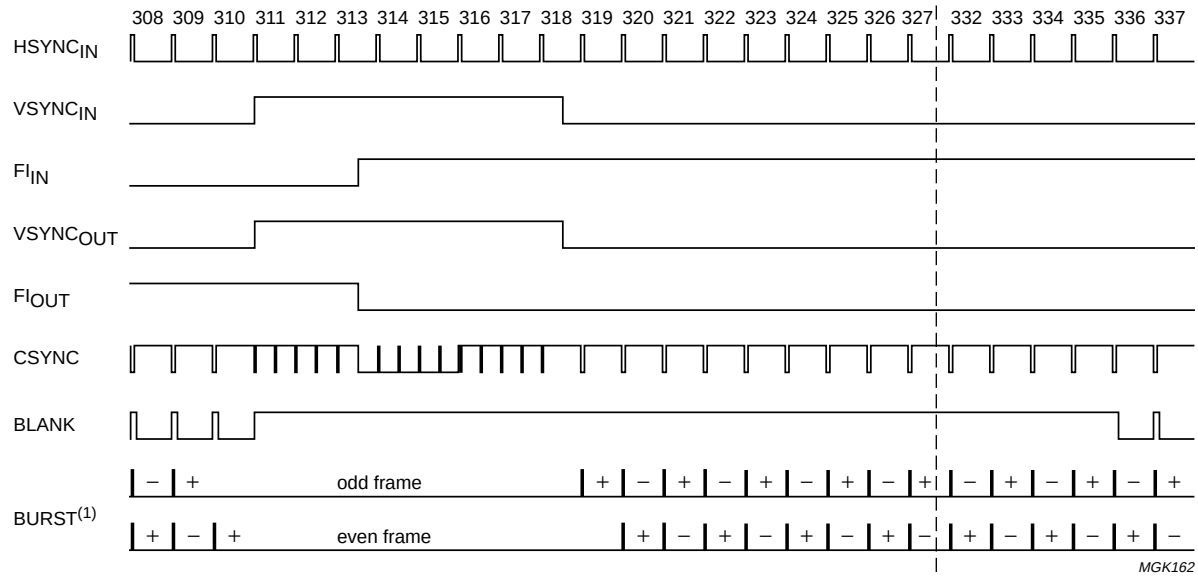


Fig.9 Vertical timing NTSC even field.



(1) +: burst phase = +135°.
–: burst phase = –135°.

Fig.10 Vertical timing PAL odd field.



(1) +: burst phase = +135°.
–: burst phase = –135°.

Fig.11 Vertical timing PAL even field.

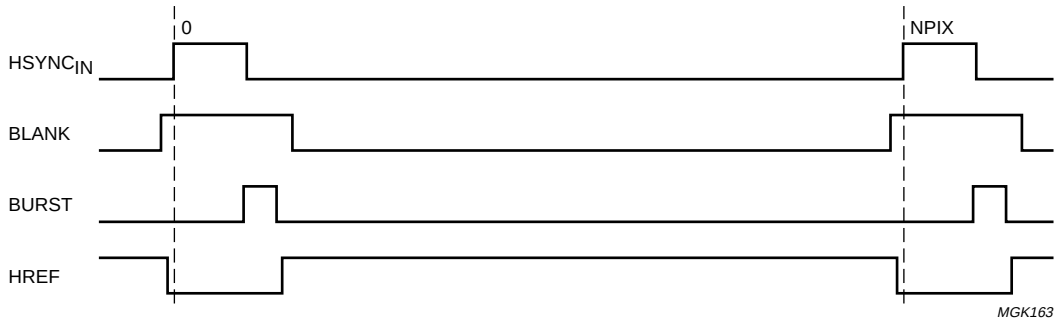


Fig.12 Horizontal timing for non-CIF processing.

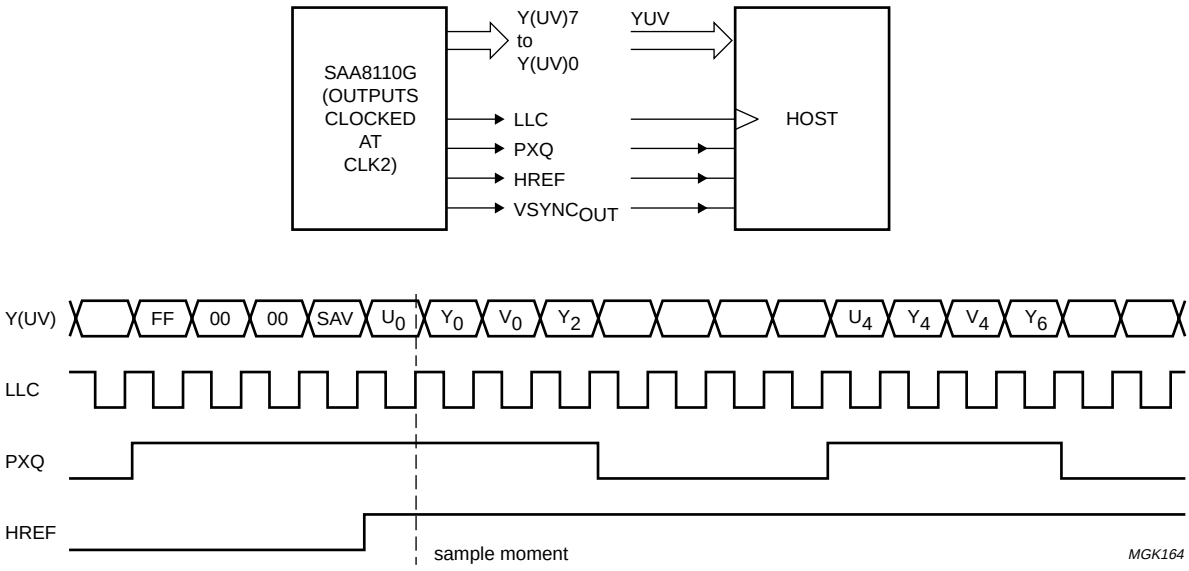


Fig.13 8-bits multiplexed format (D1, CCIR656); example: CIF down-sampling.

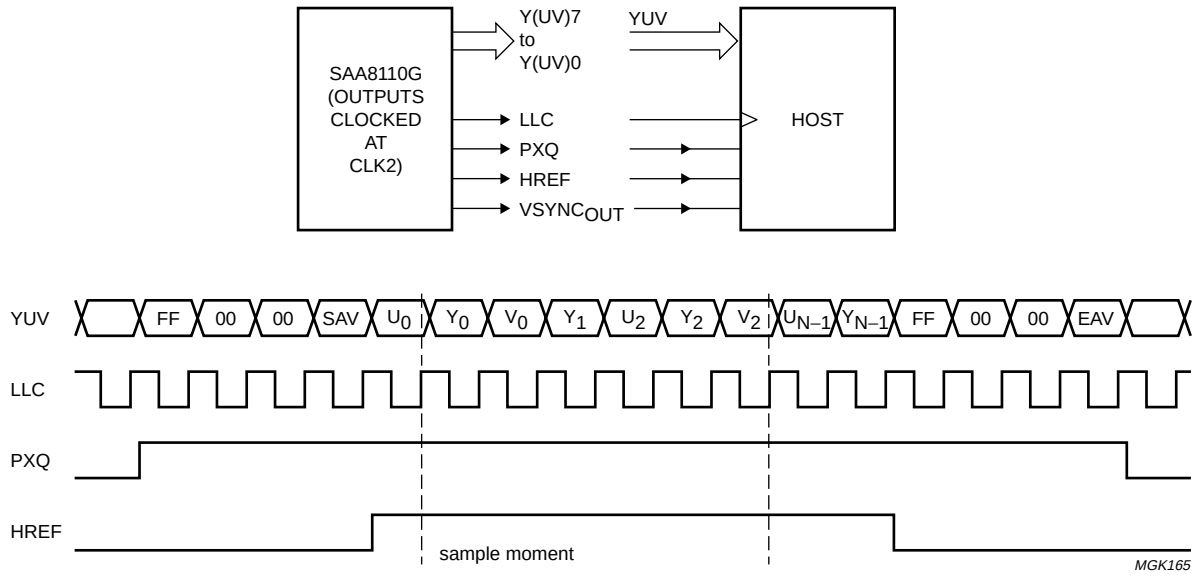


Fig.14 8-bits multiplexed format (D1, CCIR656); SAV/EAV included.

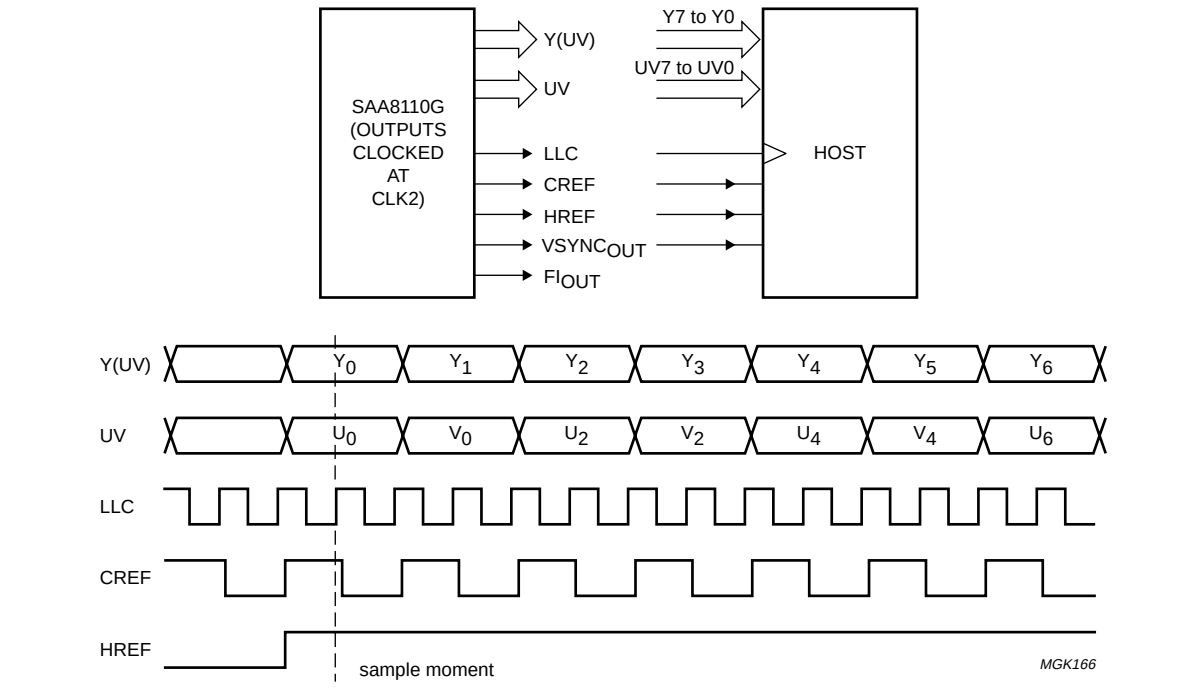


Fig.15 16-bits multiplexed format (DTV2, CCIR601).

Analog output preprocessing

This block contains several features:

- Delay compensation for the luminance signal
- Up-sampling of the UV signal
- PAL/NTSC encoding
- YUV to RGB conversion
- Selection of the required analog output format (RGB, YUV, YC or CVBS).

The analog outputs are given by three voltage DACs in RGB or YUV or CVBS or YC format. Channels Y and G include the sync information. Over-sampling at twice f_{clk} is made so that external filtering becomes easier. It is also possible to have an adjustment of the subcarrier via the serial interface. When CVBS output is used, chrominance range is halved compared to luminance.

Measurement engine

The measurement engine performs measurements on some selectable internal signals on frame/field basis and prepares data for auto exposure, auto focus and auto white balance processing. It uses an internal RAM work-space for its control and data handling operations. The contents of the work-space can be accessed via the serial interface.

Vertical/horizontal reference and window timing and control

The SAA8110G uses two vertical and horizontal synchronization input signals ($VSYNC_{IN}$ and $HSYNC_{IN}$) to derive internal vertical and horizontal reference signals. Besides a Field Identification input (FI_{IN}) signal is required. The timing of the vertical and horizontal input signals should be such that:

1. The pixel frequency (CLK1) must be line-locked to the line frequency of $HSYNC_{IN}$: the number of clock periods between two $HSYNC_{IN}$ pulses must be a fixed integer number. The $HSYNC_{IN}$ should be at least one clock period active HIGH.
2. The $VSYNC_{IN}$ signal indicates the start of a field (**or frame in case of progressive scanning**); this signal is also required for non-interlaced applications. The $VSYNC_{IN}$ should be at least one clock period HIGH.
3. The FI_{IN} pulse indicates the phase of the field in case of interlaced applications (FI_{IN} = 0 means odd field).

Serial interface

The serial interface can either be an I²C-bus or a 80C51 UART (SNERT) (selectable with the SIS pin). Via the serial interface the external microcontroller can control the internal settings of the SAA8110G and read/write from/to the internal RAM work-space linked to the measurement engine (see list of parameter settings in Chapter “Programming”). Some of the registers are double-buffered to prevent that the change of control data becomes visible on the output display.

Miscellaneous functions

A three wire bus is used to send 10-bit settings from a microcontroller to the TDA8786 via the SAA8110G registers.The SAA8110G supplies picture parameters and needs some configuration parameters. Those values are contained in registers and are updated during every vertical synchronization pulse.

Mode control

This block controls the operation mode of the SAA8110G. As described in Table 2, four modes may be selected: depending on power reduction and I²C-bus timing.

Power dissipation management

The power dissipation of the SAA8110G will depend on the required activity for a certain application. It is possible to switch off via the serial interface unconcerned parts for a given application. When an analog output is not used, the power voltage pin of the DAC can be connected to ground to limit the power consumption.

Clock configurations

Following conditions must be fulfilled:

- CLK1 should be generated as divide-by-two from CLK2
- The RESET pin should not go LOW before CLK1 and CLK2 are both HIGH or LOW.

Table 2 SAA8110G mode control

T2	T1	T0	MODE	POWER REDUCTION	$t_{o(h)}$ I²C-BUS
0	0	0	application mode	on	short
0	0	1		on	long
0	1	0		off	short
0	1	1		off	long

Table 3 Sensor and output formats covered by the SAA8110G

CCD-formats			RESOLUTION		PIXEL FREQUENCY (MHz)	OUTPUT FORMATS		
STANDARD	FRAME SCANNING AND FREQUENCY (Hz)		ACTIVE H/V	TOTAL H/V		DIGITAL		ANALOG
						DTV2/D1	CIF	
CIF	non-interlaced	60	352/243	429/262	6.75	no	yes	yes
CIF	non-interlaced	50	352/288	432/312	6.75	no	yes	yes
NTSC high resolution	non-interlaced interlaced	60.054 29.997	768/243 768/494	910/262 910/525	14.3181	yes	yes	yes
PAL high resolution	non-interlaced interlaced	50 25	752/288 752/582	908/312 908/625	14.1875	yes	yes	yes
NTSC medium resolution	non-interlaced interlaced	60 30	512/243 512/492	606/262 606/525	9.53495	yes	no	yes
PAL medium resolution	non-interlaced interlaced	50 25	512/288 512/582	618/312 618/625	9.65625	yes	no	yes

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	–0.3	+7.0	V
V_{DDA}	analog supply voltage	–0.3	+7.0	V
$\Delta V_{DDD-DDA}$	supply voltage difference between the digital and the analog supply voltages	–0.1	+0.1	V
V_I	input voltage	–0.3	V_{DD} + 0.3	V
V_O	output voltage	–0.3	V_{DD} + 0.3	V
P_{tot}	total allowed power dissipation at T_{amb} = 75 °C	–	1	W
T_{stg}	storage temperature	–55	+150	°C
T_j	junction temperature	–	125	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	50	K/W

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDACs specification						
OUTPUTS PINS OUT1 TO OUT3 (IN CASE OF SCALE FACTOR = 1)						
V_o	output voltage (see note 1)	code 0	0	0.2	0.3	V
		code 511	1.3	1.5	1.6	V
V_{offset}	amplitude offset voltage between DACs		–60		+60	mV
INPUTS						
R_{bias}	bias resistor	note 2	14	15	16	kΩ
		note 3	44	47	50	kΩ
R_{ext}	external anti-reflection resistor	note 2	–	21	–	Ω
		note 3	–	70.6	–	Ω
C_{decoup}	decoupling capacitor		10	–	100	nF
TRANSFER FUNCTION						
RES	resolution		–	9	–	bit
NL_{diff}	differential non-linearity		–	–	1.5	LSB
NL_{int}	integral non-linearity		–	–	1.5	LSB
THD_{60}	total harmonic distortion at 60% of full-scale	f_{clk} = 30 MHz, f_i = 1 MHz, V_{DDA} = 5 V	–	55	45	dB
S/N	signal-to-noise ratio	f_{clk} = 30 MHz, f_o = 1 MHz, V_{DDA} = 5 V	–	45	38	dB
APPLICATION1: PAL/NTSC HIGH RESOLUTION						
V_{DD1}	supply voltage		4.5	5.0	5.5	V
V_{DD2}	supply voltage		3.0	3.3	3.6	V
CR	conversion rate		–	28.6	–	MHz
f_{clk}	clock frequency		–	28.6	–	MHz
B_a	analog bandwidth		–	7.6	–	MHz
APPLICATION 2: PAL/NTSC MEDIUM RESOLUTION						
V_{DD1}	supply voltage		4.5	5.0	5.5	V
V_{DD2}	supply voltage		3.0	3.3	3.6	V
f_{clk}	clock frequency		–	19	–	MHz
B_a	analog bandwidth		–	6.5	–	MHz
SWITCHING CHARACTERISTICS ON RISING FULL-SCALE STEP (see Fig.16)						
t_{PD}	propagation delay time	to 50% value	–	9	13	ns
$t_{st(10-90)}$	settling time	10% to 90% full-scale	–	9	11	ns
$t_{st(LSB)}$	setting time (to ±1 LSB)		–	25	30	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CDAC specification (V_{DD} = 5 V)						
L_{int}	integral linearity		–	–	1	LSB
L_{diff}	differential linearity		–	–	½	LSB
$V_{o(CDAC)}$	output voltage at pin CDAC	code 0	–	10	300	mV
		code 61, V_{DDA} = 5 V	–4.6	4.95	–	V
		code 61, V_{DDA} = 3.3 V	3	3.25	–	V
$R_{o(CDAC)}$	output resistance at pin CDAC		–	13	–	Ω
f_{clk}	clock frequency		–	28.6	–	MHz
R_L	load resistance		–	10	–	kΩ
C_L	load capacitance		–	–	10	pF
t_{PD}	propagation delay time	to 50% value (see Fig.17), V_{DDA} = 5 V	–	–	104	ns
$t_{st(10-90)}$	settling time	10% to 90% full-scale (see Fig.16)	–	9	–	ns
$t_{st(LSB)}$	setting time	to ±1 LSB (see Fig.16)	–	25	–	ns
INPUTS RELATED TO CLK1: CCD0 TO CCD9, $VSYNC_{IN}$, $HSYNC_{IN}$, FI_{IN}						
$t_{su(i)(D)1}$	data input set-up time CCD inputs, $HSYNC_{IN}$, $VSYNC_{IN}$, FI_{IN}		0	3	5	ns
$t_{su(i)(D)2}$	data input set-up time SN_{RES} and SN_{DA}		0	1	2	ns
$t_{h(i)(CCD)}$	data hold time CCD inputs		–1	–	+1	ns
$t_{h(i)(D)}$	data input hold time	$VSYNC_{IN}$, $HSYNC_{IN}$, FI_{IN}	0	1	3	ns
OUTPUTS RELATED TO CLK2: Y7 TO Y0, UV7 TO UV0, CREF, HREF, $VSYNC_{OUT}$, FI_{OUT} AND LLC						
$t_{h(o)(D)}$	data output hold time		–	8	22	ns
$t_{d(o)(D)}$	data output delay time		–	25	31	ns
OUTPUTS RELATED TO CLK1: SDATA, STROBE, SMP, P0, P1 AND SCLK						
$t_{h(o)(D)}$	data output hold time		–	13	21	ns
$t_{d(o)(D)}$	data output delay time		–	15	24	ns
δ_{clk}	clock duty cycle		40	–	60	%

Notes

1. When CVBS output is used the chrominance range is halved compared to luminance.
2. Monitor load of 75 Ω with R_{ext} = 21 Ω and R_{bias} = 15 kΩ at 3.3 V application.
3. Monitor load of 75 Ω with R_{ext} = 70.6 Ω and R_{bias} = 47 kΩ at 5.0 V application.

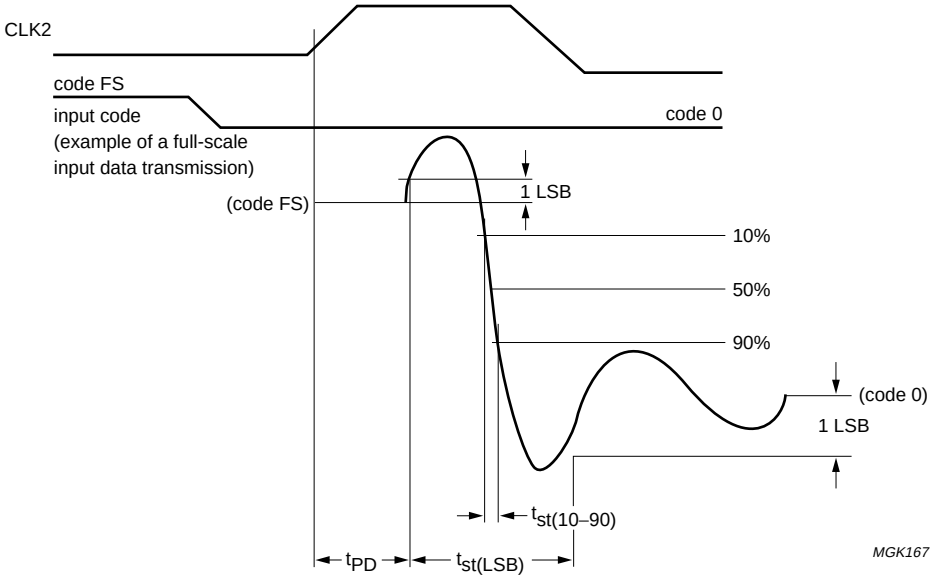


Fig.16 Switching characteristics.

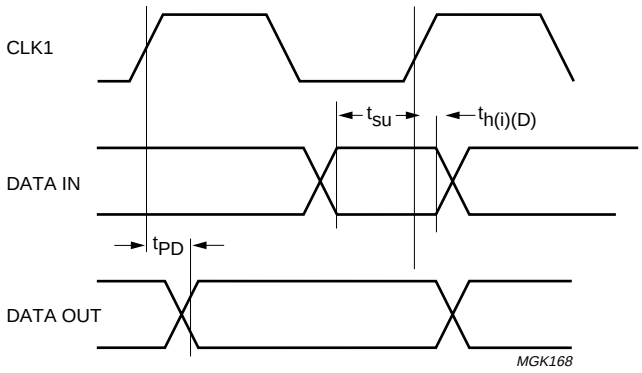


Fig.17 Data input/output timing.

PROGRAMMING

Overview available write

ADDRESS	SYMBOL	FUNCTION	FORMAT	RANGE/VALUE
0	CONTROL0	miscellaneous; see Table 4	byte	n.a.
1	CONTROL1	miscellaneous; see Table 5[1]	byte	n.a.
2	CONTROL2	miscellaneous; see Table 6	byte	n.a.
4	OB_STARTL_F0	first line optical black window in field 0	byte	0 to 255
5	OB_STARTL_F1	first line optical black window in field 1/frame	byte	0 to 255
7	OB_STARTP	first pixel optical black window	byte	0 to 255
8	OB_PE_F0	fixed optical black level for even pixel in field 0	byte	0
9	OB_PO_F0	fixed optical black level for odd pixel in field 0	byte	0
10	OB_PE_F1	fixed optical black level for even pixel in field 1/frame	byte	0
11	OB_PO_F1	fixed optical black level for odd pixel in field 1/frame	byte	0
12	OB_OFFSET_LE	optical black offset for even line	byte	0
13	OB_OFFSET_LO	optical black offset for odd line	byte	0
14	MOSAIC_SEP_S1	multiplication-factor for Yn at even line and even pixel	byte	0 to 255
15	MOSAIC_SEP_S2	multiplication-factor for Yn at even line and odd pixel	byte	0 to 255
16	MOSAIC_SEP_S3	multiplication-factor for Yn at odd line and even pixel	byte	0 to 255
17	MOSAIC_SEP_S4	multiplication-factor for Yn at odd line and odd pixel	byte	0 to 255
18	WHITE_CLIP_THR	threshold for white clip	byte	768 to 1023
19	COL_MAT_P11	colour matrix coefficient p11	byte	−128 to 127
20	COL_MAT_P12	colour matrix coefficient p12	byte	−128 to 127
21	COL_MAT_P13	colour matrix coefficient p13	byte	−128 to 127
22	COL_MAT_P21	colour matrix coefficient p21	byte	−128 to 127
23	COL_MAT_P22	colour matrix coefficient p22	byte	−128 to 127
24	COL_MAT_P23	colour matrix coefficient p23	byte	−128 to 127
25	COL_MAT_P31	colour matrix coefficient p31	byte	−128 to 127
26	COL_MAT_P32	colour matrix coefficient p32	byte	−128 to 127
27	COL_MAT_P33	colour matrix coefficient p33	byte	−128 to 127
28	COL_MAT_RGAIN	colour matrix R-gain factor[1]	byte	0 to 255
29	COL_MAT_BGAIN	colour matrix B-gain factor[1]	byte	0 to 255
34	BLACK_LEVEL_R	fixed R-black level offset[1]	byte	−128 to 127
35	BLACK_LEVEL_G	fixed G-black level offset[1]	byte	−128 to 127
36	BLACK_LEVEL_B	fixed B-black level offset[1]	byte	−128 to 127
37	RGB_KNEE_OFFSET	offset for RGB-knee[1]	byte	0 to 255
38	GAMMA_BALANCE	gamma multiplication factor (LS)[1]	6 bits	0 to 63

ADDRESS	SYMBOL	FUNCTION	FORMAT	RANGE/VALUE
39	NPIX_LSB	number of pixels on a line	byte	0 to 255
40	NPIX_MSB	number of pixels on a line	2 bits	0 to 3
41	FPIX_ACT	number of first active pixel on a line	byte	0 to 255
42	LPIX_ACT_LSB	number of last active pixel on a line	byte	0 to 255
43	FLINE_ACT_F0	number of first active line in field 0	byte	0 to 255
44	LLINE_ACT_F0_LSB	number of last active line in field 0	byte	0 to 255
45	FLINE_ACT_F1_LSB	number of first active line in field 1/frame	byte	0 to 255
46	LLINE_ACT_F1_LSB	number of last active line in field 1/frame	byte	0 to 255
47	ACT_LINES_MSB	MSBs of active line numbers	byte	see Table 7
48	CTR_UPD_LINE	number of line for double buffered update control registers	byte	0 to 255
49	KCOMB	vertical contour comb filter coefficient (MS)	3 bits	0 to 7
	VCGAIN	vertical contour gain (LS)	4 bits	0 to 15
50	CLDLEV	contour level dependancy level(1)	byte	0 to 255
51	HCHGAIN	horizontal contour band pass filter high gain (MS)	4 bits	0 to 15
	HCLGAIN	horizontal contour band pass filter low gain (LS)	4 bits	0 to 15
52	CNCLEV	contour noise coring level(1)	6 bits	0 to 63
53	CONGAIN	contour gain factor	byte	0 to 63
54	FCDLEV	false colour detect level	byte	0 to 255
55	YNCLEV	Y (luminance) noise coring level	byte	0 to 127
56	YGAIN	Y (luminance) gain factor(1)	byte	0
57	YCMPDEL	Y (luminance) compensation delay	4 bits	–3 to 4 see Table 8
58	UVNCLEV	UV (chrominance) noise coring level	byte	0 to 255
59	UGAIN	U(B – Y) gain factor(1)	byte	0
60	VGAIN	V(R – Y) gain factor(1)	byte	0
61	DTO_FREQ_LSB	DTO frequency (MSB)(1)	byte	0 to 255
62	DTO_FREQ_ISB	DTO frequency(1)	byte	0 to 255
63	DTO_FREQ_MSB	DTO frequency (LSB)(1)	byte	0 to 255
64	PHASESHIFT	PHASE_SHIFT colour subcarrier	byte	0 to 255
65	BURST_LEVEL	BURST_LEVEL colour burst	byte	0 to 255
66	A	AWB_A (ME)	byte	–98
		pole_thresh #A (DPD)	byte	0 to 255
67	B	AWB_B (ME); pole_thresh #B (DPD)	byte	–104
68	C	AWB_C (ME); pole_thresh #A (DPD)	byte	–68
69	D	AWB_D (ME); pole_thresh #B (DPD)	byte	126
70	E	AWB_E (ME)	6 bits	63
		pole_thresh #A (DPD)	byte	63
71	F	AWB_F (ME)	6 bits	0
		pole_thresh #B (DPD)	byte	0
72	HIGHLIGHTTHR	highlight-threshold (ME); pole_thresh #A(DPD)	byte	60

ADDRESS	SYMBOL	FUNCTION	FORMAT	RANGE/VALUE
73	ME_RESSCALE	ME_sync + ME_Resultscale (ME)	4 bits	0, 1 see Table 9
		pole_thresh #B (DPD)	byte	0 to 255
74	MWHVGRID	measurement horizontal and vertical grid	6 bits	see Table 10
78	WHITECLIP	white clip limiter level for analog outputs	byte	256 + (0 to 255)
79	AUTO_BLACK	auto black attack slope control	2 bits	see Table 20
82	DOP_CNTRL0	digital output processing control	byte	see Table 11
83	DOP_CNTRL1	digital output processing control(1)	byte	see Table 12
84	CIF_WSTRT	CIF-window start pixel (LSBs)	byte	0 to 255
85	CIF_WSTRT	CIF-window start line (LSBs)	byte	0 to 255
86	PRE_SI_LSB	control data for analog preprocessing	byte	0 to 255
87	PRE_SI_MSB	control data/address for analog preprocessing	5 bits	see Table 13
88	SMP_CNTRL	control for switched mode power supply	byte	0
89	PRE_CNTRL	preprocessing/timing control	byte	see Table 14
90	DIG_SETUP	set-up in digital output	byte	0.255
91	BLANKLEV	blanking level in analog output	byte	0 to 255
92	BL-SETUP	set-up level in analog output	byte	0 to 255
93	AOF_CNTRL	analog output format control(1)	byte	see Table 15
94	PRE_PROC_DEL	control compensation delay W.I.L preprocessing	4 bits	0 to 15
126	RAMWRPTR	write pointer for RAM work-space	byte	0 to 223
127	RAMWRDATA	write data for RAM work-space	byte	0 to 255

Note

1. Double buffered write register.

Register details

Table 4 CONTROL0

NAME.BITNR	NAME	FUNCTION
CONTROL0.0	AUTO_OPT_BLACK	Auto Optical Black ON/OFF
CONTROL0.1	SENS_VGA	RGB-bayer/complementary mosaic colour filter
CONTROL0.2	MOSAIC_FIL_TYPE	complementary mosaic colour filter
CONTROL0.3	PIX_PHASE	toggle phase for pixel in colour separation
CONTROL0.4	LINE_PHASE	toggle phase for line in colour separation
CONTROL0.5	FIELD_PHASE	toggle phase for field in colour separation

Table 5 CONTROL1

NAME.BITNR	NAME	FUNCTION
CONTROL1.2	RGB_KNEE_K	compression factor for RGB-knee (see Table 16)(1)
CONTROL1.3	RGB_KNEE_K	compression factor for RGB-knee (see Table 16)(1)
CONTROL1.4	MED_RES	medium resolution for PAL/NTSC encoder
CONTROL1.5	PAL_NTSC	choose between PAL/NTSC
CONTROL1.6	BSSCALE	black stretch scaling factor (see Table 17)(1)
CONTROL1.7	BSSCALE	black stretch scaling factor (see Table 17)(1)

Note

1. Double buffered write register.

Table 6 CONTROL2

NAME.BITNR	NAME	FUNCTION
CONTROL2.0	FCC_FILTER+	false colour low-pass filter ON/OFF
CONTROL2.1	NI	non-interlaced/interlaced
CONTROL2.2	DTOMWL_LSB	DTO measurement window length(1)
CONTROL2.3	DTOMWL_MSB	DTO measurement window length(1)
CONTROL2.4	WH_CL_MAP	white clip mapping on UV-grid (see Table 18)
CONTROL2.5	WH_CL_MAP	white clip mapping on UV-grid (see Table 18)
CONTROL2.6	FC_MAP	false colour mapping on UV-grid (see Table 19)
CONTROL2.7	FC_MAP	false colour mapping on UV-grid (see Table 19)

Note

1. Double buffered write register.

Table 7 ACT_LINES_MSB

NAME.BITNR	FUNCTION
ACT_LINES_MSB.0 and ACT_LINES_MSB.1	bits 8 and 9 for last active pixel number on a line
ACT_LINES_MSB.2 and ACT_LINES_MSB.3	bits 8 and 9 for last active line number in field 0
ACT_LINES_MSB.4 and ACT_LINES_MSB.5	bits 8 and 9 for first active line number in field 1/frame
ACT_LINES_MSB.6 and ACT_LINES_MSB.7	bits 8 and 9 for last active line number in field 1/frame

Table 8 YCMPDEL

CONTENT	FUNCTION $(1 + 4 \times B3 + B2 + 2 \times B1 + 1 \times B0) \times t_d$
0000	$1t_d$
0001	$2t_d$
0010	$3t_d$
0011	$4t_d$
0100	$5t_d$
0101	$6t_d$
0110	$7t_d$
0111	$8t_d$
1000	$5t_d$
1001	$6t_d$
1010	$7t_d$
1011	$8t_d$
1100	$9t_d$
1101	$10t_d$
1110	$11t_d$
1111	$12t_d$

Table 9 MECNTRL

NAME.BITNR	FUNCTION	DEFAULT
MECNRTL.0, MECNRTL.1, MECNRTL.2	ME_Resultscaler selection (0, 2, 4, 8, 16, 32)	1
MECNRTL.3	ME_Sync (synchronize field/frame toggle of measurement engine)	0

Table 10 MWHVGRID

NAME.BITNR	FUNCTION	DEFAULT
MWHVGRID.0, MWHVGRID.1, MWHVGRID.2 and MWHVGRID.3	horizontal ME-window pixel size selection	4
MWHVGRID.4 and MWHVGRID.5	vertical ME-window pixel size selection	4

Table 11 DOP_CNTRL0

NAME.BITNR	FUNCTION
DOP_CNTRL0.0 and DOP_CNTRL0.1	horizontal CIF-processing control bits HCIF.0 and HCIF.1 (see Table 21)
DOP_CNTRL0.2 and DOP_CNTRL0.3	vertical CIF-processing control bits VCIF.0 and VCIF.1 (see Table 22)
DOP_CNTRL0.4 and DOP_CNTRL0.5	temporal CIF-processing control bits TCIF.0 and TCIF.1 (see Table 23)
DOP_CNTRL0.6	CIF-processing enabled/disabled (by-pass)
DOP_CNTRL0.7	CIF-format/QCIF format

Table 12 DOP_CNTRL1

NAME.BITNR	FUNCTION	DEFAULT
DOP_CNTRL1.0 and DOP_CNTRL1.1	horizontal pixel start MSBs for CIF-window	–
DOP_CNTRL1.2 and DOP_CNTRL1,3	vertical line start MSBs for CIF-window	–
DOP_CNTRL1.4	PXQ-output/CREF-output	–
DOP_CNTRL1.5	CIF-sensor applied/non CIF-sensor applied	–
DOP_CNTRL1.6	d1/d2 output format	–
DOP_CNTRL1.7	DOP-processing active/disabled	1

Table 13 PRE_SI_MSB

NAME.BITNR	FUNCTION
PRE_SI_MSB.0 and PRE_SI_MSB.1	control data bits d8 and d9
PRE_SI_MSB.2 to PRE_SI_MSB.4	control address bits a0 to a2

Table 14 PRE_CNTRL

NAME.BITNR	FUNCTION
PRE_CNTRL.0 to PRE_CNTRL.5	control DAC-data bits 0 to 5
PRE_CNTRL.6 and PRE_CNTRL.7	static control outputs P0 and P1

Table 15 AOF_CNTRL

NAME.BITNR	FUNCTION	DEFAULT
AOF_CNTRL.0 and AOF_CNTRL.1	analog output format selection (see Table 24)	1
AOF_CNTRL.2 and AOF_CNTRL.3	scale factor #1 for GY-multiplex (see Table 25)	–
AOF_CNTRL.4 and AOF_CNTRL.5	scale factor #2 for BU-, C- and RV-multiplex (see Table 26)	–
AOF_CNTRL.6	analog output processing active/disabled	1
AOF_CNTRL.7	triple DAC output range control large/small	–

Table 16 Knee compression factors

W 1.n		COMPRESSION FACTOR
n = 3	n = 2	
0	0	$\frac{1}{8}$
0	1	$\frac{1}{4}$
1	0	$\frac{3}{8}$
1	1	$\frac{1}{2}$

Table 17 Black stretch scaling factors

W 1.n		SCALING FACTOR
n = 7	n = 6	
0	0	0
0	1	$\frac{1}{4}$
1	0	$\frac{1}{2}$
1	1	$\frac{3}{4}$

Table 18 White-clip detection spreading

W 2.n		SPREADING FILTER
n = 5	n = 4	
0	0	[0 0 1 0 0]
0	1	[0 1 1 1 0]
1	X	[1 1 1 1 1]

Table 19 False colour detection spreading

W 2.n		SPREADING FILTER
n = 7	n = 6	
0	0	[0 0 1 0 0]
0	1	[0 1 1 1 0]
1	X	[1 1 1 1 1]

Table 20 Auto black attack slope control

W 79.n		SLOPE FACTOR
n = 7	n = 6	
0	0	$^1/_4$
0	1	$^1/_8$
1	0	$^1/_{16}$
1	1	$^1/_{32}$

Table 21 HCIF-control

W 82.n		SLOPE FACTOR
n = 1	n = 0	
0	0	down-sample by 4
0	1	down-sample by 2
1	X	one-to-one copy

Table 22 VCIF-control

W 82.n		PROCESSING
n = 3	n = 2	
0	0	down-sample by 4
0	1	down-sample by 2
1	0	one-to-one copy
1	1	up-sample by 2

Table 23 TCIF-control

W 82.n		PROCESSING
n = 5	n = 4	
0	0	one-to-one copy
0	1	down-sample by 2
1	0	down-sample by 4
1	1	down-sample by 8

Table 24 Analog output format selection

W 93.n		FORMAT
n = 1	n = 0	
0	0	RGB
0	1	YUV
1	0	YC
1	1	CVBS

Table 25 Scale #1 selection

W 93.n		SCALE FACTOR
n = 3	n = 2	
0	X	1
1	0	2
1	1	$^3/_2$

Table 26 Scale #2 selection

W 93.n		SCALE FACTOR
n = 5	n = 4	
0	X	1
1	0	2
1	1	$^3/_2$

APPLICATION INFORMATION

TDA8786 and SAA8110G can be used with Sharp CCDs. TDA8786A and SAA8110G can be used with Sony CCDs. Table 27 gives as an example some references of ICs which may be used with Philips TDA8786(A)/SAA8110G. This overview is not restrictive, both devices are compatible with other CCD/V-driver/PPG combinations including the more recent ones.

Table 27 Possible components for the application of Figs 18 and 19.

CCD TYPE	COMPONENT TYPE	NTSC		PAL	
		MEDIUM RESOLUTION	HIGH RESOLUTION	MEDIUM RESOLUTION	HIGH RESOLUTION
SONY CCDs	CCD	LZ2313H5	LZ2353A	LZ2323H5	LZ2363
	V-driver	LR36683N			
	timing generator	LZ95G55	LZ95G71	LZ95G55	LZ95G71
SHARP CCDs	CCD	ICX056AK	ICX068AK	ICX057AK	ICX069AK
	V-driver	CXD1250MN; CXD1267N			
	timing generator	CXD1257AR	CXD1265R	CXD1257AR	CXD1265R

Notes to the application diagram

- In the configuration of Figs 18 and 19, the microcontroller reads and writes data from/to the DSP using the SNERT-bus (UART-mode 0). Optional external control is available through the I^2C-bus.
- Free I/O pins of the microcontroller can be used to control PGG, or for other purposes.
- 83Cxxx processing is synchronized by VD interruption. Depending on VD polarity, it can be necessary to invert VD.
- A customized 83Cxxx is available for this application. Please contact your nearest Philips sales office.

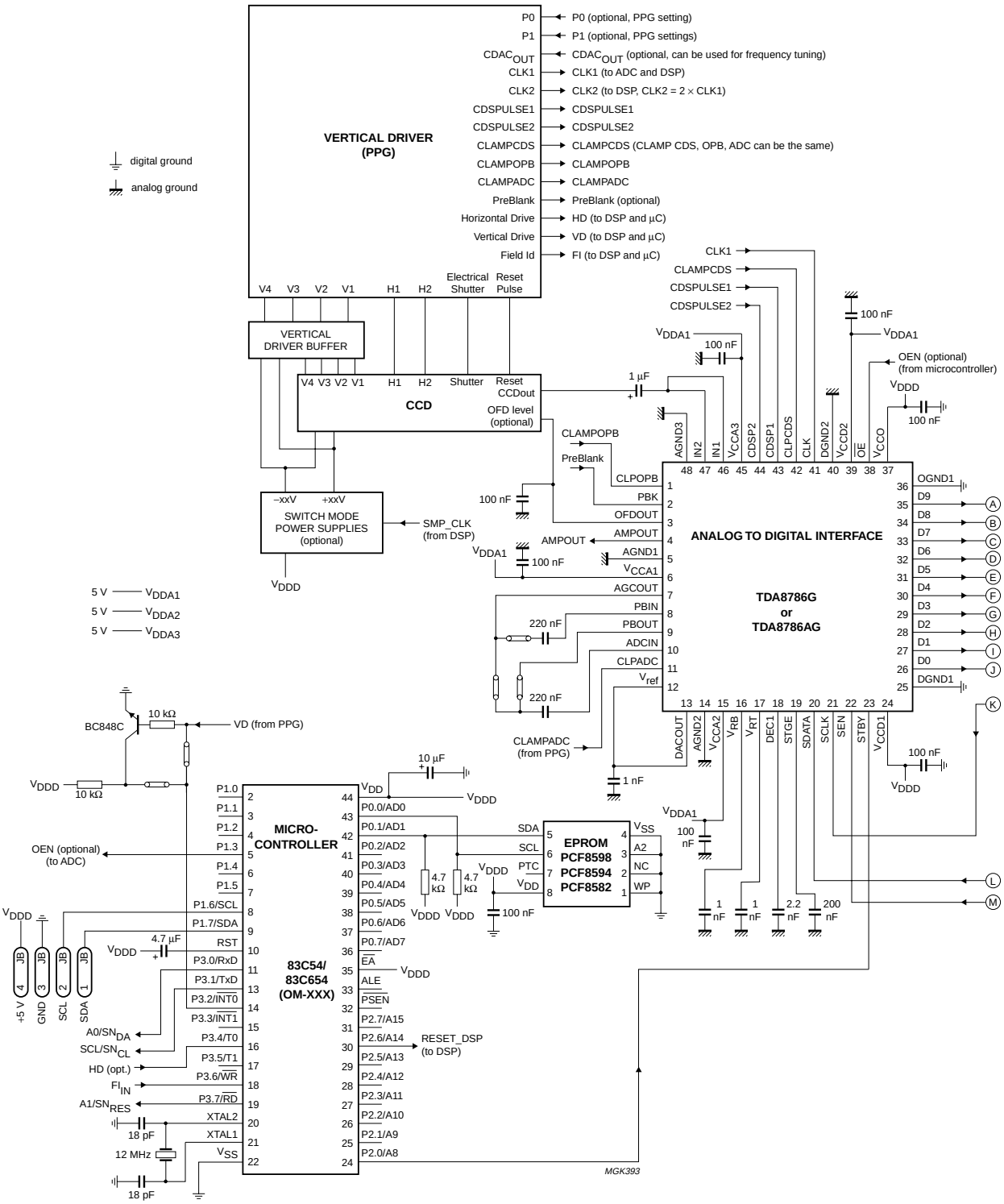
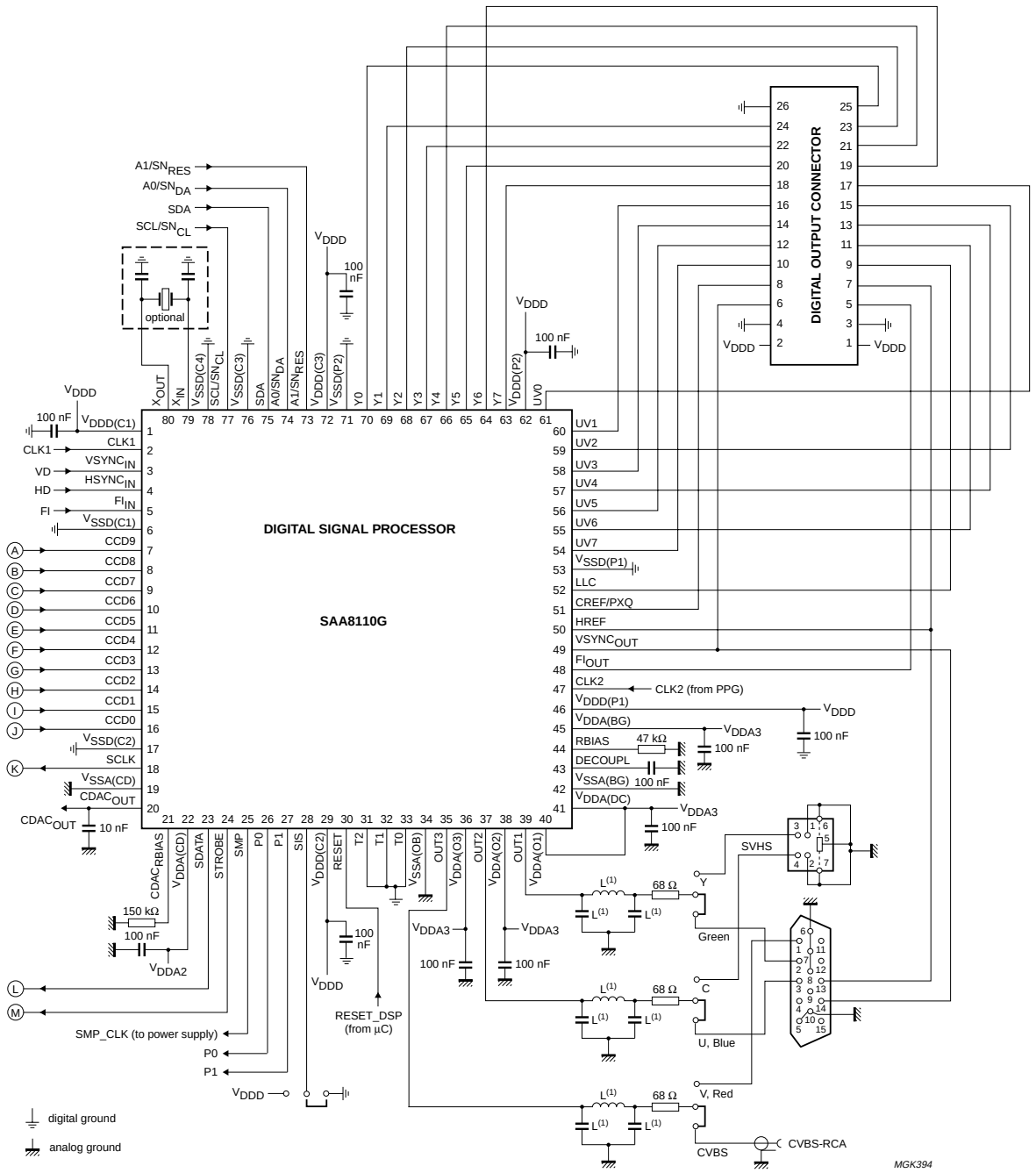


Fig.18 SAA8110G system configuration for camera application (continued in Fig.19).

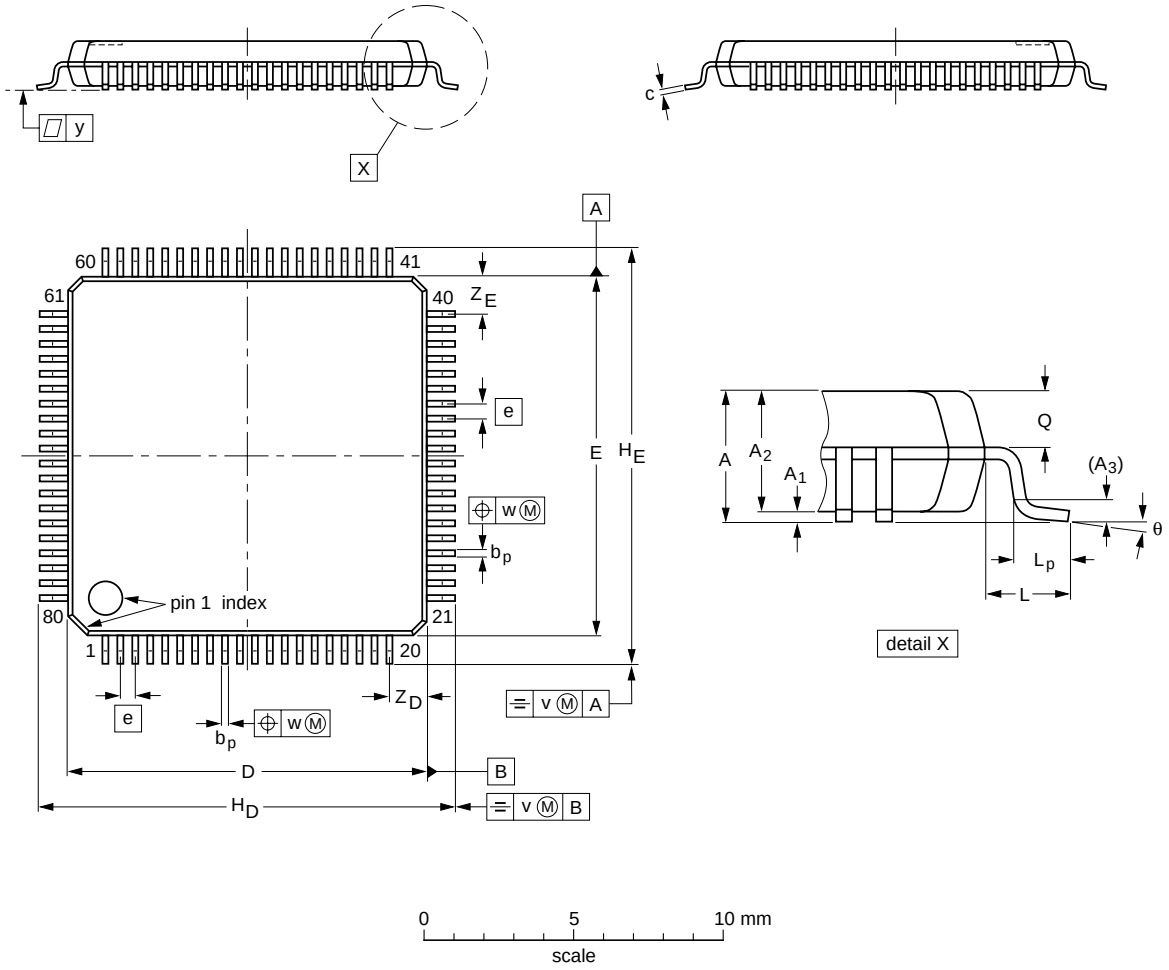


(1) Values depend on DSP output configuration.

Fig.19 SAA8110G system configuration for camera application (continued from Fig.18).

PACKAGE OUTLINE

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.25 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1.0	0.7 0.3	0.70 0.58	0.2	0.15	0.1	1.45 1.05	1.45 1.05	4^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT315-1						~~92-03-24~~ 95-12-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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Printed in The Netherlands 547047/1200/01/pp36 Date of release: 1997 Jun 13 Document order number: 9397 750 01576

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