SCAN921821 Dual 18-Bit Serializer with Pre-emphasis, IEEE 1149.1 (JTAG), and At-Speed BIST

Check for Samples: SCAN921821

FEATURES

- **15-66 MHz Dual 18:1 Serializer with 2.376 Gbps Total Throughput**
- **8-level Selectable Pre-emphasis on Each Channel Drives Lossy Cables and Backplanes**
- **>15kV HBM ESD Protection on Bus LVDS I/O Pins**
- **Robust BLVDS Serial Data Transmission with Embedded Clock for Exceptional Noise Immunity and Low EMI**
- **Power Saving Control Pin for Each Channel**
- **IEEE 1149.1 "JTAG" Compliant**
- **At-Speed BIST - PRBS Generation**
- **No External Coding Required**
- **Internal PLL, No External PLL Components Required**
- **Single +3.3V Power Supply**
- **Low Power: 260 mW (typ) Per Channel at 66 MHz with PRBS-15 Pattern**
- **Single 3.3 V Supply**
- **Fabricated with Advanced CMOS Process Technology**
- **Industrial −40 to +85°C Temperature Range**
- **Compact 100-ball NFBGA Package**

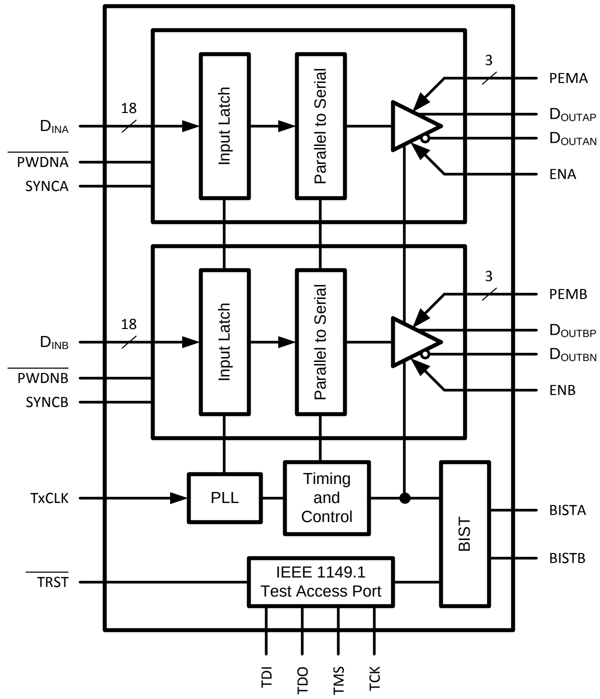
DESCRIPTION

The SCAN921821 is a dual channel 18-bit serializer featuring signal conditioning, boundary SCAN, and at-speed BIST. Each serializer block transforms an 18-bit parallel LVCMOS/LVTTL data bus into a single Bus LVDS data stream with embedded clock. This single serial data stream with embedded clock simplifies PCB design and reduces PCB cost by narrowing data paths that in turn reduce PCB size and layers. The single serial data stream also reduces cable size, the number of connectors, and eliminates clock-to-data and data-to-data skew.

Each channel also has an 8-level selectable pre-emphasis feature that significantly extends performance over lossy interconnect. Each channel also has its own powerdown pin that saves power by reducing supply current when the channel is not being used.

The SCAN921821 also incorporates advanced testability features including IEEE 1149.1 and at-speed BIST PRBS pattern generation to facilitate verification of board and link integrity

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1][2]

Supply Voltage (V_{DD})			−0.3V to +4V
Supply Voltage (V_{DD}) Ramp Rate			< 30 V/ms
LVCMOS/LVTTL Input Voltage			−0.3V to (V_{DD} +0.3V)
LVCMOS/LVTTL Output Voltage			−0.3V to (V_{DD} +0.3V)
Bus LVDS Driver Output Voltage			−0.3V to +3.9V
Bus LVDS Output Short Circuit Duration			10ms
Junction Temperature			+150°C
Storage Temperature			−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)			+220°C
Maximum Package Power Dissipation at 25°C		NFBGA-100	3.57 W
		Derating Above 25°C	28.57 mW/°C
Thermal resistance		θ_{JA}	35°C/W
		θ_{JC}	11.1°C/W
ESD Rating	HBM, 1.5 KΩ, 100 pF	All pins	>8 kV
		Bus LVDS pins	>15 kV
	MM, 0Ω, 200 pF		>1200 V
	CDM		>2 kV

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{DD})	3.15	3.3	3.45	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C
Clock Rate	15		66	MHz
Supply Noise			100	mV p-p

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS/LVTTL Input DC Specifications						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA	−1.5	-0.7		V
I_{INH}	High Level Input Current	$V_{IN} = V_{DD} = V_{DDMAX}$	−20	±2	+20	µA
I_{INL}	Low Level Output Current	$V_{IN} = V_{SS}$, $V_{DD} = V_{DDMAX}$	−10	±2	+10	µA
1149.1 (JTAG) DC Specifications						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA	−1.5	-0.7		V
I_{INH}	High Level Input Current	$V_{IN} = V_{DD} = V_{DDMAX}$	-20		+20	µA
I_{INL}	Low Level Output Current	$V_{IN} = V_{SS}$, $V_{DD} = V_{DDMAX}$	-200		+200	µA
V_{OH}	High Level Output Voltage	I_{OH} = −9 mA	2.3		V_{DD}	mV
V_{OL}	Low Level Output Voltage	I_{OL} = 9 mA	GND		0.5	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V	-100	-80	-50	mA
I_{OZ}	Output Tri-state Current	$\overline{PWDN}$ or EN = 0.8V, V_{OUT} = 0 V	-10		+10	µA
		$\overline{PWDN}$ or EN = 0.8V, V_{OUT} = VDD	-30		+30	µA
Bus LVDS Output DC Specifications						
V_{OD}	Output Differential Voltage (DO+) - (DO-)	See Figure 10, R_L = 100Ω	450	500	550	mV
ΔV_{OD}	Output Differential Voltage Unbalance			2	15	mV
V_{OS}	Offset Voltage		1.05	1.2	1.25	V
ΔV_{OS}	Offset Voltage Unbalance			2.7	15	mV

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Q_{POV}	Pre-Emphasis Output Voltage Ratio $\| V_{ODPRE} / V_{OD} \|$	Pre-Emphasis Level = 1	1.10	1.24	1.35	
		Pre-Emphasis Level = 2	1.35	1.47	1.55	
		Pre-Emphasis Level = 3	1.55	1.70	1.80	
		Pre-Emphasis Level = 4	1.80	1.91	1.95	
		Pre-Emphasis Level = 5	1.95	2.08	2.20	
		Pre-Emphasis Level = 6	2.10	2.21	2.35	
		Pre-Emphasis Level = 7	2.15	2.30	2.50	
I_{OS}	Output Short Circuit Current	DO = 0V, Din = H, $\overline{PWDN}$ and EN = 2.4V	-10	-25	-75	mA
I_{OZ}	TRI-STATE Output Current	$\overline{PWDN}$ or EN = 0.8V, DO = 0V (3)	-10	± 1	+10	µA
		$\overline{PWDN}$ or EN = 0.8V, DO = VDD (3)	-55	± 6	+55	µA
Power Supply Current (DVDD, PVDD and AVDD Pins)						
I_{DD}	Total Supply Current (includes load current)	C_L = 15pF, R_L = 100 Ω; f = 66 MHz, PRBS-15 Pattern		160	225	mA
		C_L = 15pF, R_L = 100 Ω; f = 66 MHz, Worst Case Pattern (Checker-Board Pattern)		180		mA
I_{DDP}	Total Supply Current with Pre-Emphasis (includes load current)	C_L = 15pF, R_L = 100 Ω; f = 66 MHz, PRBS-15 Pattern		240		mA
		C_L = 15pF, R_L = 100 Ω; f = 66 MHz, Worst Case Pattern (Checker-Board Pattern)		280	325	mA
I_{DDX}	Supply Current Powerdown	$\overline{PWDN}$ = 0.8V, EN = 0.8V		1.0	3.0	mA

(3) I_{OZ} is measured at each pin. The DOUT pin not under test is floated to isolate the TRI-STATE current flow.

Timing Requirements for TCLK

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TCP}	Transmit Clock Period		15.2	T	66.7	ns
t_{TCIH}	Transmit Clock High Time		0.4T	0.5T	0.6T	ns
t_{TCIL}	Transmit Clock Low Time		0.4T	0.5T	0.6T	ns
t_{CLKT}	TCLK Input Transition Time			3	6	ns
t_{JIT}	TCLK Input Jitter	See (3)			80	ps (RMS)

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.
(3) Specified by design using statistical analysis.

AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.[(1)(2)]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Serializer AC Specifications						
t_{LLHT}	Bus LVDS Low-to-High Transition Time	See Figure 2, [(3)] R_L = 100Ω, C_L=10pF to GND		0.3	0.4	ns
t_{LHLT}	Bus LVDS High-to-Low Transition Time			0.3	0.4	ns
t_{DIS}	DIN (0-17) Setup to TCLK	See Figure 4, [(3)] R_L = 100Ω, C_L=10pF to GND	1.9			ns
t_{DIH}	DIN (0-17) Hold from TCLK		0.6			ns
t_{HZD}	DO ± HIGH to TRI-STATE Delay	See Figure 5 R_L = 100Ω, C_L=10pF to GND		3.9	10	ns
t_{LZD}	DO ± LOW to TRI-STATE Delay			3.5	10	ns
t_{ZHD}	DO ± TRI-STATE to HIGH Delay			3.2	10	ns
t_{ZLD}	DO ± TRI-STATE to LOW Delay			2.4	10	ns
t_{SPW}	SYNC Pulse Width	See Figure 7, R_L = 100Ω	5*t_{TCP}		6*t_{TCP}	ns
t_{PLD}	Serializer PLL Lock Time	See Figure 6, R_L = 100Ω	510*t_{TCP}		1024*t_{TCP}	ns
t_{SD}	Serializer Delay	See Figure 8 , R_L = 100Ω	t_{TCP} + 2.5	t_{TCP} + 4.5	t_{TCP} + 6.5	ns
t_{SKCC}	Channel to Channel Skew			70		ps
t_{RJIT}	Random Jitter	Room Temperature, V_{DD} = 3.3V, 66 MHz		6.1		ps (RMS)
t_{DJIT}	Deterministic Jitter Figure 9, [(3)]	15 MHz	-390		320	ps
		66 MHz	-60		30	ps
1149.1 (JTAG) AC Specifications						
f_{MAX}	Maximum TCK Clock Frequency	C_L = 15pF, R_L = 500 Ω	25			MHz
t_S	TDI or TMS Setup to TCK, H or L		2.4			ns
t_H	TDI or TMS Hold from TCK, H or L		2.8			ns
t_{W1}	TCK Pulse Width, H or L		10			ns
t_{W2}	$\overline{TRST}$ Pulse Width, L		10			ns
t_{REC}	Recovery Time, $\overline{TRST}$ to TCK		2			ns

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.
(3) Specified by design using statistical analysis.

AC Timing Diagrams and Test Circuits

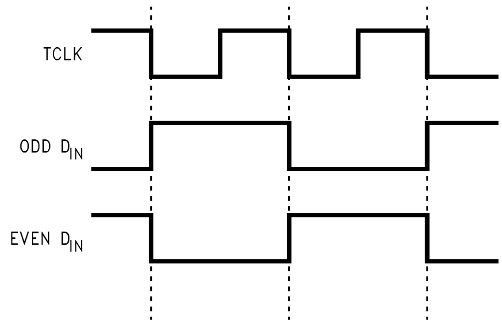


Figure 1. "Worst Case" Serializer IDD Test Pattern

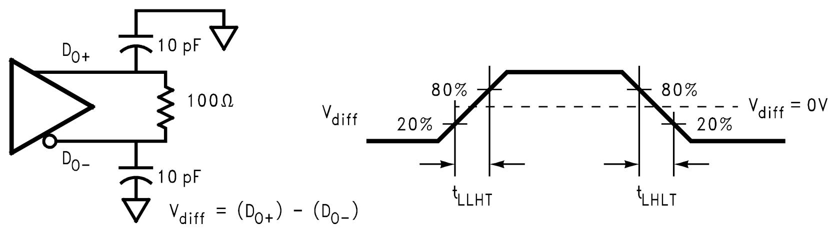


Figure 2. Serializer Bus LVDS Distributed Output Load and Transition Times

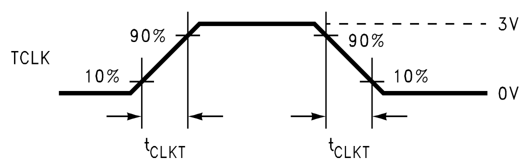


Figure 3. Serializer Input Clock Transition Time

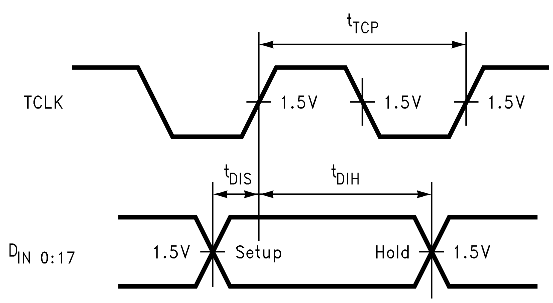


Figure 4. Serializer Setup/Hold Times

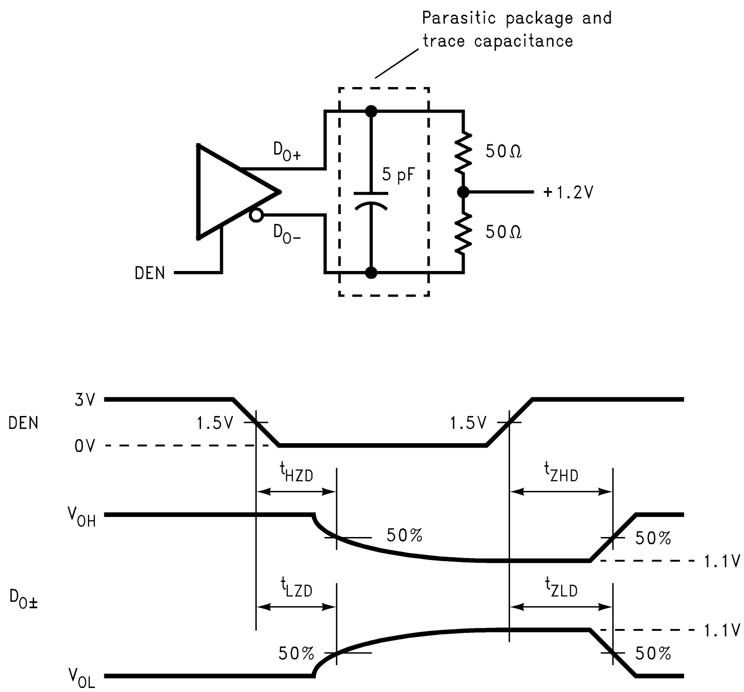


Figure 5. Serializer TRI-STATE Test Circuit and Timing

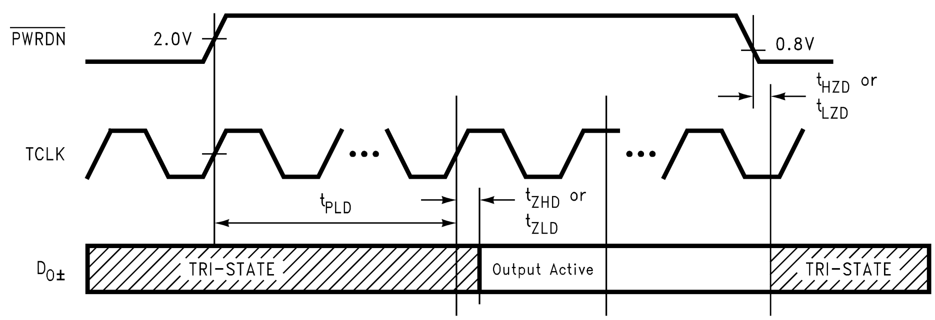


Figure 6. Serializer PLL Lock Time, and $\overline{\text{PWRDN}}$ TRI-STATE Delays

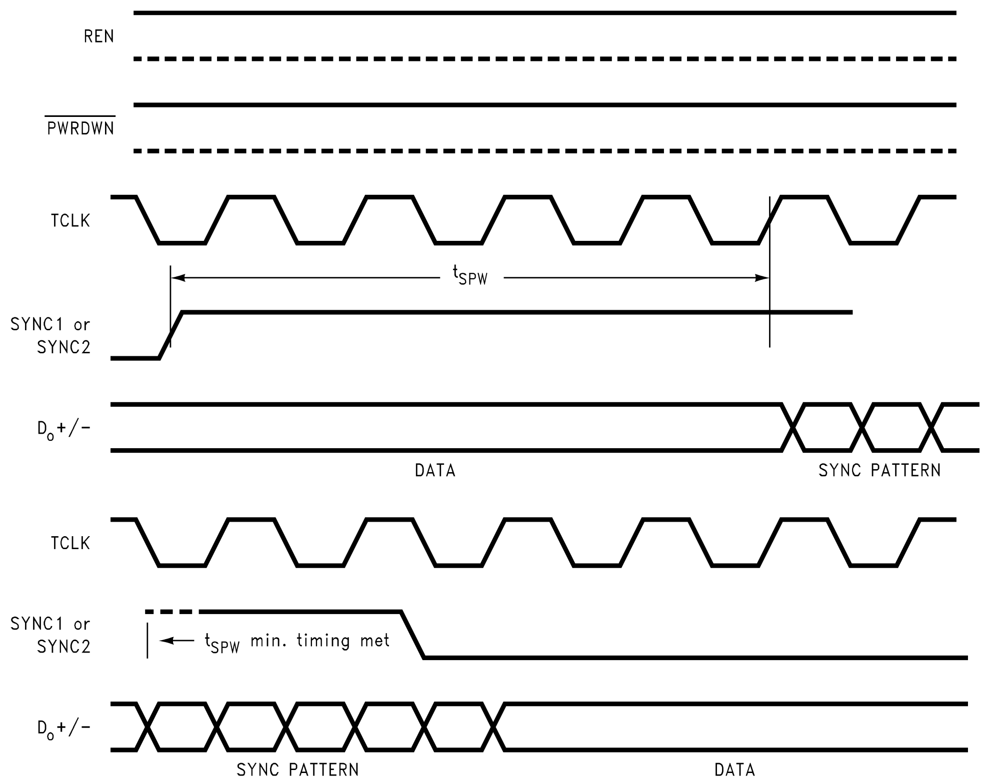


Figure 7. SYNC Timing Delay

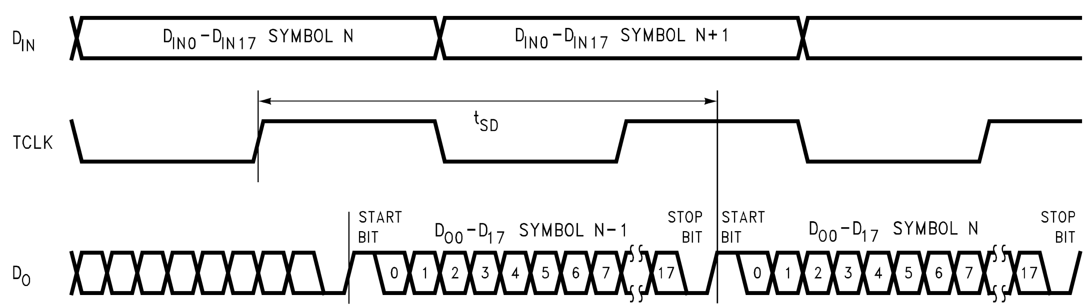


Figure 8. Serializer Delay

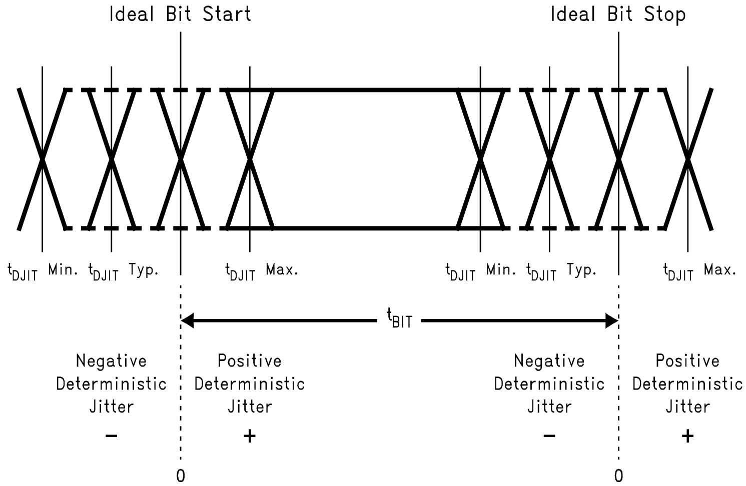
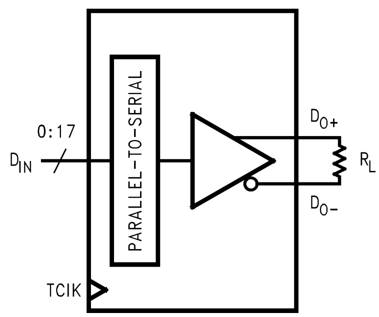


Figure 9. Deterministic Jitter and Ideal Bit Position



$V_{OD} = (DO^+)–(DO^−)$.
Differential output signal is shown as (DO+)–(DO−), device in Data Transfer mode.

Figure 10. V_{OD} Diagram

Pre-emphasis Truth Table

PEM LEVEL	PEM2	PEM1	PEM0
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L
5	H	L	H
6	H	H	L
7	H	H	H

Pin Diagram

Figure 11. SCAN921821TVV
Top View

A1 BISTB	A2 PV_{SS}	A3 DOUTBN	A4 AV_{DD}	A5 ENB	A6 AV_{DD}	A7 DOUTAN	A8 DOUTAP	A9 AV_{DD}	A10 ENA
B1 DINB16	B2 SYNCB	B3 AV_{DD}	B4 DOUTBP	B5 AV_{DD}	B6 PEMB1	B7 AV_{SS}	B8 PEMB0	B9 PEMA1	B10 BISTA
C1 DINB14	C2 DV_{DD}	C3 DV_{SS}	C4 AV_{SS}	C5 AV_{SS}	C6 AV_{SS}	C7 AV_{DD}	C8 PEMA2	C9 SYNCA	C10 DINA16
D1 DINB13	D2 DINB12	D3 DINB17	D4 DV_{DD}	D5 PV_{DD}	D6 PEMA0	D7 AV_{SS}	D8 DINA17	D9 DINA15	D10 DINA13
E1 DINB11	E2 DINB9	E3 DINB15	E4 DV_{SS}	E5 DINB8	E6 PEMB2	E7 DV_{SS}	E8 DINA14	E9 DINA12	E10 DINA9
F1 DINB10	F2 DINB7	F3 DINB5	F4 DV_{SS}	F5 PV_{DD}	F6 DINA11	F7 DV_{SS}	F8 DINA4	F9 DINA10	F10 DINA8
G1 DINB6	G2 DINB4	G3 DINB2	G4 DV_{SS}	G5 DV_{DD}	G6 DV_{DD}	G7 DINA1	G8 DINA2	G9 DINA7	G10 DINA6
H1 DINB3	H2 DINB1	H3 TxCLK	H4 DV_{SS}	H5 TCK	H6 PV_{DD}	H7 PV_{SS}	H8 DV_{SS}	H9 DINA0	H10 DINA5
J1 DINB0	J2 PWDNA	J3 DV_{DD}	J4 TRST	J5 PV_{DD}	J6 PV_{SS}	J7 PV_{DD}	J8 NC	J9 DV_{DD}	J10 DINA3
K1 DV_{SS}	K2 TDI	K3 TMS	K4 DV_{SS}	K5 TDO	K6 DV_{DD}	K7 PV_{SS}	K8 PV_{SS}	K9 PWDNB	K10 DV_{DD}

Pin Descriptions

Pin Name	Pin Count	I/O, Type	Description
DATA PINS			
DINA0-17	18	I, LVCMOS	Transmitter inputs. There is a pull-down circuitry on each of these pins which are active if respective $\overline{PWDNA}$ or $\overline{PWDNB}$ pin is pulled high.
DINB0-17	18		
DOUTAP	1	O,BLVDS	Inverting and non-inverting differential transmitter outputs.
DOUTAN	1		
DOUTBP	1		
DOUTAN	1		
TIMING AND CONTROL PINS			
TxCLK	1	I, LVCMOS	Transmitter reference clock. Used to strobe data at the inputs and to drive the transmitter PLL. There is a pull-up circuitry on this pin which is always active.
ENA	1	I, LVCMOS	Transmitter outputs enable pins. There is a pull-down circuitry on each of these pins that are active if corresponding $\overline{PWDNA}$ or $\overline{PWDNB}$ pin is pulled high. When these pins are set to LOW, the transmitter outputs will be disabled. The PLL will remain locked.
ENB	1		
$\overline{PWDNA}$	1	I, LVCMOS	Stand-by mode pins. There is a pull-down circuitry on each of these pins that are always active. When these pins are set to LOW, the transmitter will be put in low power mode and the PLL will lose lock.
$\overline{PWDNB}$	1		
SYNCA	1	I, LVCMOS	Transmitter synchronization pins. There is a pull-down circuitry on each of these pins that are active if corresponding $\overline{PWDNA}$ or $\overline{PWDNB}$ pin is pulled high. When these pins are set to HIGH, the transmitter will ignore incoming data and send SYNC patterns to provide a locking reference to receiver(s).
SYNCB	1		
PRE-EMPHASIS PINS			
PEMA0-2	3	I, LVCMOS	8-level pre-emphasis selection pins. There is a pull-down circuitry on each of these pins which are active if corresponding $\overline{PWDNA}$ or $\overline{PWDNB}$ pin is pulled high.
PEMB0-2	3		
JTAG PINS			
TDI	1	I, LVCMOS	Test Data Input to support IEEE 1149.1. There is a pull-up circuitry on this pin which is always active.
TDO	1	O, LVCMOS	Test Data Output to support IEEE 1149.1.
TMS	1	I, LVCMOS	Test Mode Select Input to support IEEE 1149.1. There is a pull-up circuitry on this pin which is always active.
TCK	1	I, LVCMOS	Test Clock Input to support IEEE 1149.1. There is no failsafe circuitry on this pin.
$\overline{TRST}$	1	I, LVCMOS	Test Reset Input to support IEEE 1149.1. There is a pull-up circuitry on this pin which is always active.
BIST PINS			
BISTA	1	I, LVCMOS	BIST selection pins. These pins select which transmitter will generate a PRBS like data. There is a pull-down circuitry on these pins which are active if corresponding $\overline{PWDNA}$ or $\overline{PWDNB}$ pin is pulled high.
BISTB	1		
POWER PINS			
AVDD	6	I, POWER	Power Supply for the LVDS circuitry.
DVDD	8	I, POWER	Power Supply for the digital circuitry.
PVDD	5	I, POWER	Power Supply for the PLL and BG circuitry.
AVSS	5	I, POWER	Ground reference for the LVDS circuitry.
DVSS	10	I, POWER	Ground reference for the digital circuitry.
PVSS	5	I, POWER	Ground reference for the PLL and BG circuitry.
OTHER PINS			
NC	1	N/A	Not connected.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SCAN921821TSM	ACTIVE	NFBGA	NZD	100	240	TBD	Call TI	Call TI	-40 to 85	SCAN921821 TSM	Samples
SCAN921821TSM/NOPB	ACTIVE	NFBGA	NZD	100	240	Green (RoHS & no Sb/Br)	SNAGCU	Level-4-260C-72 HR	-40 to 85	SCAN921821 TSM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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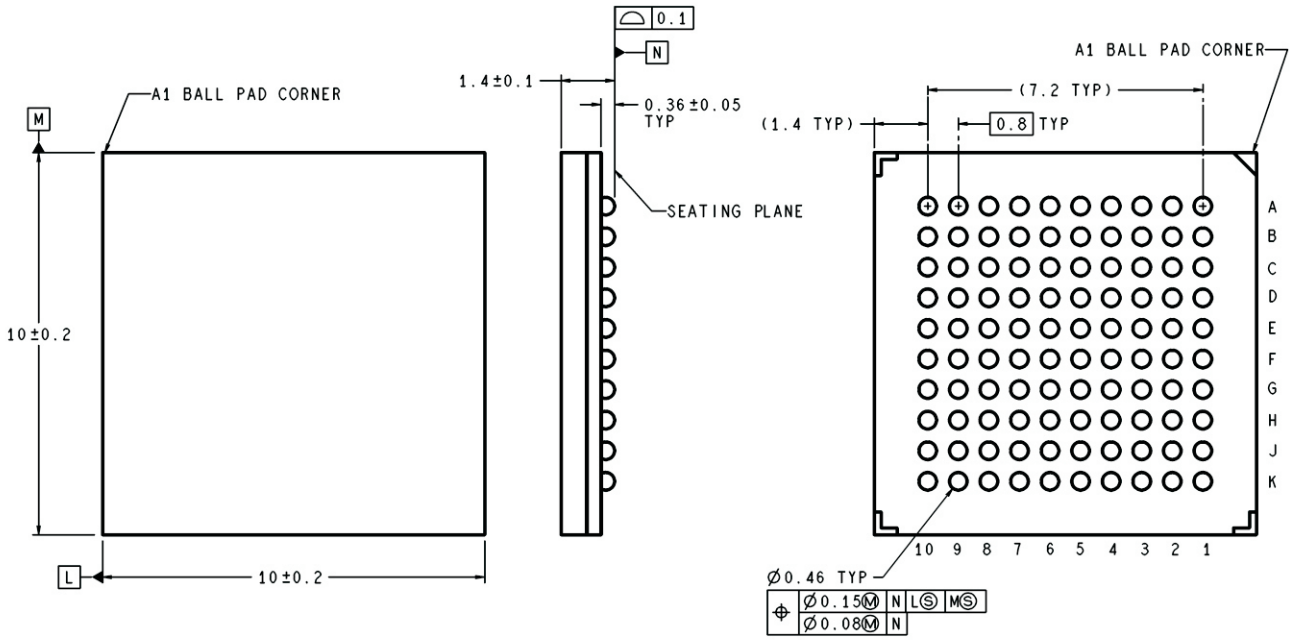

DIMENSIONS ARE IN MILLIMETERS

SLC100A (Rev B)

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