

N-CHANNEL ENHANCEMENT-MODE QUAD D-MOS FET ANALOG SWITCH ARRAYS

ORDERING INFORMATION

Sorted Chips in Waffle Pack	SD5000CHP	SD5001CHP	SD5002CHP
16-Pin Ceramic Dual In-Line Package	SD5000J	SD5001J	SD5002J
16-Pin Plastic Dual In-Line Package	SD5000N	SD5001N	SD5002N
Description	20V, 70 ohm	10V, 70 ohm	15V, 70 ohm

Note: Available in SO-14 surface mount package, refer to SD5400-02 series

FEATURES

- High Input to Output Isolation—120dB typical
- Low feedthrough and feedback transients
- Low Inter-electrode Capacitances

APPLICATIONS

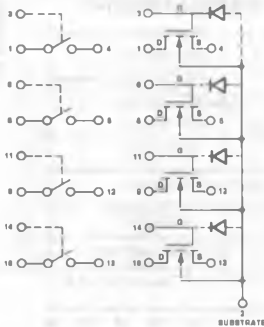
- ±10V Analog Switches—SD5000
- ±7.5V Analog Switches—SD5002
- ±5V Analog Switches—SD5001
- Sample and Hold
- Wide-Band, Dual Differential Amplifiers

ABSOLUTE MAXIMUM RATINGS (per channel, T_A = +25°C unless otherwise noted)

PARAMETER	SD5000	SD5001	SD5002	UNITS
V _{DS}	+20	+10	+15	Vdc
V _{SD}	+20	+10	+15	Vdc
V _{DB}	+25	+15	+22.5	Vdc
V _{SB}	+25	+15	+22.5	Vdc
V _{GS}	-25	-15	-22.5	Vdc
	+30	+25	+30	Vdc
V _{GB}	-0.3	-0.3	-0.3	Vdc
	+30	+25	+30	Vdc
V _{GD}	-25	-15	-22.5	Vdc
	+30	+25	+30	Vdc

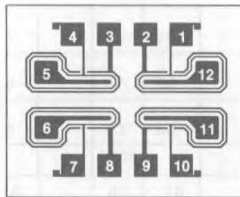
I _D	Continuous Drain Current	50mA
P _D	Total Package Power Dissipation (at or below T _A = +25°C)	640mW
	Linear Derating Factor	10.67mW/°C
P _D	Single Device Power Dissipation (at or below T _A = +25°C)	300mW
T _j	Operating Junction Temperature Range	-55 to +85°C
T _S	Storage Temperature Range	-55 to +150°C

SCHEMATIC DIAGRAM



Note: Pin numbers correspond to Package Pin-out

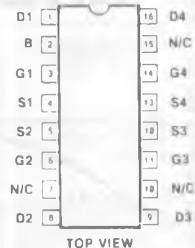
CHIP CONFIGURATION



PAD NO.	PAD FUNCTION	PAD NO.	PAD FUNCTION
1	Gate No. 1	7	Gate No. 3
2	Source No. 1	8	Source No. 3
3	Source No. 2	9	Source No. 4
4	Gate No. 2	10	Gate No. 4
5	Drain No. 2	11	Drain No. 4
6	Drain No. 3	12	Drain No. 1

Dimensions: .041 × .033 × .020 inches

PIN CONFIGURATION



DIMENSIONS

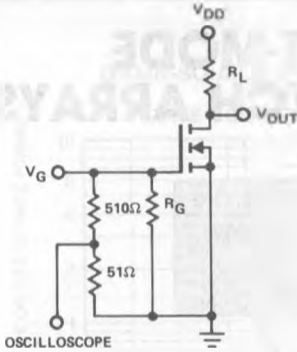
16-Pin Plastic DIP

See Package 10

16-Pin Ceramic DIP

See Package 15

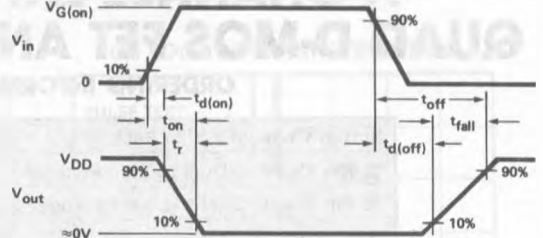
SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
 $t_r < 0.5 \text{ nSEC}$
PULSE WIDTH - 100 nSEC

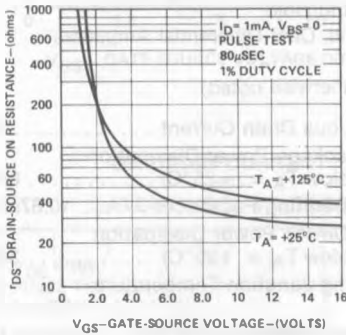
SAMPLING OSCILLOSCOPE
 $t_r < 0.38 \text{ nSEC}$
 $R_{in} > 1 \text{ M}\Omega$
 $C_{in} < 2.0 \text{ pF}$

TEST WAVEFORMS

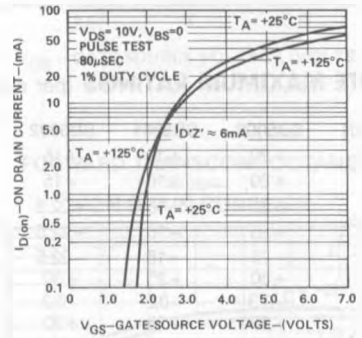


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

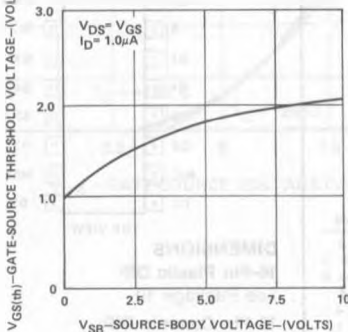
DRAIN-SOURCE ON RESISTANCE
—vs—
GATE-SOURCE VOLTAGE



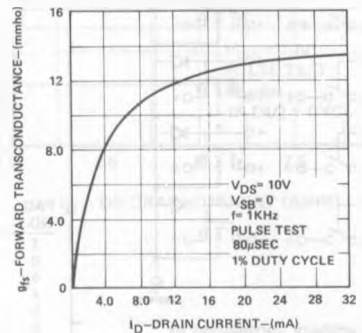
ON DRAIN CURRENT
—vs—
GATE-SOURCE VOLTAGE



GATE-SOURCE THRESHOLD VOLTAGE
—vs—
SOURCE-BODY VOLTAGE



FORWARD TRANSCONDUCTANCE
—vs—
ON DRAIN CURRENT



ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	PARAMETER	SD5000			SD5001			SD5002			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	BV_{DS} Drain-Source Breakdown Voltage	20	25		10	25		15	25		V	$I_D = 10\text{nA}$ $V_{GS} = V_{BS} = -5\text{V}$	
2	BV_{SD} Source-Drain Breakdown Voltage	20			10			15			V	$I_S = 10\text{nA}$ $V_{GD} = V_{BD} = -5\text{V}$	
3	BV_{DB} Drain-Substrate Breakdown Voltage	25			15			22.5			V	$I_D = 10\text{nA}$, $V_{GB} = 0$ Source Open	
4	BV_{SB} Source-Substrate Breakdown Voltage	25			15			22.5			V	$I_S = 10\mu\text{A}$, $V_{GB} = 0$ Drain Open	
5	$I_{D(off)}$ Drain-Source Off Current						10				nA	$V_{DS} = 10\text{V}$	
6									10		nA	$V_{DS} = 15\text{V}$	
7				10								nA	$V_{DS} = 20\text{V}$
8							10					nA	$V_{SD} = 10\text{V}$
9	$I_{S(off)}$ Source-Drain OFF Current									10	nA	$V_{SD} = 15\text{V}$	
10				10							nA	$V_{SD} = 20\text{V}$	
11							1.0					μA	$V_{GB} = 25\text{V}$
12	I_{GBS} Gate-Body Leakage Current			1.0						1.0	μA	$V_{GB} = 30\text{V}$	
13											V	$V_{DS} = V_{GS}$, $I_D = 1\mu\text{A}$ $V_{SB} = 0$	
14	$V_{GS(th)}$ Gate Threshold Voltage	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1\mu\text{A}$ $V_{SB} = 0$	
15	$r_{DS(on)}$ Drain-Source ON Resistance		50	70		50	70		50	70	ohms	$V_{GS} = 5\text{V}$	
16			30			30			30			$V_{GS} = 10\text{V}$	
17			23			23			23			$V_{GS} = 15\text{V}$	
18			19			19			19			$V_{GS} = 20\text{V}$	
18	r_{DSM} ON Resistance Match		1.0	5.0		1.0	5.0		1.0	5.0		$V_{GS} = 5\text{V}$	
19	g_{fs} Common-Source Forward Transcond.	10	12		10	12		10	12		mmhos	$V_{DS} = 10\text{V}$, $I_D = 20\text{mA}$ $f = 1\text{KHz}$, $V_{SB} = 0$	
20	$C_{(gs + gd + gb)}$ Gate Node Capacitance		2.4	3.5		2.4	3.5		2.4	3.5	pF	$V_{DS} = 10\text{V}$ $V_{GS} = V_{BS} = -15\text{V}$ $f = 1\text{MHz}$	
21	$C_{(gs + db)}$ Drain Node Capacitance		1.3	1.5		1.3	1.5		1.3	1.5			
22	$C_{(gs + sb)}$ Source Node Capacitance		3.5	4.0		3.5	4.0		3.5	4.0			
23	$C_{(dg)}$ Reverse Transfer Capacitance		0.3	0.5		0.3	0.5		0.3	0.5			
24	C_T Cross Talk		-107			-107			-107				
25	$t_{d(on)}$ Turn ON Delay Time		0.7	1.0		0.7	1.0		0.7	1.0	nSec	$V_{DD} = 5\text{V}$, $V_{G(on)} = 10\text{V}$ $R_L = 680\Omega$, $R_G = 51\Omega$	
26	t_r Rise Time		0.8	1.0		0.8	1.0		0.8	1.0			
27	t_{off} Turn OFF Time		10			10			10				