NIPPON PRECISION CIRCUITS INC.

SM8613AV

Laser Switching Driver IC

OVERVIEW

The SM8613AV is a portable CD player laser diode (LD) driver IC. Conventional portable CD players use a fixed-current LD drive method, but this increases the power dissipation and limits battery life. The SM8613AV employs an intermittent LD driver duty operation to reduce the laser power dissipation, which greatly reduces the current consumption when reading data and extends battery driver life.

FEATURES

- 2.3V low-voltage supply operation
- Intermittent-duty laser driver built-in (4-times speed read, 38MHz max. intermittent output)
- Laser switching frequency range: 8.6 to 38MHz
- Fixed-current drive/intermittent-duty drive switch function
- Intermittent current duty ratio adjust function
- Automatic power control (APC) function using luminosity-monitoring photodiode (PD)
- Low power dissipation
- Package: 16-pin VSOP (lead-free)

APPLICATIONS

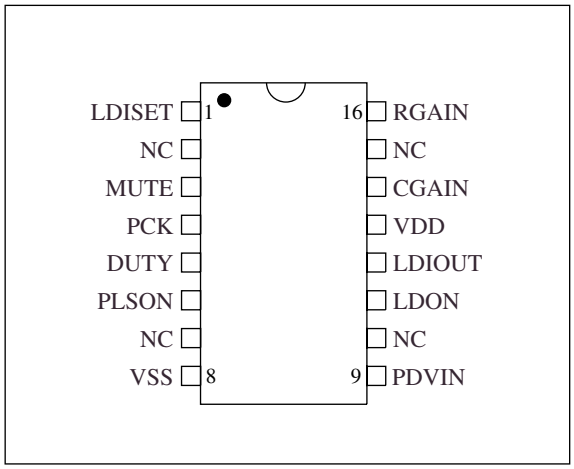
- Portable CD player

ORDERING INFORMATION

Device	Package
SM8613AV	16-pin VSOP

PINOUT

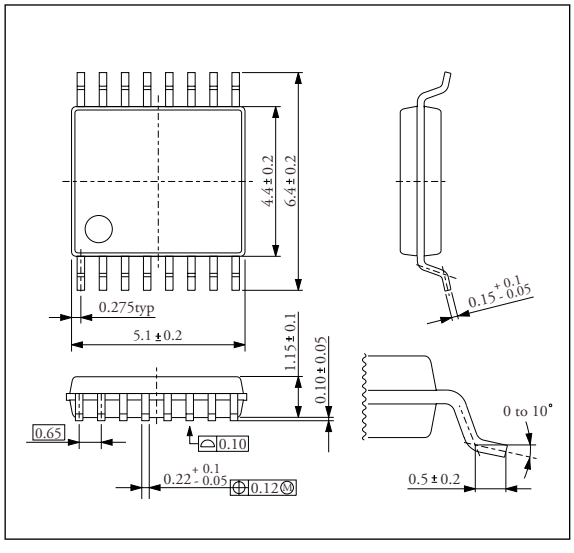
(Top view)



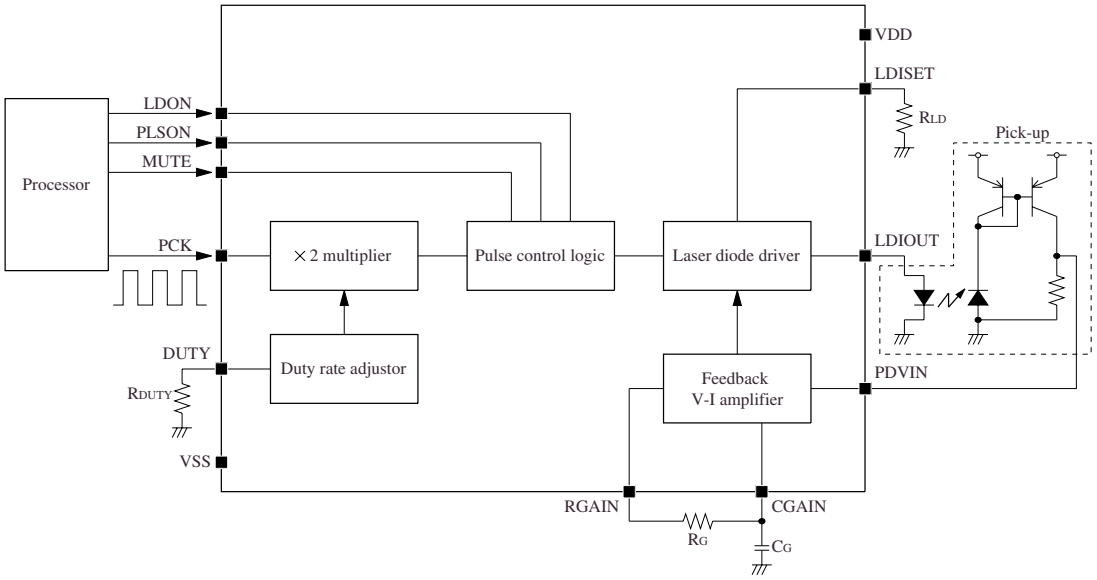
PACKAGE DIMENSIONS

(Unit: mm)

Weight: 0.07g



BLOCK DIAGRAM



PIN DESCRIPTION

<table>
<tr><th>Number</th><th>Name</th><th>i/o</th><th>Description</th></tr>
<tr><td>1</td><td>LDISET</td><td>o</td><td>LD drive maximum current setting resistor connection</td></tr>
<tr><td>2</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>3</td><td>MUTE</td><td>ip</td><td>Intermittent-drive stop signal
<table>
<tr><th>MUTE</th><th>Laser drive state</th></tr>
<tr><td>L</td><td>LD intermittent drive control (PLSON = H)</td></tr>
<tr><td>H</td><td>LD constant-current drive</td></tr>
</table></td></tr>
<tr><td>4</td><td>PCK</td><td>i</td><td>Intermittent control reference pulse input</td></tr>
<tr><td>5</td><td>DUTY</td><td>o</td><td>Intermittent-duty ratio adjust resistor connection</td></tr>
<tr><td>6</td><td>PLSON</td><td>ip</td><td>Intermittent-drive control signal
<table>
<tr><th>PLSON</th><th>Laser drive state</th></tr>
<tr><td>L</td><td>LD constant-current drive</td></tr>
<tr><td>H</td><td>LD intermittent drive control</td></tr>
</table></td></tr>
<tr><td>7</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>8</td><td>VSS</td><td>–</td><td>Ground (0V DC)</td></tr>
<tr><td>9</td><td>PDVIN</td><td>i</td><td>Laser luminosity monitor voltage input</td></tr>
<tr><td>10</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>11</td><td>LDON</td><td>ip</td><td>LD drive current control signal
<table>
<tr><th>LDON</th><th>Laser drive state</th></tr>
<tr><td>L</td><td>LD drive stop control (sleep mode)</td></tr>
<tr><td>H</td><td>LD drive ON</td></tr>
</table></td></tr>
<tr><td>12</td><td>LDIOUT</td><td>o</td><td>LD drive current output</td></tr>
<tr><td>13</td><td>VDD</td><td>–</td><td>Supply voltage (2.5V DC)</td></tr>
<tr><td>14</td><td>CGAIN</td><td>o</td><td>APC frequency response control capacitor connection</td></tr>
<tr><td>15</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>16</td><td>RGAIN</td><td>o</td><td>APC loop gain control resistor connection</td></tr>
</table>

ip: Built-in pull-down resistor

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	– 0.5 to 7.0	V
Input voltage	V_{IN}	– 0.5 to V_{DD} + 0.5	V
Input current	I_{IN}	– 3.0 to + 3.0	mA
Operating temperature	T_{OPR}	– 20 to 70	°C
Storage temperature	T_{STG}	– 40 to 125	°C
Power dissipation	P_W	96	mW

DC Electrical Characteristics

V_{DD} = 2.5V, Ta = + 25 °C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Guaranteed operating supply voltage	V_{DD}		2.3	2.5	3.3	V	I
Current consumption	I_{DD1}	PDVIN–LDIOUT short, R_{LDIOUT} = 4Ω, LDON = HIGH, Excluding LDIOUT current	1.0	1.7	2.3	mA	I
	I_{DD2}	LDON = LOW	–	–	30	µA	I

Input Specifications

V_{DD} = 2.5V, Ta = + 25 °C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
PCK HIGH-level voltage	V_{IHPCK}		$V_{DD} \times 0.7$	–	–	V	I
PCK LOW-level voltage	V_{ILPCK}		–	–	$V_{DD} \times 0.3$	V	I
PCK HIGH-level sink current	I_{HPCK}		–	–	20	µA	I
LDON HIGH-level voltage	V_{IHLDON}		$V_{DD} \times 0.7$	–	–	V	I
LDON LOW-level voltage	V_{ILLDON}		–	–	$V_{DD} \times 0.3$	V	I
LDON HIGH-level sink current	I_{HLDON}		–	–	20	µA	I
PLSON HIGH-level voltage	$V_{IHPLSON}$		$V_{DD} \times 0.7$	–	–	V	I
PLSON LOW-level voltage	$V_{ILPLSON}$		–	–	$V_{DD} \times 0.3$	V	I
PLSON HIGH-level sink current	I_{HPLSON}		–	–	20	µA	I
MUTE HIGH-level voltage	V_{IHMUTE}		$V_{DD} \times 0.7$	–	–	V	I
MUTE LOW-level voltage	V_{ILMUTE}		–	–	$V_{DD} \times 0.3$	V	I
MUTE HIGH-level sink current	I_{HMUTE}		–	–	20	µA	I

Electrical Characteristics

V_{DD} = 2.5V, Ta = + 25 °C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
PCK minimum input frequency	f_{PCKMIN}		–	–	4.3	MHz	I
PCK maximum input frequency	f_{PCKMAX}		19	–	–	MHz	I
Intermittent current output frequency range	f_{LD}		8.6	–	38	MHz	I
LDON response time	t_{LDON}	LDON = LOW to HIGH, I(LDIOUT) to 90%, C_G = 6800pF	–	–	110	µs	II
PLSON, MUTE response time 1	t_{PLSON1}	PLSON = LOW to HIGH (MUTE: LOW), MUTE = HIGH to LOW (PLSON: HIGH), until the duty ratio stabilizes	–	–	20	µs	II
PLSON, MUTE response time 2	t_{PLSON2}	PLSON = HIGH to LOW (MUTE: LOW), MUTE = LOW to HIGH (PLSON: HIGH)	–	–	25	ns	II
LDIOUT maximum output current	I_{LDMAX}	PDVIN = 0V	40	–	–	mA	I
LDIOUT intermittent current rise time	t_{LDIR}		–	–	10	ns	II
LDIOUT intermittent current fall time	t_{LDIF}		–	–	10	ns	II
LDISET voltage	V_{LDISET}	$1/3V_{DD}$	0.75	0.83	0.92	V	I
PDVIN convergence voltage	V_{PDVIN}	R_G = 33kΩ, V_{DD} = 2.5V, PDVIN–LDIOUT short, R_{LDIOUT} = 20Ω	145	160	175	mV	I
PDVIN input impedance	Z_{PDVIN}		1	–	–	MΩ	II
APC loop cutoff frequency	f_{APC}	C_G = 6800pF	–	25	100	kHz	I
Minimum duty ratio	DR_{MIN}	PCK = 4.3MHz, R_{DUTY} = 15kΩ	20	–	40	%	I
Maximum duty ratio	DR_{MAX}	PCK = 4.3MHz, R_{DUTY} = 5kΩ	55	–	85	%	I
Minimum LD current ON time	t_{LDION}		–	14	–	ns	II

Note 1) LDON has internal pull-down resistor.
Note 2) PLSON has internal pull-down resistor.
Note 3) MUTE has internal pull-down resistor.
Note 4) LDISET is in high-impedance state when LDON is HIGH.
Note 5) DUTY is in high-impedance state when LDON is HIGH.

Test level description

Test level I	100% of devices tested at + 25°C
Test level II	Specifications guaranteed according to design and evaluation tests.

FUNCTIONAL DESCRIPTION

LD Driver Control

The LD is controlled by the 3 logic-level signals on LDON, PLSON, and MUTE. When LDON is HIGH, the LD is in drive mode and the drive current is output on LDIOUT. When LDON is LOW (sleep mode), the LD drive mode stops (LDIOUT output current = 0mA).

Also when LDON is HIGH, LD intermittent drive mode operation occurs when PLSON is HIGH and MUTE is LOW.

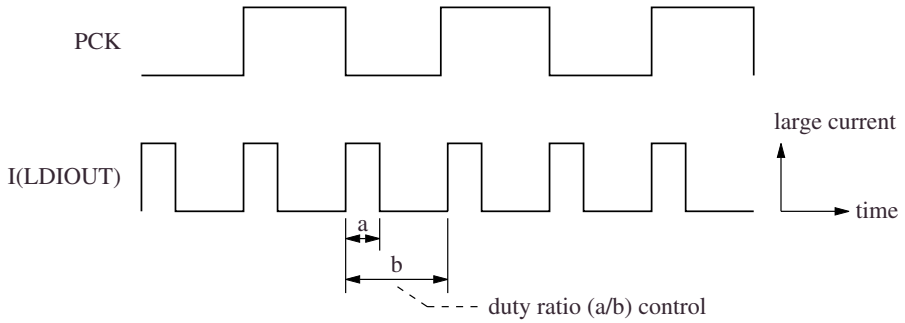
Table 1. Control signals and laser drive states

LDON	PLSON	MUTE	Laser drive state
H	L	L	LDIOUT constant-current output
H	L	H	LDIOUT constant-current output
H	H	L	LDIOUT intermittent current output
H	H	H	LDIOUT constant-current output
L	×	×	LDIOUT = 0mA (sleep mode)

Note) × : Don't care.

Frequency Multiplier Function and LD Drive Current Duty Ratio Setting

The SM8613AV multiplies the PCK input frequency by 2, which is then used as the intermittent-drive reference frequency. The intermittent drive LD current ON time is shown in the following figure.



The intermittent current output from LDIOUT is automatically adjusted as the frequency changes to maintain the duty ratio almost constant. The intermittent current duty ratio is set by resistor R_{DUTY} connected between DUTY and VSS pins, and is given by the following equation.

$$dutyratio = \left(1 - \frac{\frac{3}{2}V(DUTY)}{\frac{1}{2}VDD}\right) \times 100 = \frac{44[\mathrm{k}\Omega] - 2 \times R_{DUTY}}{R_{DUTY} + 44[\mathrm{k}\Omega]} \times 100\ [\%]$$

$$V(DUTY) = \frac{R_{DUTY}}{R_{DUTY} + 44[\mathrm{k}\Omega]} \times VDD\ [\mathrm{V}]$$

R_{DUTY} : resistor connected to DUTY pin [kΩ]

Laser Diode Drive Current Mid-value Set Function

The laser diode drive current mid-value can be adjusted by changing the resistance R_{LD} connected between the LDISET and VSS pins. The laser diode drive current mid-value reference value I_{LD0}, given by the following equation, is set to the LDIOUT output current when the PDVIN voltage is in balance state (147 to 193mV). Note that the actual LDIOUT current may change due to feedback gain, and laser diode/photo diode tolerance variations.

If R_G is not connected, the output current has no relationship to the reference current value, but is determined by the PDVIN convergence voltage.

$$I_{LD0} = I_{LDSET} \times 120 = \frac{40VDD}{R_{LD}} \text{ [A]}$$

R_{LD} : LDISET connected resistor [Ω]

APC Loop Gain Setting

The APC loop gain can be adjusted using an external resistor R_G. The gain set resistor, R_G, is connected between RGAIN and CGAIN. The PDVIN voltage to laser drive current open-loop gain is given approximately by the following equation.

$$Gm_{PDVIN} = 1.15 \times 10^{-4} R_G \text{ [S]}$$

ΔLDIOUT current /ΔPDVIN voltage ratio [S]
R_G : RGAIN–CGAIN resistor [Ω]

If the external resistor R_G is removed, the maximum gain Gm = 26 [S] is selected.

APC Loop Cutoff Frequency Setting

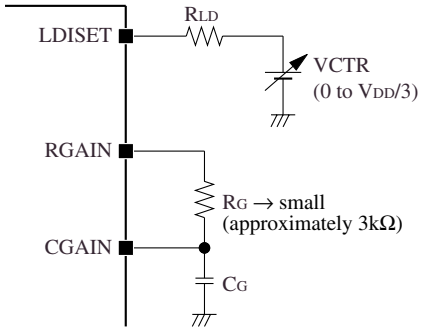
The APC loop cutoff frequency f_{APC} is determined by the capacitor C_G connected between CGAIN and VSS pins. The same result occurs if C_G is connected between RGAIN and CGAIN pins.

$$f_{APC} = \frac{1}{2\pi 950 C_G} \text{ [Hz]}$$

Laser APC Convergence Current External Signal Adjustment

The LD convergence current is determined by the internal bias voltage. However, if the APC loop gain resistor R_G is small, the convergence current can be adjusted externally.

The convergence current is adjusted by the LDISET current, shown in the figure below. With VCTR in the range 0 to $1/3V_{DD}$, the LDISET current decreases with increasing VCTR, and the laser convergence current center point also decreases in response.



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