- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (– 32-mA I_{OH}, 64-mA I_{OL})**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54ABT16245 . . . WD PACKAGE
SN74ABT16245 . . . DGG OR DL PACKAGE
(TOP VIEW)

1DIR	1	48	1$\overline{OE}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V_{CC}	7	42	V_{CC}
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V_{CC}	18	31	V_{CC}
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	2$\overline{OE}$
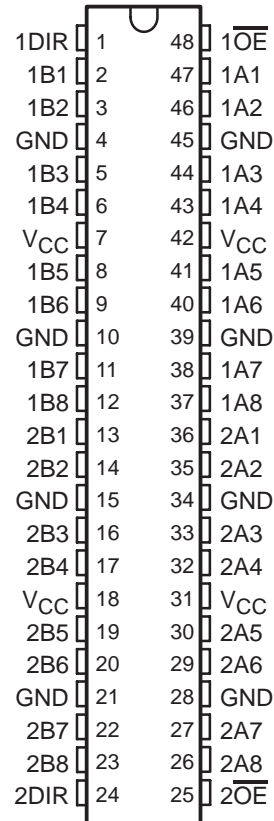
description

The ′ABT16245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16245 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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logic symbol†

logic diagram (positive logic)

To Seven Other Channels

To Seven Other Channels
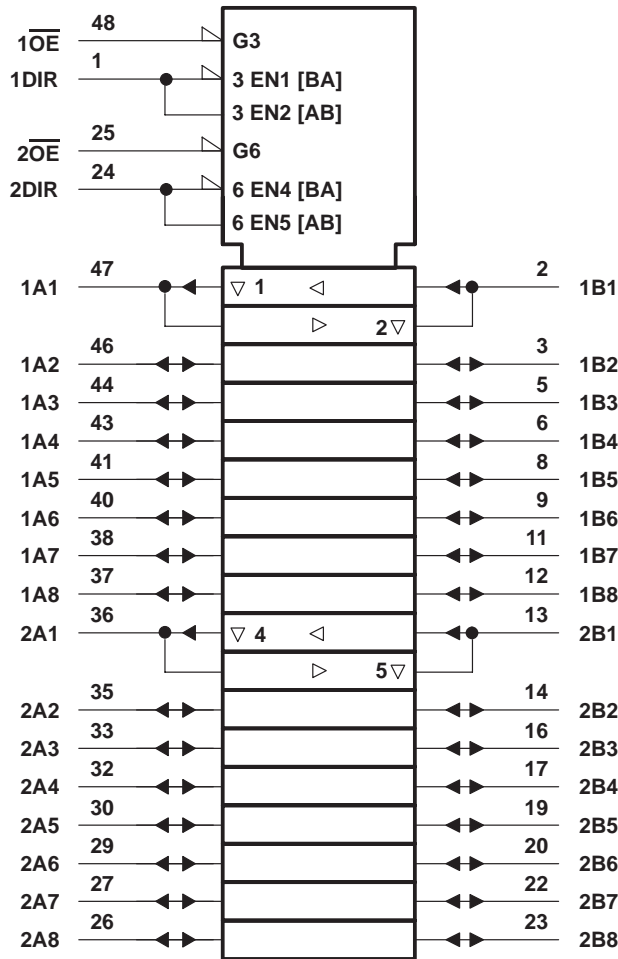
† This symbol is in accordance with ANSI/IEEE Std 91-1984
and IEC Publication 617-12.
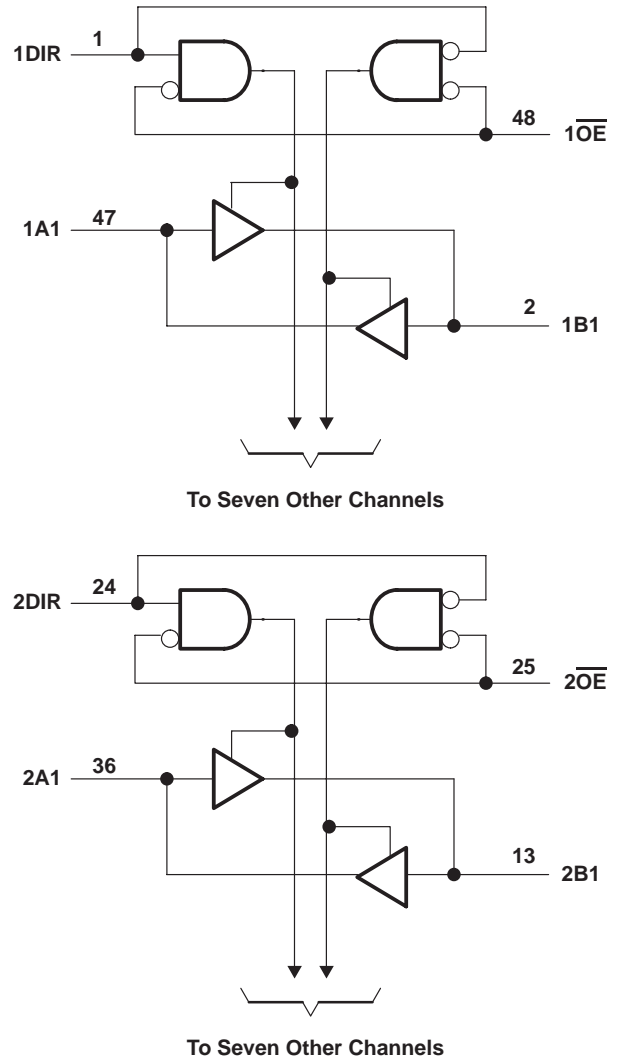
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16245 . . . . 96 mA
SN74ABT16245 . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . −18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package . . . . 0.8 W
DL package . . . . 0.85 W
Storage temperature range . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1:   The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT16245 MIN	SN54ABT16245 MAX	SN74ABT16245 MIN	SN74ABT16245 MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C MIN	T_A = 25°C TYP[†]	T_A = 25°C MAX	SN54ABT16245 MIN	SN54ABT16245 MAX	SN74ABT16245 MIN	SN74ABT16245 MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = − 3 mA	2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = − 3 mA	3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = − 24 mA	2			2				
	V_{CC} = 4.5 V,	I_{OH} = − 32 mA	2[‡]					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55		0.55			V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA			0.55[‡]				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND	Control inputs			±1		±1		±1	μA
		A or B ports			±100		±100		±100	
I_{OZH}[§]	V_{CC} = 5.5 V,	V_O = 2.7 V			10[¶]		10		10[¶]	μA
I_{OZL}[§]	V_{CC} = 5.5 V,	V_O = 0.5 V			−10[¶]		−10		−10[¶]	μA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V			±100				±100	μA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high		50		50		50	μA
I_O[#]	V_{CC} = 5.5 V,	V_O = 2.5 V	−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		2		2		2	mA
			Outputs low		32		32		32	
			Outputs disabled		2		2		2	
ΔI_{CC}[‖]	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled		1		1.5		1	mA
			Outputs disabled		0.05		1		0.05	
		Control inputs			1.5		1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V	Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V	A or B ports		8.5						pF

[†] All typical values are at V_{CC} = 5 V.
[‡] On products compliant to MIL-STD-883, Class B, this parameter does not apply.
[§] The parameters I_{OZH} and I_{OZL} include the input leakage current.
[¶] This data sheet limit may vary among suppliers.
[#] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
[‖] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16245		SN74ABT16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2.2	3.4	0.5	4	1	3.9	ns
t_{PHL}			1	2.1	3.8	0.5	4.6	1	4.5	
t_{PZH}	$\overline{OE}$	B or A	1	3.1	4.4	0.8	5.5	1	5.4	ns
t_{PZL}			1	3	6.1	0.9	7.3	1	7.2	
t_{PHZ}	$\overline{OE}$	B or A	1.3	3.5	4.7	1.3	6.3	1.3	5.5	ns
t_{PLZ}			1.4	3.2	4.7	1.4	5.3	1.4	5.2	

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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open
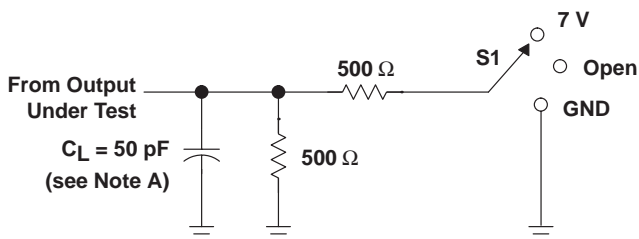
LOAD CIRCUIT FOR OUTPUTS
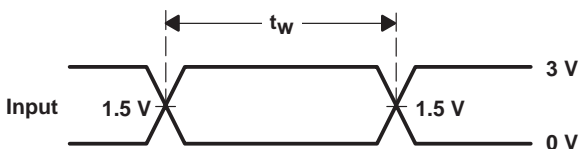
VOLTAGE WAVEFORMS
PULSE DURATION
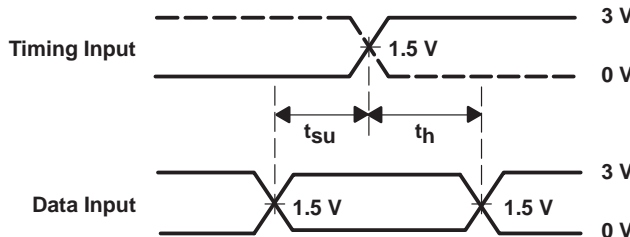
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
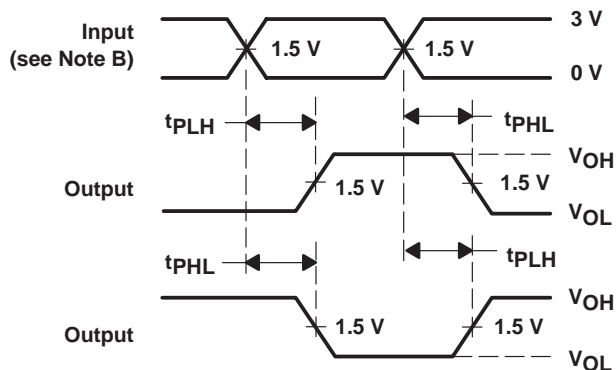
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
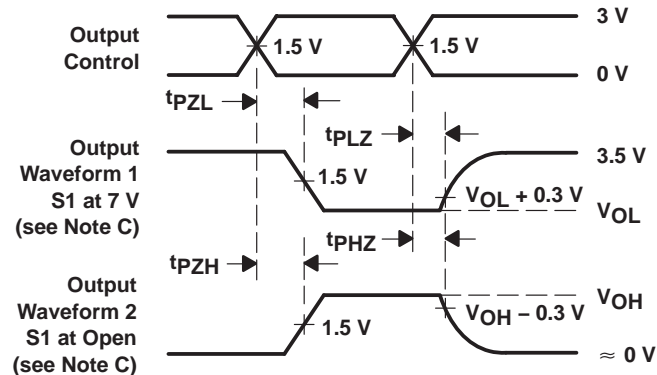
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
   B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \, \Omega$, $t_r ≤ 2.5$ ns, $t_f ≤ 2.5$ ns.
   C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74ABT16245DGGR	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI
SN74ABT16245DL	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI
SN74ABT16245DLR	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DL (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

0.025 (0,635)

0.0135 (0,343)
0.008 (0,203)

⊕ 0.005 (0,13) Ⓜ

48   25

0.010 (0,25)
0.005 (0,13)

0.299 (7,59)
0.291 (7,39)

0.420 (10,67)
0.395 (10,03)

Gage Plane

0.010 (0,25)

1   24

0°–8°

A

0.040 (1,02)
0.020 (0,51)

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

PINS ** DIM	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / E 12/01
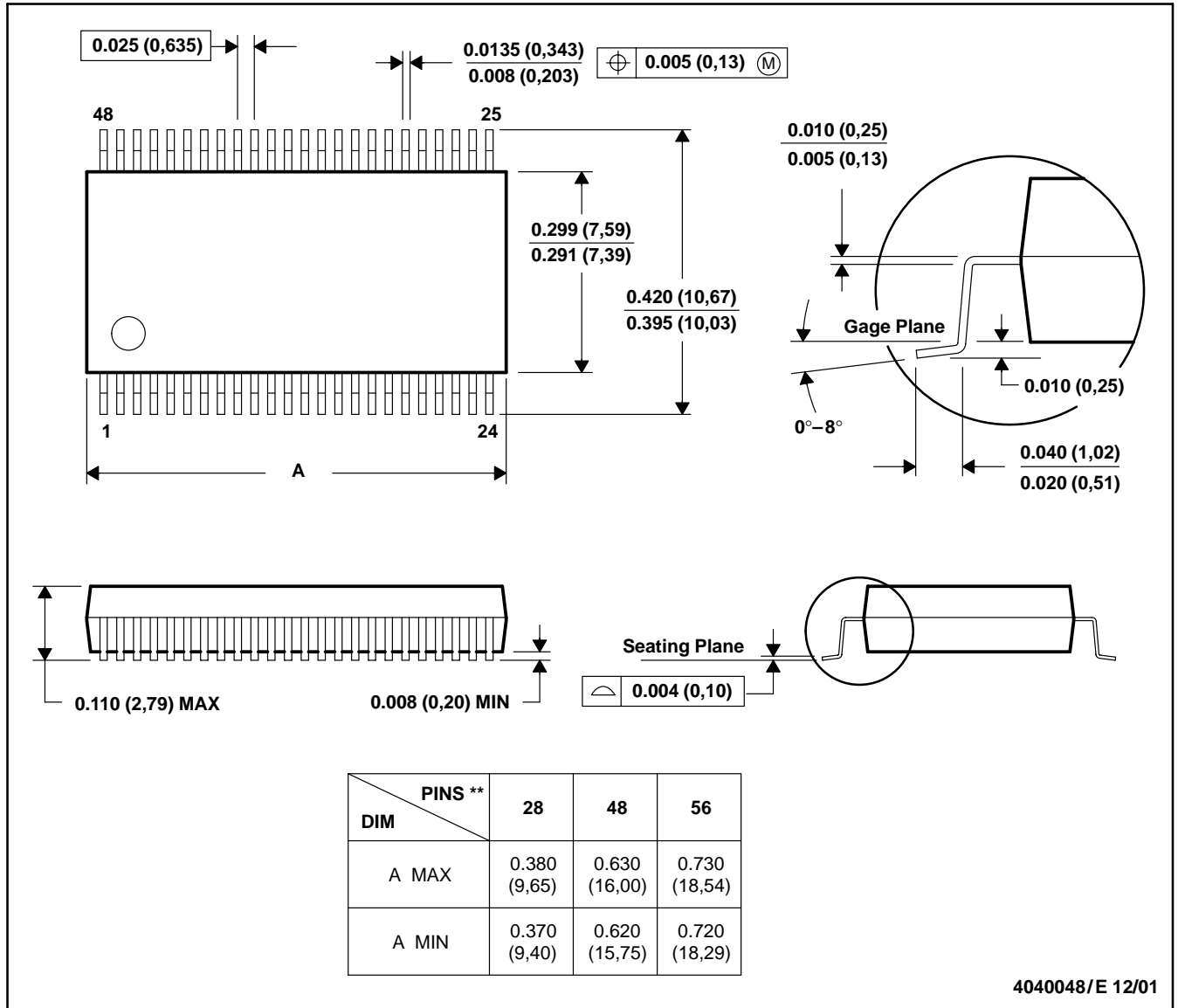
NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MO-118

DGG (R-PDSO-G)**　　　　　　　　　　　　　**PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
　　　　B. This drawing is subject to change without notice.
　　　　C. Body dimensions do not include mold protrusion not to exceed 0,15.
　　　　D. Falls within JEDEC MO-153

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