

# SN54ABT16470, SN74ABT16470 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS085E – FEBRUARY 1991 – REVISED MAY 1997

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

## description

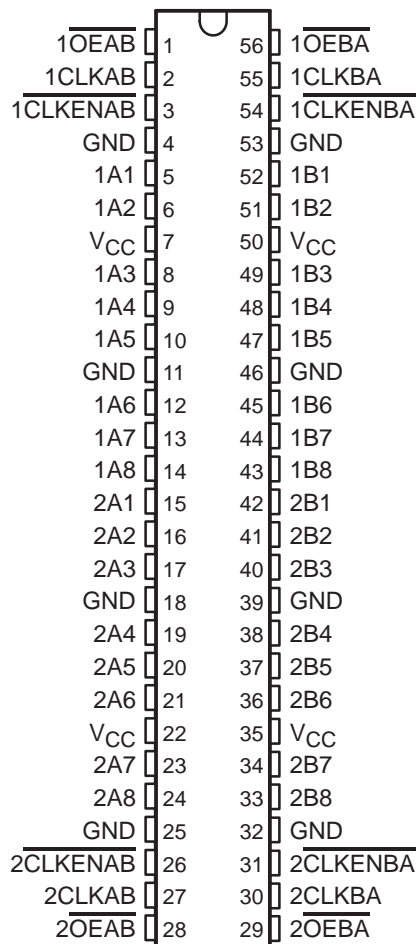
The 'ABT16470 are 16-bit registered transceivers that contain two sets of D-type flip-flops for temporary storage of data flowing in either direction. The 'ABT16470 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate clock (CLKAB or CLKBA) and output-enable ( $\overline{OEAB}$  or  $\overline{OEBA}$ ) inputs are provided for each register to permit independent control in either direction of data flow.

To avoid false clocking of the flip-flops, clock enable ( $\overline{CLKEN}$ ) should not be switched from high to low while CLK is high.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16470 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT16470 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT16470 . . . WD PACKAGE  
SN74ABT16470 . . . DGG OR DL PACKAGE  
(TOP VIEW)



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 **TEXAS  
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**16-BIT REGISTERED TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

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**FUNCTION TABLE†**

INPUTS				OUTPUT B
$\overline{\text{CLKENAB}}$	CLKAB	$\overline{\text{OEAB}}$	A	
H	X	X	X	Z
X	X	H	X	Z
L	L	L	X	$B_0^\ddagger$
L	↑	L	L	L
L	↑	L	H	H

† A-to-B data flow is shown; B-to-A flow is similar but uses  $\overline{\text{CLKENBA}}$ , CLKBA, and OEBA.

‡ Output level before the indicated steady-state input conditions were established

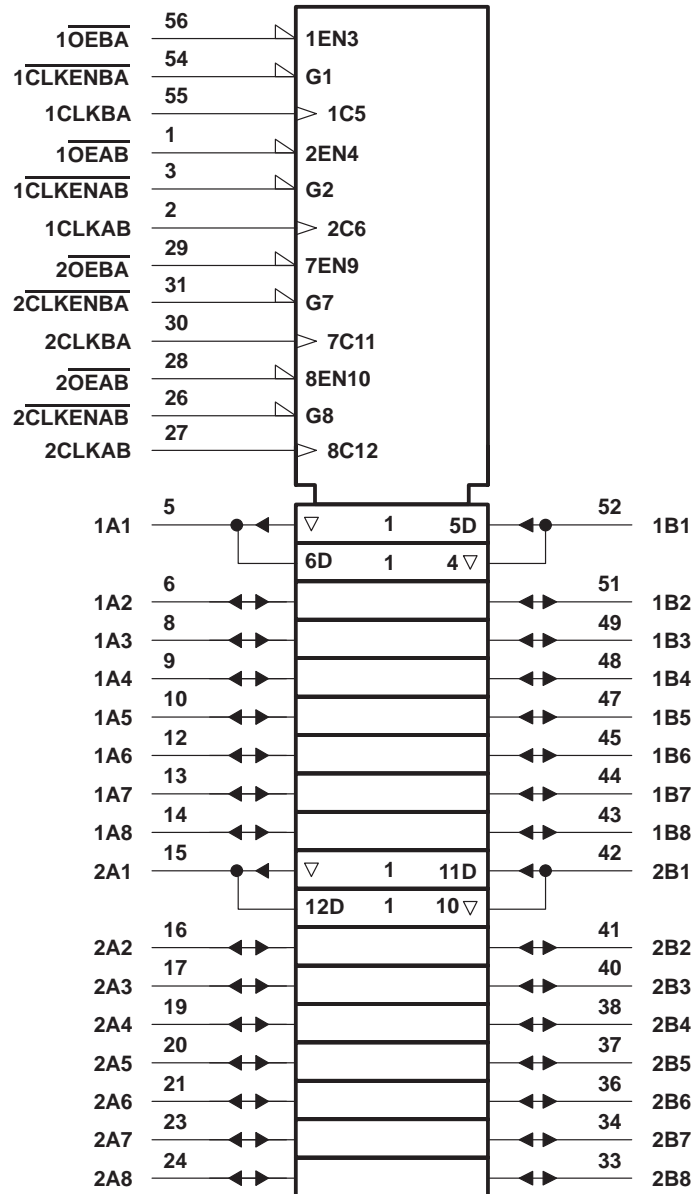


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logic symbol†

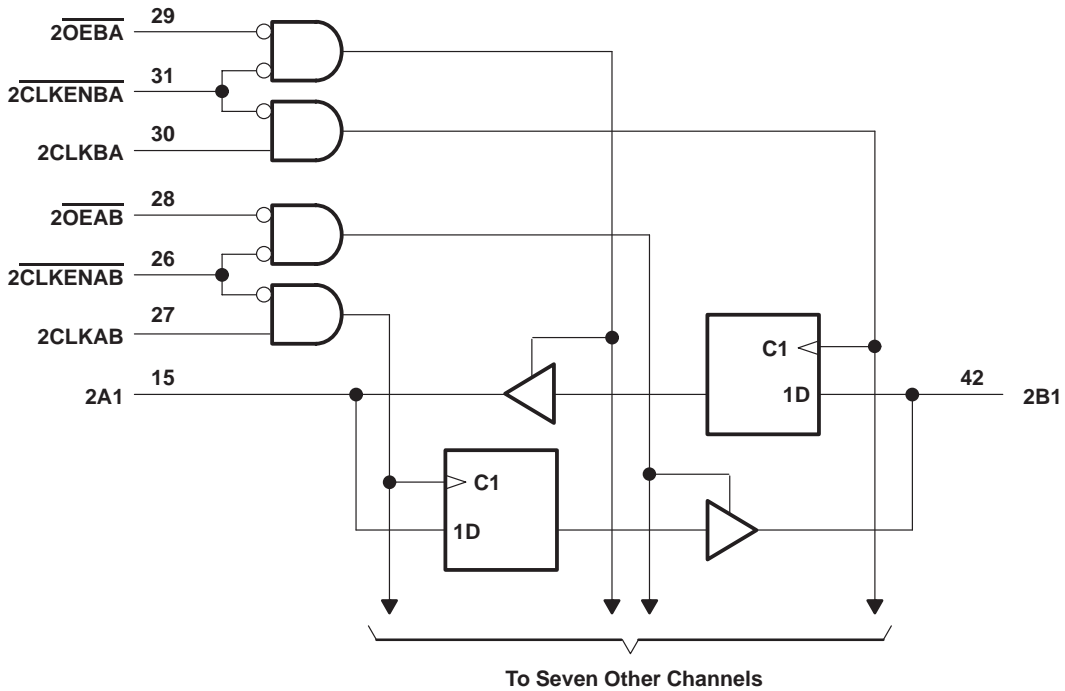
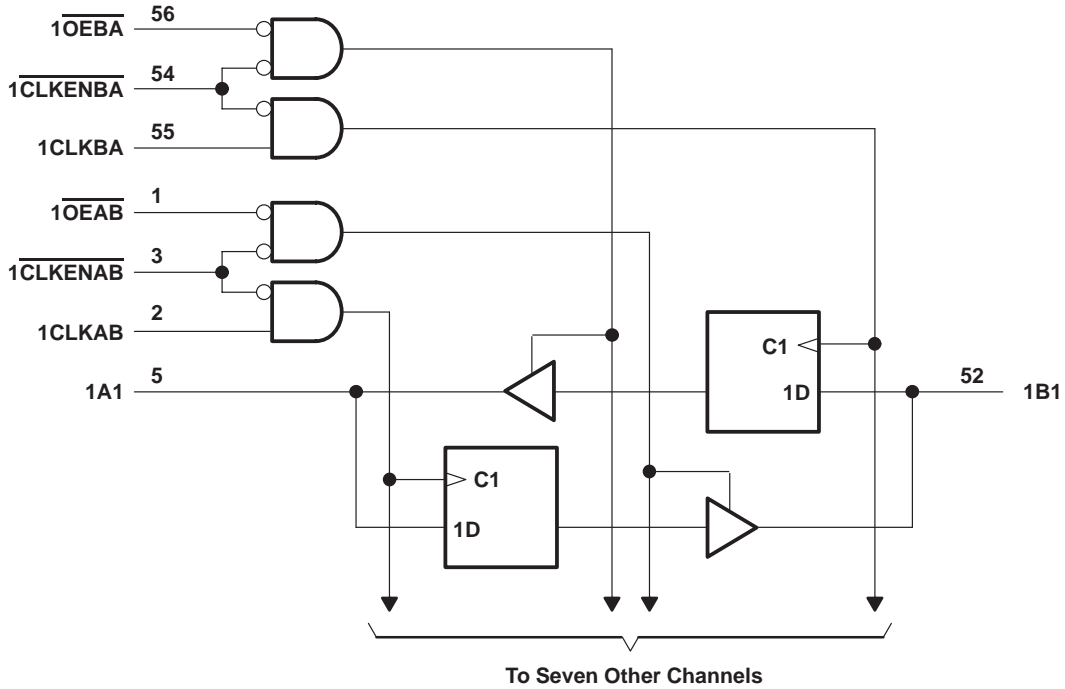


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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## logic diagram (positive logic)



# SN54ABT16470, SN74ABT16470 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT16470	96 mA
SN74ABT16470	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

## recommended operating conditions (see Note 3)

		SN54ABT16470		SN74ABT16470		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT16470		SN74ABT16470		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA			2.5		2.5		2.5	V	
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA			3		3		3		
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -24 mA		2		2				
		I <sub>OH</sub> = -32 mA		2*				2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA				0.55		0.55	V	
		I <sub>OL</sub> = 64 mA				0.55*		0.55		
V <sub>hys</sub>				100					mV	
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1		±1		±1	μA
	A or B ports				±100		±100		±100	
I <sub>OZH</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V			50		50		50	μA	
I <sub>OZL</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V			-50		-50		-50	μA	
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	μA	
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high				50		50	μA	
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V			-50	-100	-200		-50	-200	mA
I <sub>CC</sub>	A or B ports	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high			2		2	2	mA
			Outputs low			35		35	35	
			Outputs disabled			2		2	2	
ΔI <sub>CC</sub> ¶	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND					0.5		0.5	mA	
C <sub>I</sub>	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V				3			pF	
C <sub>IO</sub>	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V				8.5			pF	

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT16470		SN74ABT16470		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	150	0	150	0	150	MHz
t <sub>w</sub> #	Pulse duration, CLKAB or CLKBA high or low	3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before CLKAB↑ or CLKBA↑	4		4		4		ns
t <sub>h</sub>	Hold time, data after CLKAB↑ or CLKBA↑	1		1		1		ns

# This parameter is characterized, but not production tested.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABT16470		SN74ABT16470		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			150			150		150		MHz
$t_{PLH}$	CLK	A or B	1.4	3.1	4.8	1.4	5.1	1.4	4.9	ns
$t_{PHL}$			1.3	3.2	4.6	1.3	5.1	1.3	4.9	
$t_{PZH}$	$\overline{OE}$	A or B	1	3.1	4.3	1	5	1	4.9	ns
$t_{PZL}$			1.2	3.6	5.8	1.2	6.9	1.2	6.8	
$t_{PHZ}$	$\overline{OE}$	A or B	1.9	3.7	4.9	1.9	6	1.9	5.5	ns
$t_{PLZ}$			1.6	3.3	4.8	1.6	5.4	1.6	5.3	
$t_{PZH}$	$\overline{CLKEN}$	A or B	1	3.4	4.6	1	5.8	1	5.7	ns
$t_{PZL}$			1.2	3.9	6	1.2	7.3	1.2	7.2	
$t_{PHZ}$	$\overline{CLKEN}$	A or B	1.7	3.9	5.2	1.7	6.2	1.7	5.8	ns
$t_{PLZ}$			1.5	3.6	5.3	1.5	5.5	1.5	5.4	

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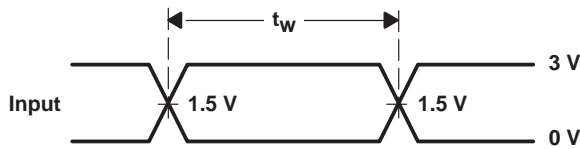
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**PARAMETER MEASUREMENT INFORMATION**

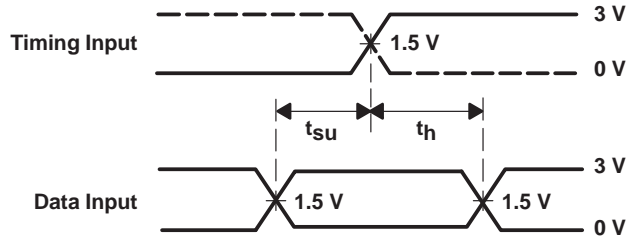


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open

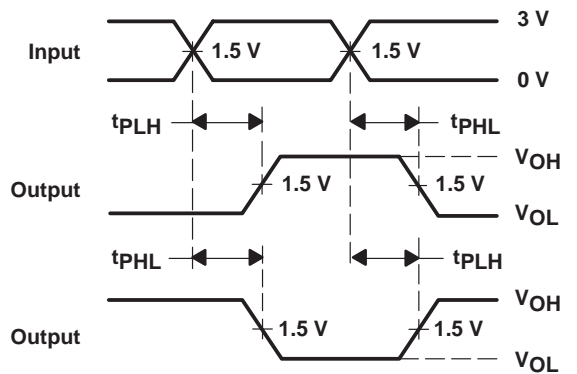
**LOAD CIRCUIT**



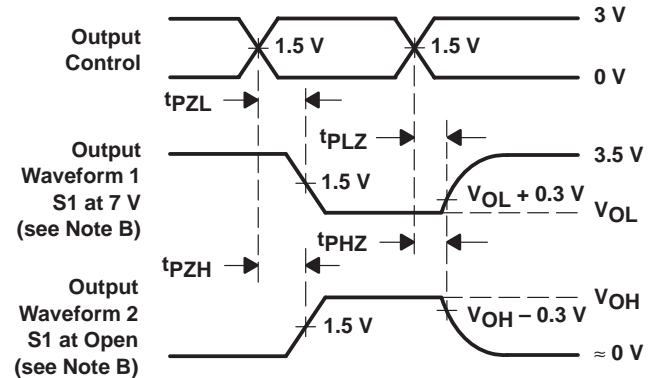
**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**  
**INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**  
**LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**



**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16470DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ABT16470DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16470DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74ABT16470DLR	SSOP	DL	56	1000	346.0	346.0	49.0

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