'LS673

- **16-Bit Serial-In, Serial-Out Shift Register with 16-Bit Parallel-Out Storage Register**

- **Performs Serial-to-Parallel Conversion**

'LS674

- **16-Bit Parallel-In, Serial-Out Shift Register**

- **Performs Parallel-to-Serial Conversion**

description

SN54LS673, SN74LS673

The 'LS673 is a 16-bit shift register and a 16-bit storage register in a single 24-pin package. A three-state input/output (SER/Q15) port to the shift register allows serial entry and/or reading of data. The storage register is connected in a parallel data loop with the shift register and may be asynchronously cleared by taking the store-clear input low. The storage register may be parallel loaded with shift-register data to provide shift-register status via the parallel outputs. The shift register can be parallel loaded with the storage-register data upon command.

A high logic level at the chip-level ($\overline{CS}$) input disables both the shift-register clock and the storage register clock and places SER/Q15 in the high-impedance state. The store-clear function is not disabled by the chip select.

Caution must be exercised to prevent false clocking of either the shift register or the storage register via the chip-select input. The shift clock should be low during the low-to-high transition of chip select and the store clock should be low during the high-to-low transition of chip select.
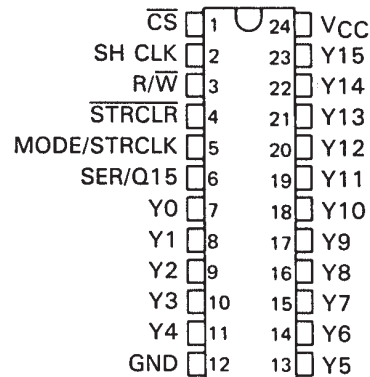
SN54LS674, SN74LS674

The 'LS674 is a 16-bit parallel-in, serial-out shift register. A three-state input/output (SER/Q15) port provides access for entering a serial data or reading the shift-register word in a recirculating loop.
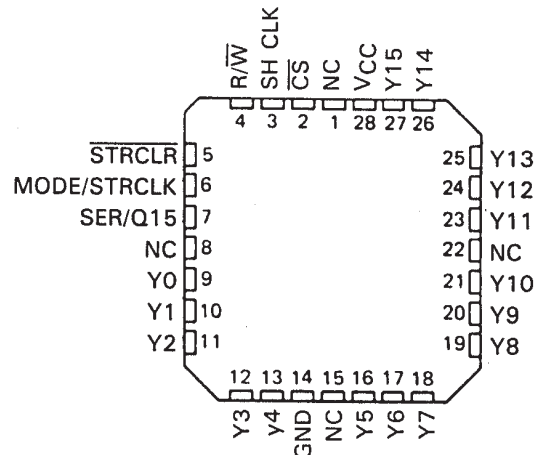
The device has four basic modes of operation:

1) Hold (do nothing)
2) Write (serially via input/output)
3) Read (serially)
4) Load (parallel via data inputs)

Low-to-high-level changes at the chip select input should be made only when the clock input is low to prevent false clocking.

SN54LS673 . . . J OR W PACKAGE
SN74LS673 . . . DW OR N PACKAGE
(TOP VIEW)

$\overline{CS}$	1	24	V$_{CC}$
SH CLK	2	23	Y15
R/$\overline{W}$	3	22	Y14
$\overline{STRCLR}$	4	21	Y13
MODE/STRCLK	5	20	Y12
SER/Q15	6	19	Y11
Y0	7	18	Y10
Y1	8	17	Y9
Y2	9	16	Y8
Y3	10	15	Y7
Y4	11	14	Y6
GND	12	13	Y5

SN54LS673 . . . FK PACKAGE
(TOP VIEW)

Top pins: R/$\overline{W}$ (4), SH CLK (3), $\overline{CS}$ (2), NC (1), VCC (28), Y15 (27), Y14 (26)

$\overline{STRCLR}$	5	25	Y13
MODE/STRCLK	6	24	Y12
SER/Q15	7	23	Y11
NC	8	22	NC
Y0	9	21	Y10
Y1	10	20	Y9
Y2	11	19	Y8

Bottom pins: Y3 (12), Y4 (13), GND (14), NC (15), Y5 (16), Y6 (17), Y7 (18)

NC—No internal connection

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SN54LS674 . . . J OR W PACKAGE
SN74LS674 . . . DW OR N PACKAGE
(TOP VIEW)

```
        ___
  CS  [ 1   24 ] VCC
 CLK  [ 2   23 ] P15
 R/W  [ 3   22 ] P14
  NC  [ 4   21 ] P13
 MODE [ 5   20 ] P12
SER/Q15[6   19 ] P11
  P0  [ 7   18 ] P10
  P1  [ 8   17 ] P9
  P2  [ 9   16 ] P8
  P3  [ 10  15 ] P7
  P4  [ 11  14 ] P6
 GND  [ 12  13 ] P5
```
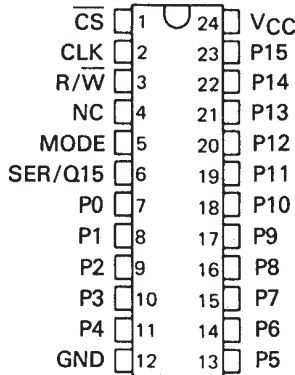
SN54LS674 . . . FK PACKAGE
(TOP VIEW)

```
           R/W  CLK  CS  NC  VCC  P15  P14
            4    3   2   1   28   27   26
  NC  [ 5                            25 ] P13
 MODE [ 6                            24 ] P12
SER/Q15[7                            23 ] P11
  NC  [ 8                            22 ] NC
  P0  [ 9                            21 ] P10
  P1  [ 10                           20 ] P9
  P2  [ 11                           19 ] P8
            12   13  14  15  16  17  18
            P3   P4  GND NC  P5  P6  P7
```
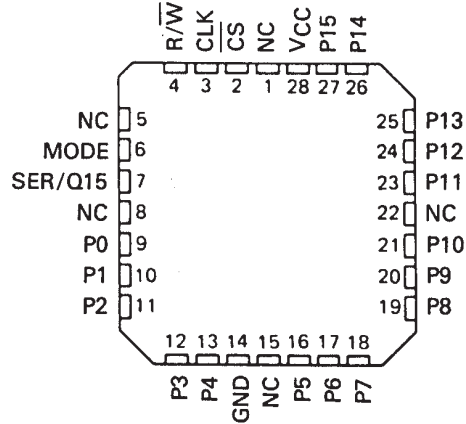
'LS673
FUNCTION TABLE

INPUTS					SER/Q15	SHIFT REGISTER FUNCTIONS				STORAGE REGISTER FUNCTIONS	
$\overline{CS}$	R/$\overline{W}$	SH CLK	$\overline{STRCLR}$	MODE/STRCLK		SHIFT	READ FROM SERIAL OUTPUT	WRITE INTO SERIAL INPUT	PARALLEL LOAD	CLEAR	LOAD
H	X	X	X	X	Z	NO	NO	NO	NO		NO
X	X	X	L	X						YES	
L	L	↓	X	X	Z	YES	NO	YES	NO		
L	H	X	X	X	Q15		YES	NO			NO
L	H	↓	X	L	Q14n	YES	YES	NO	NO		NO
L	H	↓	L	H	L	NO	YES		YES	YES	NO
L	H	↓	H	H	Y15n	NO	YES		YES	NO	NO
L	L	X	H	↑	Z		NO		NO	NO	YES

'LS674 FUNCTION TABLE

INPUTS				SER/Q15	OPERATION
$\overline{CS}$	R/$\overline{W}$	MODE	CLK		
H	X	X	X	Z	Do nothing
L	L	X	↓	Z	Shift and write (serial load)
L	H	L	↓	Q14n	Shift and read
L	H	H	↓	P15	Parallel load

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
X = irrelevant (any input including transitions)
Z = high impedance, input mode
Q14n = content of 14th bit of the shift register before the most recent ↓ transition of the clock.
Q15 = present content of 15th bit of the shift register
Y15n = content of the 15th bit of the storage register before the most recent ↓ transition of the clock.
P15 = level of input P15

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic symbols[†]

'LS673

'LS674

[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, N, and W packages.

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INSTRUMENTS

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3

SN54LS673, SN54LS674, SN74LS673, SN74LS674
16-BIT SHIFT REGISTERS

functional block diagrams

SN54LS673, SN74LS673

SN54LS674, SN74LS674
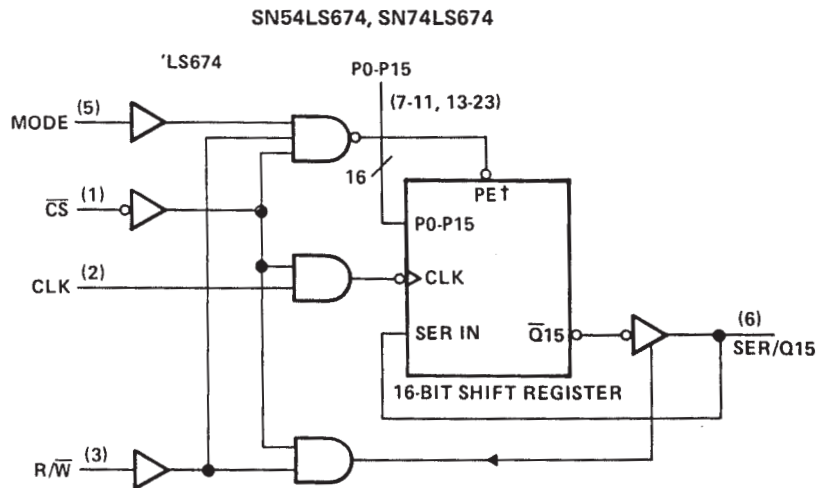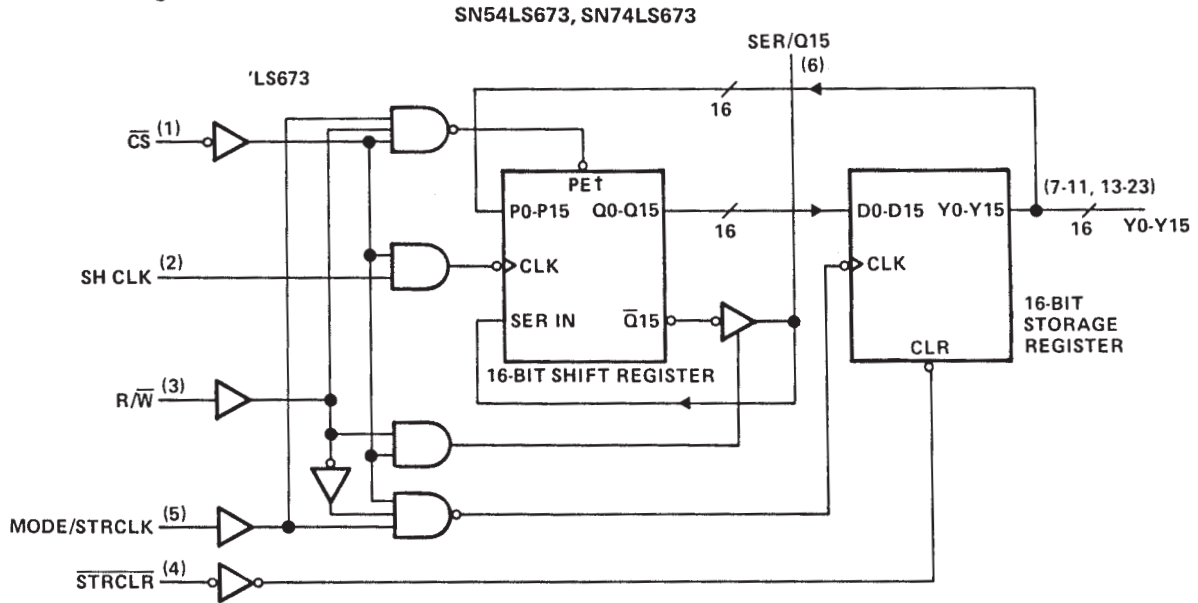
†When PE is active, data is synchronously parallel loaded into the shift registers from the 16 P inputs and no shifting takes place.
Pin numbers shown are for DW, J, N, and W packages.

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schematics of inputs and outputs

| EQUIVALENT OF SER/Q15 AND PARALLEL INPUTS | EQUIVALENT OF OTHER INPUTS | SER/Q15 OUTPUT | TYPICAL OF Y0 THRU Y15 OUTPUTS ('LS673 ONLY) |

SER/Q15: R_{eq} = 20 kΩ NOM
PARALLEL INPUTS: R_{eq} = 30 kΩ NOM
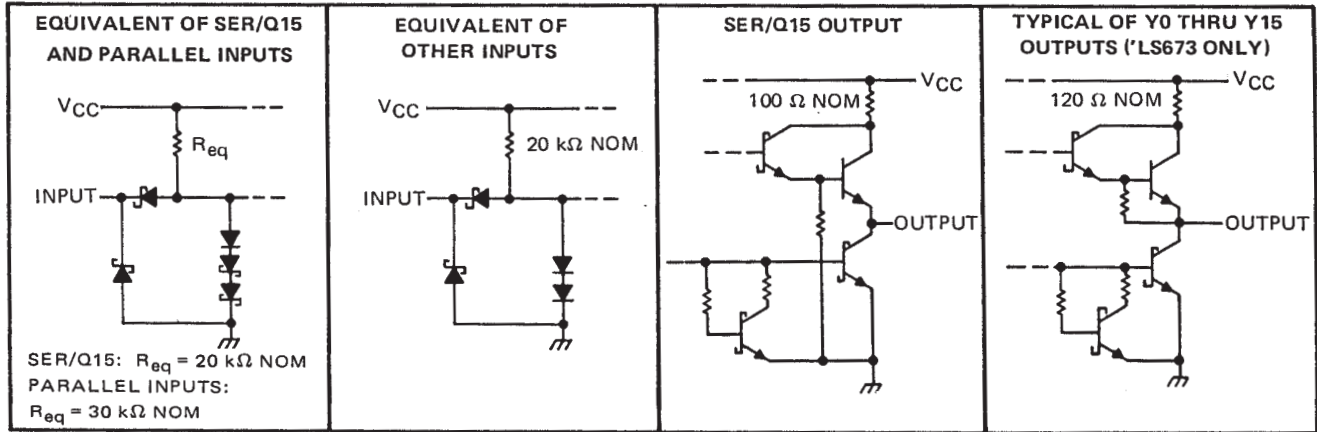
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage: SER/Q15 .... 5.5 V
             All others .... 7 V
Off-state output voltage .... 5.5 V
Operating free-air temperature range: SN54LS673, SN54LS674 .... −55°C to 125°C
                      SN74LS673, SN74LS674 .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

NOTE 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS' MIN	SN54LS' NOM	SN54LS' MAX	SN74LS' MIN	SN74LS' NOM	SN74LS' MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current	SER/Q15			−1			−2.6	mA
		Y0 thru Y15			−0.4			−0.4	
I_{OL}	Low-level output current	SER/Q15			12			24	mA
		Y0 thru Y15			4			8	
f_{clock}	Clock frequency		0		20	0		20	MHz
$t_{w(clock)}$	Width of clock input pulse		20			20			ns
$t_{w(clear)}$	Width of clear input pulse		20			20			ns
t_{su}	Setup time	SER/Q15	20			20			ns
		P0 thru P15	20			20			
		Mode	35			35			
		R/$\overline{W}$, $\overline{CS}$	35			35			
		SH CLK ↓ to Mode/STR CLK ↑ See Note 2	25			25			
t_h	Hold time	SER/Q15	0			0			ns
		P0 thru P15 'LS673	0			0			
		P0 thru P15 'LS674	5.0			5.0			
		Mode	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 2: This setup time ensures the storage register will see stable data from the shift register.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]		SN54LS' MIN	SN54LS' TYP[‡]	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP[‡]	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	SER/Q15	V_{CC} = MIN, V_{IH} = 2 V,	2.4	3.2		2.4	3.1		V
		Y0 thru Y15[¶]	V_{IL} = V_{IL}max, I_{OH} = MAX	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	SER/Q15	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		Y0 thru Y15[¶]		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	SER/Q15	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL}max, V_O = 2.7 V			40			40	µA
I_{OZL}	Off-state output current, low-level voltage applied	SER/Q15	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL}max, V_O = 0.4 V			−0.4			−0.4	mA
I_I	Input current at maximum input voltage	SER/Q15	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		Others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current	SER/Q15	V_{CC} = MAX, V_I = 2.7 V			40			40	µA
		Others				20			20	
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current[§]	SER/Q15	V_{CC} = MAX	−30		−130	−30		−130	mA
		Y0 thru Y15[¶]		−20		−100	−20		−100	
I_{CC}	Supply current	'LS673	V_{CC} = MAX		50	80		52	80	mA
		'LS674			25	40		25	40	

[†] For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§] Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
[¶] 'LS673 only.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	'LS673 FROM	'LS673 TO	'LS674 FROM	'LS674 TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	SH CLK	SER/Q15	CLK	SER/Q15	R_L = 667 Ω, C_L = 45 pF	20	28		MHz
t_{PHL}	STRCLR	Y0 thru Y15			R_L = 2 kΩ, C_L = 15 pF		25	40	ns
t_{PLH}	MODE/ STRCLK	Y0 thru Y15					28	45	
t_{PHL}							30	45	
t_{PLH}	SH CLK	SER/Q15	CLK	SER/Q15	R_L = 667 Ω, C_L = 45 pF		21	33	ns
t_{PHL}							26	40	
t_{PZH}	$\overline{CS}$, R/$\overline{W}$	SER/Q15	$\overline{CS}$, R/$\overline{W}$	SER/Q15	R_L = 667 Ω, C_L = 45 pF		30	45	ns
t_{PZL}							30	45	
t_{PHZ}	$\overline{CS}$, R/$\overline{W}$	SER/Q15	$\overline{CS}$, R/$\overline{W}$	SER/Q15	R_L = 667 Ω, C_L = 5 pF		25	40	ns
t_{PLZ}							25	40	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
5962-88602013A	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Call TI	
5962-8860201JA	ACTIVE	CDIP	J	24	1	TBD	Call TI	Call TI	
5962-8860201JA	ACTIVE	CDIP	J	24	1	TBD	Call TI	Call TI	
5962-8860201KA	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI	
5962-8860201KA	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI	
5962-8860201LA	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Call TI	
5962-8860201LA	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Call TI	
5962-88607013A	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Call TI	
5962-88607013A	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Call TI	
5962-8860701JA	ACTIVE	CDIP	J	24	1	TBD	Call TI	Call TI	
5962-8860701JA	ACTIVE	CDIP	J	24	1	TBD	Call TI	Call TI	
5962-8860701KA	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI	
5962-8860701KA	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI	
SN54LS673J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	
SN54LS673J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	
SN54LS674J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	
SN54LS674J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	
SN74LS673DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS673DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS673DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS673DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS673DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS673DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS673N	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS673N	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
SN74LS673NE4	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS673NE4	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS674DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS674DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS674DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS674DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS674N	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS674N	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS674NE4	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS674NE4	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNJ54LS673FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS673FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS673J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	
SNJ54LS673J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	
SNJ54LS673JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	
SNJ54LS673JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	
SNJ54LS673W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI	
SNJ54LS673W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI	
SNJ54LS674FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS674FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS674J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	
SNJ54LS674J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	
SNJ54LS674JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	
SNJ54LS674JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	
SNJ54LS674W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI	
SNJ54LS674W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54LS673, SN54LS674, SN74LS673, SN74LS674 :

● Catalog: SN74LS673, SN74LS674

● Military: SN54LS673, SN54LS674

NOTE: Qualified Version Definitions:

     ● Catalog - TI's standard catalog product

     ● Military - QML certified for Military and Defense Applications

MECHANICAL DATA

J (R-GDIP-T**)   **CERAMIC DUAL-IN-LINE PACKAGE**

24 PINS SHOWN

DIM	PINS **	24 NARR	24 WIDE	28 NARR	28 WIDE	32 NARR	32 WIDE	40 NARR	40 WIDE
"A"	MAX	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)
"A"	MIN	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)
"B"	MAX	1.265(32,13)	1.265(32,13)	1.465(37,21)	1.465(37,21)	1.668(42,37)	1.668(42,37)	2.068(52,53)	2.068(52,53)
"B"	MIN	1.235(31,37)	1.235(31,37)	1.435(36,45)	1.435(36,45)	1.632(41,45)	1.632(41,45)	2.032(51,61)	2.032(51,61)
"C"	MAX	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)
"C"	MIN	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)

4040084/C 10/97

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
D. This package can be hermetically sealed with a ceramic lid using glass frit.
E. Index point is provided on cap for terminal identification.

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JT (R-GDIP-T**)
24 LEADS SHOWN

CERAMIC DUAL-IN-LINE

PINS ** DIM	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)

A

24   13

B

1   12

0.070 (1,78)
0.030 (0,76)

0.100 (2,54) MAX

0.015 (0,38) MIN

0.320 (8,13)
0.290 (7,37)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.023 (0,58)
0.015 (0,38)

0.100 (2,54)

0°–15°

0.014 (0,36)
0.008 (0,20)

4040110/C 08/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

MCFP007 – OCTOBER 1994

W (R-GDFP-F24)   CERAMIC DUAL FLATPACK
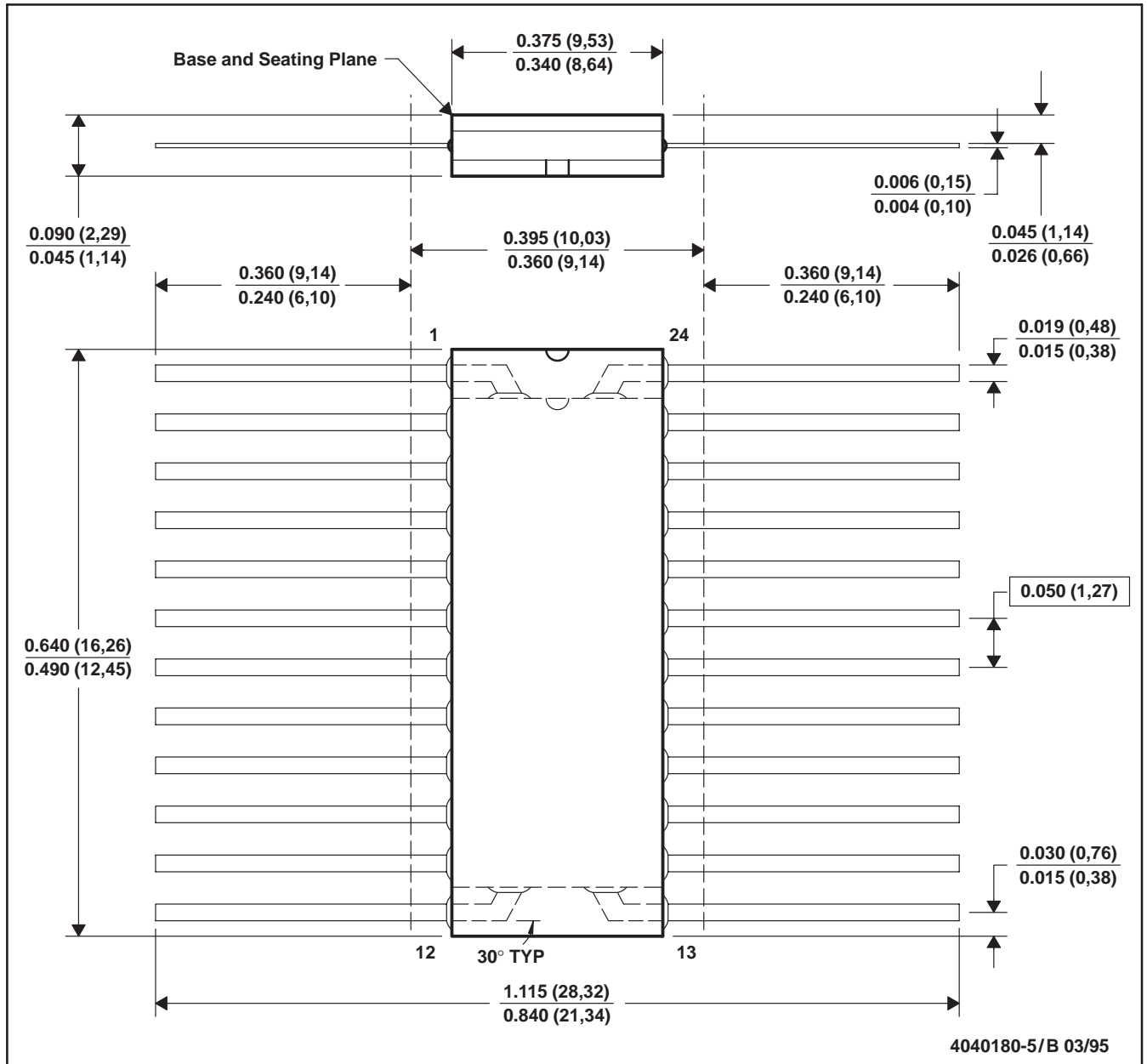
Base and Seating Plane

$\frac{0.375 (9,53)}{0.340 (8,64)}$

$\frac{0.006 (0,15)}{0.004 (0,10)}$

$\frac{0.090 (2,29)}{0.045 (1,14)}$

$\frac{0.045 (1,14)}{0.026 (0,66)}$

$\frac{0.395 (10,03)}{0.360 (9,14)}$

$\frac{0.360 (9,14)}{0.240 (6,10)}$

$\frac{0.360 (9,14)}{0.240 (6,10)}$

$\frac{0.019 (0,48)}{0.015 (0,38)}$

1   24

0.050 (1,27)

$\frac{0.640 (16,26)}{0.490 (12,45)}$

$\frac{0.030 (0,76)}{0.015 (0,38)}$

12   30° TYP   13

$\frac{1.115 (28,32)}{0.840 (21,34)}$

4040180-5 / B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a ceramic lid using glass frit.
        D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
        E. Index point is provided on cap for terminal identification only.

FK (S−CQCC−N**) LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

4040140/D 01/11

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS−004

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N (R–PDIP–T24)   **PLASTIC   DUAL–IN–LINE**
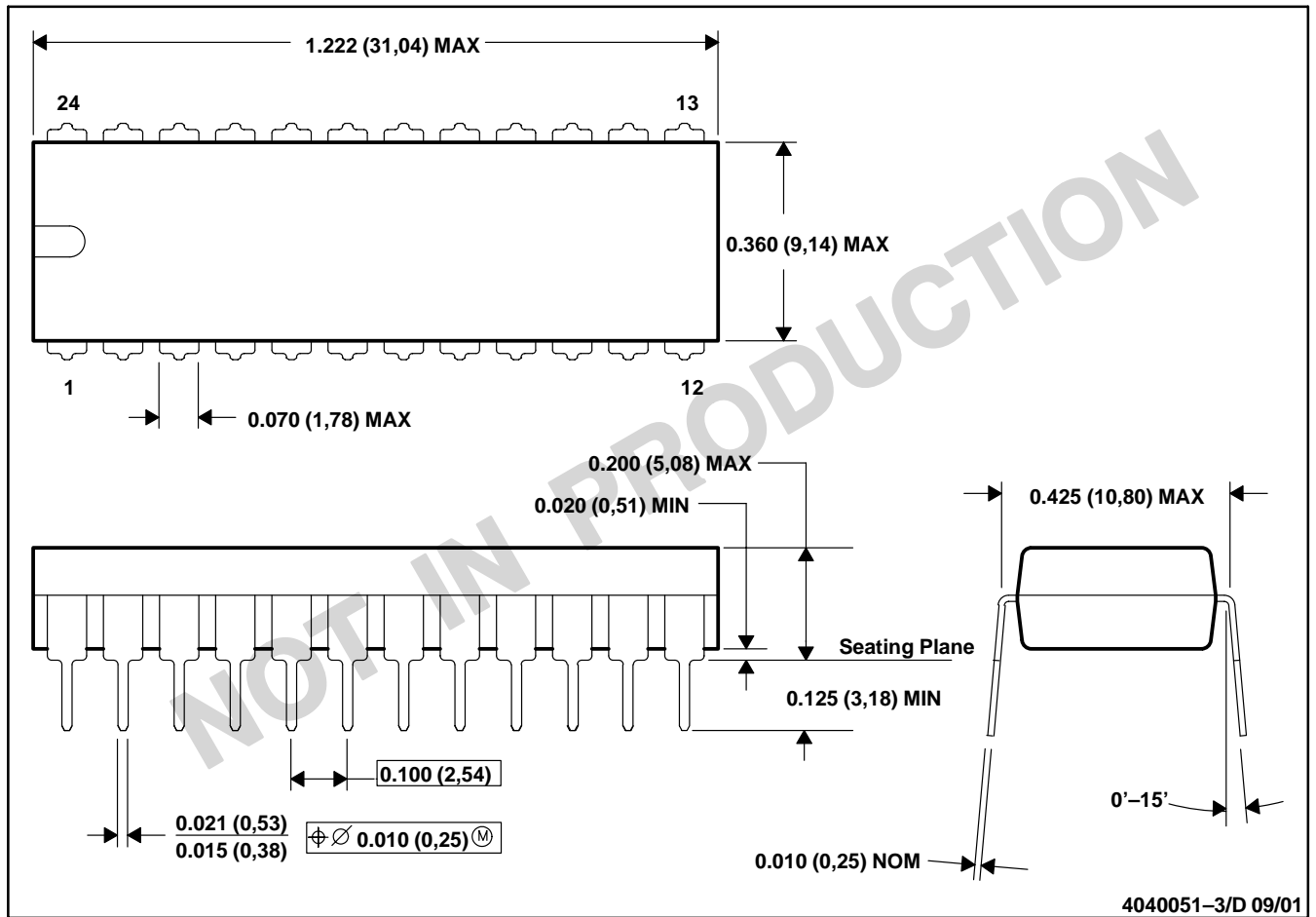
4040051–3/D 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–010

MPDI008 – OCTOBER 1994

N (R-PDIP-T**)   **PLASTIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN

0.560 (14,22)
0.520 (13,21)

0.060 (1,52) TYP

0.200 (5,08) MAX

0.020 (0,51) MIN

0.610 (15,49)
0.590 (14,99)

Seating Plane

0.100 (2,54)

0.125 (3,18) MIN

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.010 (0,25) NOM

0°−15°

PINS ** DIM	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

4040053 / B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Falls within JEDEC MS-011
         D. Falls within JEDEC MS-015 (32 pin only)

DW (R−PDSO−G24)   PLASTIC SMALL OUTLINE

0.614 (15,60)
0.598 (15,20)

24   13

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   12

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−5/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AD.

IMPORTANT NOTICE